

Design Techniques for EMC – Part 1

Circuit Design, and Choice of Components

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This is the first in a series of six articles on best-practice EMC techniques in electrical/electronic/mechanical hardware design, to be published in this journal over the following year. The series is intended for the designer of electronic products, from building block units such as power supplies, single-board computers, and “industrial components” such as motor drives, through to stand-alone or networked products such as computers, audio/video/TV, instruments, etc.

These articles were first published in the EMC Journal as a series during 1999. This version includes a number of corrections, modifications, and additions, many of which have been made as a result of correspondence with the following, to whom I am very grateful: Feng Chen, Kevin Ellis, Neil Helsby, Mike Langrish, Tom Liszka, Alan Keenan, T Sato, and John Woodgate. I am also indebted to Tom Sato for translating these articles into Japanese and posting them on his website: <http://member.nifty.ne.jp/tsato/>, as well as suggesting a number of improvements.

The techniques covered in these six articles are:

- 1) Circuit design (digital, analogue, switch-mode, communications), and choosing components**
- 2) Cables and connectors
- 3) Filters and transient suppressors
- 4) Shielding
- 5) PCB layout (including transmission lines)
- 6) ESD, electromechanical devices, and power factor correction

A textbook could be written about any one of the above topics (and many have), so this magazine article format can do no more than introduce the various issues and point to the most important of the best-practice techniques.

Before starting on the above list of topics it is useful see them in the context of the ideal EMC lifecycle of a new product design and development project.

The project EMC lifecycle

The EMC issues in a new project lifecycle are summarised below:

- Establishment of the target electromagnetic specifications for the new product, including:
 - The electromagnetic environment it must withstand (including continuous, high-probability, and low-probability disturbance events) and the degradation in performance to be allowed during disturbance events;
 - Its possible proximity to sensitive apparatus and allowable consequences, hence the emissions specifications;
 - Whether there are any safety issues requiring additional electromagnetic performance specifications. Safety compliance is covered by safety directives, not by EMC Directive;
 - All the EMC standards to be met, regulatory compliance documentation to be created, and how much “due diligence” to apply in each case (consider all markets, any customers’ in-house specifications, etc.).
- System design:
 - Employ system-level best-practices (“bottom-up”);
 - flow the “top-level” EMC specifications down into the various system blocks (“top-down”).

- System block (electronic) designs:
 - Employ electrical/electronic hardware design best-practices (“bottom-up”) (covered by these six articles);
 - Simulate EMC of designs prior to creating hardware, perform simple EMC tests on early prototypes, more standardised EMC tests on first production issue.
- Employ best-practice EMC techniques in software design.
- Achieve regulatory compliance for all target markets.
- Employ EMC techniques in QA to control:
 - All changes in assembly, including wiring routes and component substitutions;
 - All electrical/electronic/mechanical design modifications and software bug-fixes;
 - All variants.
- Sell only into the markets originally designed for;
 - To add new markets go through the initial electromagnetic specification stage again.
- Investigate all complaints of interference problems
 - Feed any resulting improvements to design back into existing designs and new products (a corrective action loop).

This may look quite daunting, but it is only what successful professional marketeers and engineers already know to do, so as not to expose their company to excessive commercial and/or legal risks.

As electronic technology becomes more advanced, more advanced management and design techniques (such as EMC) are required. There is no escaping the ratcheting effects of new electronic technologies if a company wants to remain profitable and competitive. But new electronics technologies are creating the worlds largest market, expected to exceed US\$1 trillion annually in value (that's \$1 million million) within a couple of years and continue to increase at 15% or so per annum after that. Rewards are there for those that can take the pace.

The following outlines a number of the most important best-EMC-practices. They deal with “what” and “how” issues, rather than with why they are needed or why they work. A good understanding of the basics of EMC is a great benefit in helping to prevent under or over-engineering, but goes beyond the scope of these articles.

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1. Circuit design and choice of components for EMC

Correct choice of active and passive components, and good circuit design techniques used from the beginning of a new design and development project, will help achieve EMC compliance in the most cost-effective way, reducing the cost, size, and weight of the eventual filtering and shielding required.

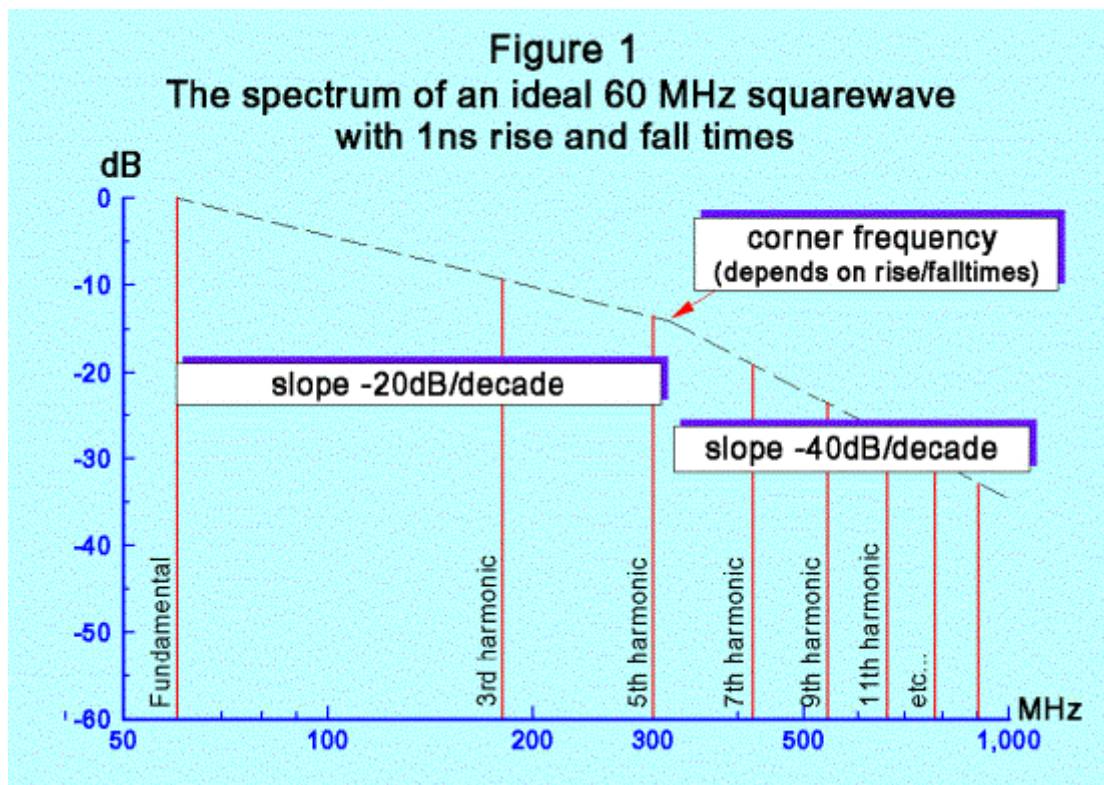
These techniques also improve digital signal integrity and analogue signal-to-noise, and can save at least one iteration of hardware and software. This will help new products achieve their functional specifications, and get to market, earlier. These EMC techniques should be seen as a part of a company's competitive edge, for maximum commercial benefit.

1.1 Digital components and circuit design for EMC

1.1.1 Choosing components

Most digital IC manufacturers have at least one glue-logic range with low emissions, and a few versions of I/O chips with improved immunity to ESD. Some offer VLSI in “EMC friendly” versions (some “EMC” microprocessors have 40 dB lower emissions than regular versions).

Most digital circuits are clocked with squarewaves, which have a very high harmonic content, as shown by Figure 1.



The faster the clock rate, and the sharper the edges, the higher the frequency and emissions levels of the harmonics.

So always choose the slowest clock rate, and the slowest edge rate that will still allow the product to achieve its specification. Never use AC when HC will do. Never use HC when CMOS 4000 will do.

Choose integrated circuits with advanced signal integrity and EMC features, such as:

- Adjacent, multiple, or centre-pinned power and ground.
Adjacent ground and power pins, multiple ground and power pins, and centre-pinned power and ground all help maximise the mutual inductance between power and ground current paths, and minimise their self-inductance, reducing the current loop area of the power supply currents and helping decoupling to work more effectively. This reduces problems for EMC and ground-bounce.
- Reduced output voltage swing and controlled slew rates.
Reduced output voltage swing and controlled slew rates both reduce the dV/dt and dI/dt of the signals and can reduce emissions by several dB. Although these techniques improve emissions, they could worsen immunity in some situations, so a compromise may be needed
- Transmission-line matching I/Os.
ICs with outputs capable of matching to transmission-lines are needed when high-speed signals have to be sent down long conductors. E.g. bus drivers are available which will drive a 25Ω shunt-terminated load. These will drive 1 off 25Ω transmission line (e.g. RAMBUS); or will drive 2 off 50Ω lines, 4 off 100Ω lines, or 6 off 150Ω lines (when star-connected).
- Balanced signalling.
Balanced signalling uses \pm (differential) signals and does not use 0V as its signal return. Such ICs are very helpful when driving high-speed signals (e.g. clocks $> 66\text{MHz}$) because they help to preserve signal integrity and also can considerably improve common-mode emissions and immunity.
- Low ground bounce.
ICs with low ground-bounce will generally be better for EMC too.
- Low levels of emissions.
Most digital IC manufacturers offer glue-logic ranges with low emissions. For instance ACQ and ACTQ have lower emissions than AC and ACT. Some offer VLSI in “EMC friendly” versions, for example Philips have at least two 80C51 microprocessor models which are up to 40dB quieter than their other 80C51 products.
- Non-saturating logic preferred.
Non-saturating logic is preferred, because its rise and fall times tend to be smoother (slew-rate controlled) and so contain lower levels of high-order harmonics than saturating logic such as TTL.
- High levels of immunity to ESD and other disturbing phenomena.
Serial communications devices (e.g. RS232, RS 485) are available with high levels of immunity to ESD and other transients on their pins. If their immunity performance isn't specified to at least the same standards and levels that you need for your product, additional suppression components will be needed.
- Low input capacitance.
Low input capacitance devices help to reduce the current peaks which occur whenever a logic state changes, and hence reduce the magnetic field emissions and ground return currents (both prime causes of digital emissions).
- Low levels of power supply transient currents.

Totem-pole output stages in digital ICs go through a brief period when both devices are on, whenever they switch from one state to the other. During this brief period the supply rail is shorted to 0V, and the power supply current transient can exceed the signal's output current. Both the transient current (sometimes called the 'shoot-through' current) and the voltage noise it causes on the power rails are prime causes of emissions. Relevant parameters may include the transient current's peak value, its dI/dt (or frequency spectrum) and its total charge, any/all of which can be important for the correct design of the power supply's decoupling. ICs with *specified* low levels of power supply transients should be chosen where possible.

- Output drive capability no larger than need for the application.

The output drive current of an IC (especially a bus driver) should be no larger than is needed. Drivers rated for a higher current have larger output transistors, which can mean considerably larger power supply transients. Their increased drive capability can also mean that the traces they drive can experience faster rise and fall times than are needed, leading to increased overshoot and ringing problems for signal integrity as well as higher levels of RF emissions.

All of the above should have guaranteed minimum or maximum (as appropriate) specifications (or at least typical specifications) in their data sheets.

Second-sourced parts (with the same type number and specifications but from different manufacturers) can have significantly different EMC performance – something it is important to control in production to ensure continuing compliance in serial manufacture. If products haven't been EMC tested with the alternative ICs fitted, it will be best to stick with a single source.

Suppliers of high-technology ICs may provide detailed EMC design instructions, as Intel does for its Pentium MMO chips. Get them, and follow them closely. Detailed EMC design advice shows that the manufacturer cares about the real needs of his customers, and may tip the balance when choosing devices.

Some FPGAs (and maybe other ICs) now have the ability to program the slew rate, output drive capability and/or output impedance of their drive signals. Their drive characteristics can be adjusted to give better signal integrity and/or EMC performance and this should help save time in development by reducing the need to replace ICs, change the values of components on the PCB, or modify the PCB layout.

Where ICs' EMC performances are unknown, correct selection at an early design stage can be made by EMC testing a variety of contenders in a simple standard functional circuit that at least runs their clocks, preferably performs operations on high-rate data too.

Testing for emissions can easily be done in a few minutes on a standard test bench with a close-field magnetic loop probe connected to a spectrum analyser (or a wideband oscilloscope). Some devices will be obviously much quieter than others. Testing for immunity can use the same probe connected to the output of a signal generator (continuous RF or transient) – but if it is a proprietary probe (and not just a shorted turn of wire) first check that its power handling is adequate.

Close-field probes need to be held almost touching the devices or PCBs being probed. To locate the "hottest spots" and maximise probe orientation they should first be scanned in a horizontal and vertical matrix over the whole area (holding the probe in different orientations at 90° to each other for each direction), then concentrating on the areas with the strongest signals.

1.1.2 Batch and mask-shrink problems

Some batches of ICs with the same type numbers and manufacturers can have different EMC performance.

Semiconductor manufacturers are always trying to improve the yields they get from a silicon wafer, and one way of doing this is to mask-shrink the ICs so they are smaller. Mask-shrunk ICs can have significantly different EMC performance, because smaller devices means:

- less energy is required (in terms of voltage, current, power or charge) to control the internal transistors, which can mean lowered levels of immunity
- thinner oxide layers, which can mean less immunity to damage from ESD, surge, or overvoltage

- lower thermal capacity of internal transistors can mean higher susceptibility to electrical overstress
- faster operation of transistors, which can mean higher levels of emissions and higher frequencies of emissions.

Large users can usually arrange to get advance warnings of mask-shrinks so they can buy enough of the 'old' ICs to keep them in production while they find out how to deal with the changed EMC from the new mask-shrunk IC.

It is possible to perform simple goods-in checks of IC EMC performance to see whether a new batch has different EMC performance, for whatever reason. This helps discover problems early on, and so save money.

Alternatively, sample-based EMC testing in serial manufacture is required to avoid shipping non-compliant or unreliable products, but it is much more costly to detect components with changed EMC performance this way than it is at goods-in.

1.1.3 IC sockets are bad

IC sockets are very bad for EMC, and directly soldered surface-mount chips (or chip and wire, or similar direct chip termination techniques) are preferred. Smaller ICs with smaller bondwires and leadframes are better, with BGA and similar styles of chip packaging being the best possible to date.

Often the emissions and susceptibility of non-volatile memory mounted on sockets (or, worse still, sockets containing battery backup) ruin the EMC of an otherwise good design. Field-programmable low-profile SMD non-volatile memory ICs soldered direct to the PCB are preferred.

Motherboards with ZIF sockets and spring-mounted heatsinks for their processors (to allow easy upgrading) are going to require additional costs on filtering and shielding, even so it will help to choose surface-mounted ZIF sockets with the shortest lengths of internal metalwork for their contacts.

1.1.4 Circuit techniques

- Level detection (rather than edge-detection) preferred for control inputs and keypresses.
Use level detection ICs for all control inputs and keypresses. Edge detecting ICs are very sensitive to high-frequency interference such as ESD. (If control signals need to use such very high rates that they need to use edge-detecting devices, they should be treated for EMC as for any other high-speed communication link.)
- Use digital edge-rates that are as slow and smooth as possible should be used wherever possible, especially for long PCB traces and wired interconnections (without compromising skew limits).
Where skew is not a problem very slow edges should be used (could be 'squared-up' with Schmitt gates where locally necessary).
- On prototype PCBs allow for control of logic edge speed or bandwidths (e.g. with soft ferrite beads, series resistors, RC or Tee filters at driven ends).
Many IC data books don't specify their output rise or fall times at all (or only specify the maximum times, leaving typical rates unspecified). Because it is often necessary to control unwanted harmonics, it is advisable to make provision for control of logic edge speed or bandwidths, (on prototype PCBs at least).
Series resistors or ferrite beads are usually the best way to control edge rates and unwanted harmonics, although R-C-R tee filters can also be used and may be able to give better control of harmonics where transmission lines are used. (simple capacitors to ground can increase output transient currents and increase emissions.)
- Keep load capacitance low.

This reduces the output current transient when the logic state changes over and helps to reduce magnetic field emissions, ground bounce, and transient voltage drops in the ground plane and power supply, all important issues for EMC.

- Fit pull-ups for open-collector drivers near to their output devices, using the highest resistor values that will work.

This helps reduce the current loop area and the maximum current, and so helps to reduce magnetic field emissions. However, this could worsen immunity performance in some situations, so a compromise may be needed.

- Keep high speed devices far away from connectors and wires.

Coupling (e.g. crosstalk) can occur between the metallisation, bond wires, and lead frame inside an IC and other conductors nearby. These coupled voltages and currents can greatly increase CM emissions at high frequencies. So keep high speed devices away from all connectors, wires, cables, and other conductors. The only exception is high-speed connectors dedicated to that IC (e.g. motherboard connectors).

When a product is finally assembled, flexible wires and cables inside may lie in a variety of positions. Ensure that no wires or cables can lie near any high-speed devices. (Products without internal wires or cables are usually easier to make EMC compliant anyway.)

A heatsink is an example of a conductor, and clearly can't be located a long way away from the IC it is to be cooling. But heatsinks can suffer from coupled signals from inside an IC just like any other conductor. The usual technique is to isolate the heatsink from the IC with a thermal conductor (the thicker the better as long as thermal dissipation targets are met), then 'ground' the heatsink to the local ground plane with many very short connections (the mechanical fixings can often be used).

- A good quality watchdog that 'keeps on barking' is required.

Interference often occurs in bursts lasting for tens or hundreds of milliseconds. A watchdog which is supposed to restart a processor will be no good if it allows the processor to be crashed or hung permanently by later parts of the same burst that first triggered the watchdog. So it is best if the watchdog is an astable (not a monostable) that will keep on timing out and resetting the microprocessor until it detects a successful reboot. (Don't forget that the watchdog's timeout period must be longer than the processor's rebooting time.)

AC-coupling of the watchdog input from a programmable port on the micro helps ensure reliable watchdog operation. For more on watchdogs, see section 7.2.3 in [1].

- An accurate power monitor is needed (sometimes called a 'brownout' monitor).

Power supply dips, dropouts interruptions, sags, and brownouts can make the logic's DC rail drop below the voltage required for the correct operation of logic ICs, leading to incorrect functioning and sometimes over-writing areas of memory with corrupt instructions or data. So an accurate power monitor is required to protect memory and prevent erroneous control activity. Simple resistor-capacitor 'power-on reset' circuits are almost certainly inadequate.

- Never use programmable watchdogs or brownout monitors.

Because programmable devices can have their programs corrupted by interference, programmable devices must not be used for watchdog or power monitor functions.

- Appropriate circuit and software techniques also required for power monitors and watchdogs so that they cope with most eventualities, depending on the criticality of the product, (not discussed further in this series of articles).

- High quality RF bypassing (decoupling) of power supplies is vital at every power or reference voltage pin of an IC (refer to Part 5 of this series).

- High quality RF reference potential and return-current planes (usually abbreviated to 'ground planes') are needed for all digital circuits (refer to Part 5 of this series).

- Use transmission line techniques wherever the rise/fall time of the logic signal edge is shorter than the “round trip time” of the signal in the PCB track (transmission lines are described in detail in the 5th article in this series).

Rule of thumb: round trip time equals 13ps for every millimetre of track length. For best EMC it may be necessary to use transmission line techniques for tracks which are even shorter than this rule of thumb suggests.

- Asynchronous processing is preferred.

Asynchronous (naturally clocked) techniques have much lower emissions than synchronous logic, and much lower power consumption too. ARM have been developing asynchronous processors for many years, and other manufacturers are now beginning to produce asynchronous products.

One of the limitations on designing asynchronous ICs was the lack of suitable design tools (e.g. timing analysers). But at least one asynchronous IC design tool is now commercially available.

Some digital ICs emit high level fields from their own bodies, and often benefit from being shielded by their own little metal box soldered to the PCB ground plane. Shielding at PCB level is very low-cost, but can't always be applied to devices that run hot and need free air circulation.

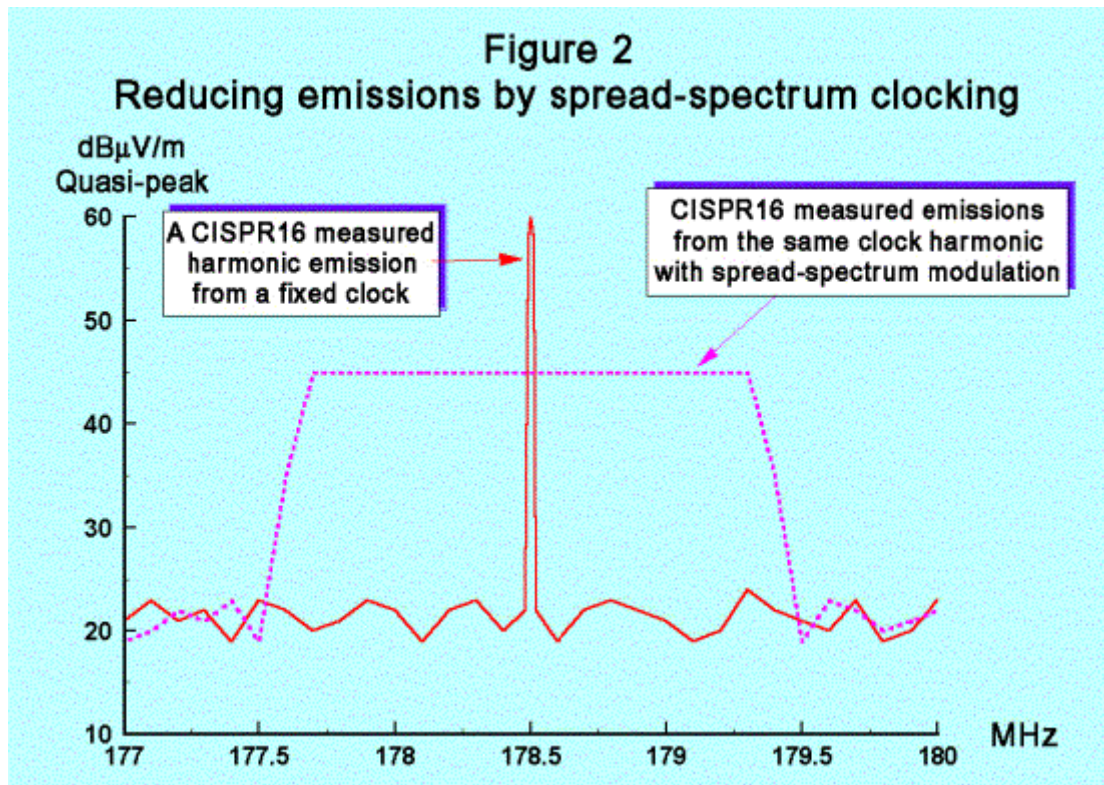
Clock circuits are usually the worst offenders for emissions, and their PCB tracks will be the most critical nets on a PCB, requiring component layout to be adjusted to minimise clock track length and keep each clock track on one layer with no via holes.

When a clock must travel a long distance to a number of loads, fit a clock buffer near the loads so the long track (or wire) has smaller currents in it. Where relative skew is not a problem clock edges in the long track should be well-rounded, even sine-waves, squared up by the buffer near the loads.

1.1.5 Spread-spectrum clocking

So-called "spread-spectrum clocking" is a recent technique that reduces the measured emissions, although it doesn't actually reduce the instantaneous emitted power so could still cause the same levels of interference with some fast-responding devices. It modulates the clock frequency by 1 or 2% to spread the harmonics and give a lower peak measurement on CISPR16 or FCC emissions tests. The reduction in measured emissions relies upon the bandwidths and integration time constants of the test receivers, so is a bit of a trick, but has been accepted by the FCC and is in common use in the US and EU. The modulation rates in the audio band so as not to compromise clock squareness specifications.

Figure 2 shows an example of an emission improvement for one clock harmonic.



Debate continues about the possible effects of spread-spectrum clocking on complex digital ICs with the suppliers claiming no problems and some pundits still urging caution, but at least one major manufacturer of high-quality PC motherboards is using this technique as standard on new products.

Spread-spectrum clocking should not be used for timing-critical communications links, such as Ethernet, Fibre channel, FDDI, ATM, SONET, and ADSL.

Most of the problems with emissions from digital circuits are due to synchronous clocking. Asynchronous logic techniques (such as the AMULET microprocessors being developed by Prof. Steve Furber's group at UMIST) will dramatically reduce the total amount of emissions and also achieve a true spread-spectrum instead of concentrating emissions at narrow clock harmonics.

1.2 Analogue components and circuit design

1.2.1 Choosing analogue components

Choosing analogue components for EMC is not as straightforward as for digital because of the greater variety of output waveshapes. But as a general rule for low emissions in high-frequency analogue circuits: slew rates, voltage swings, and output drive current capability should be selected for the minimum necessary to achieve the function (given device and circuit tolerances, temperature, etc.).

But the biggest problem for most analogue ICs in low-frequency applications is their susceptibility to demodulating radio frequency signals which are outside their linear band of operation, and there are few if any data sheet specifications which can act as a guide for this. Specifications and standards for immunity testing of ICs are being developed, and in the future it may be possible to buy ICs which have EMC specifications on their data sheets.

Different batches, second-sourced, or mask-shrunk analogue ICs can have significantly different EMC performance for both emissions and immunity. It is important to control these issues by design, testing, or purchasing to ensure continuing compliance in serial manufacture, and some suitable techniques were described earlier (section on choosing digital ICs).

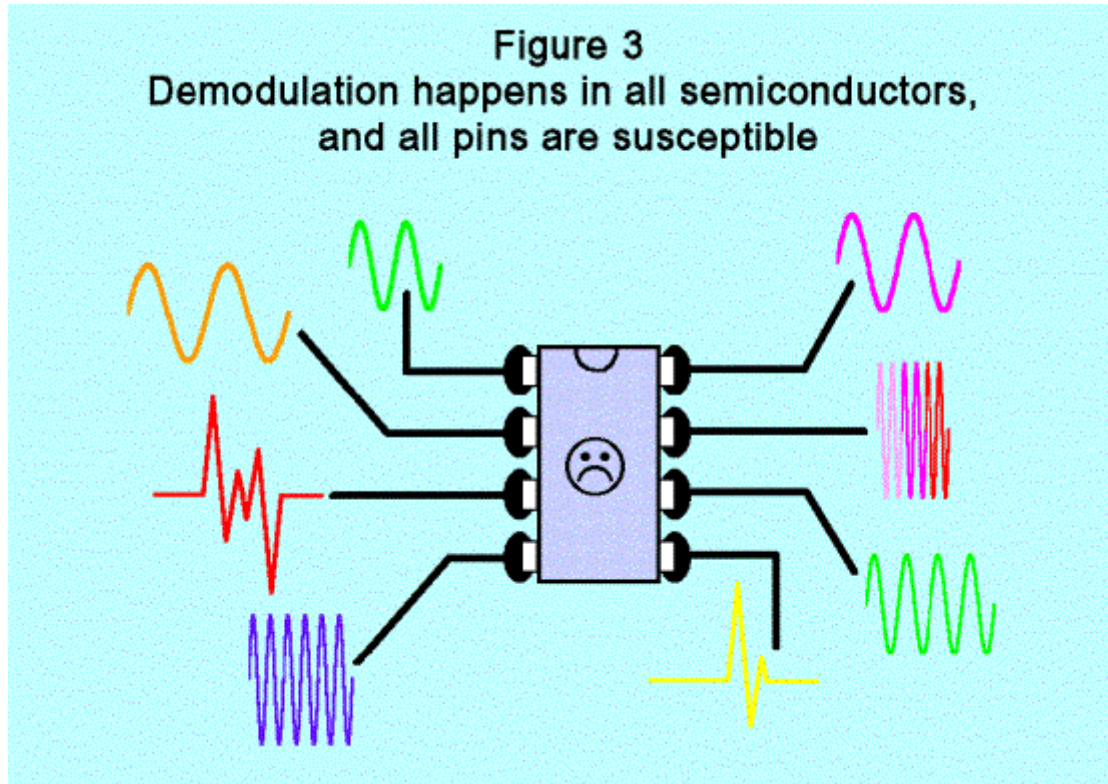
Manufacturers of sensitive or high-speed analogue parts (and data converters) often publish EMC or signal-to-noise application notes for circuit design and/or PCB layout. This usually shows they have

some care for the real needs of their customers, and may help tip the balance when making a purchasing decision.

1.2.2 Preventing demodulation problems

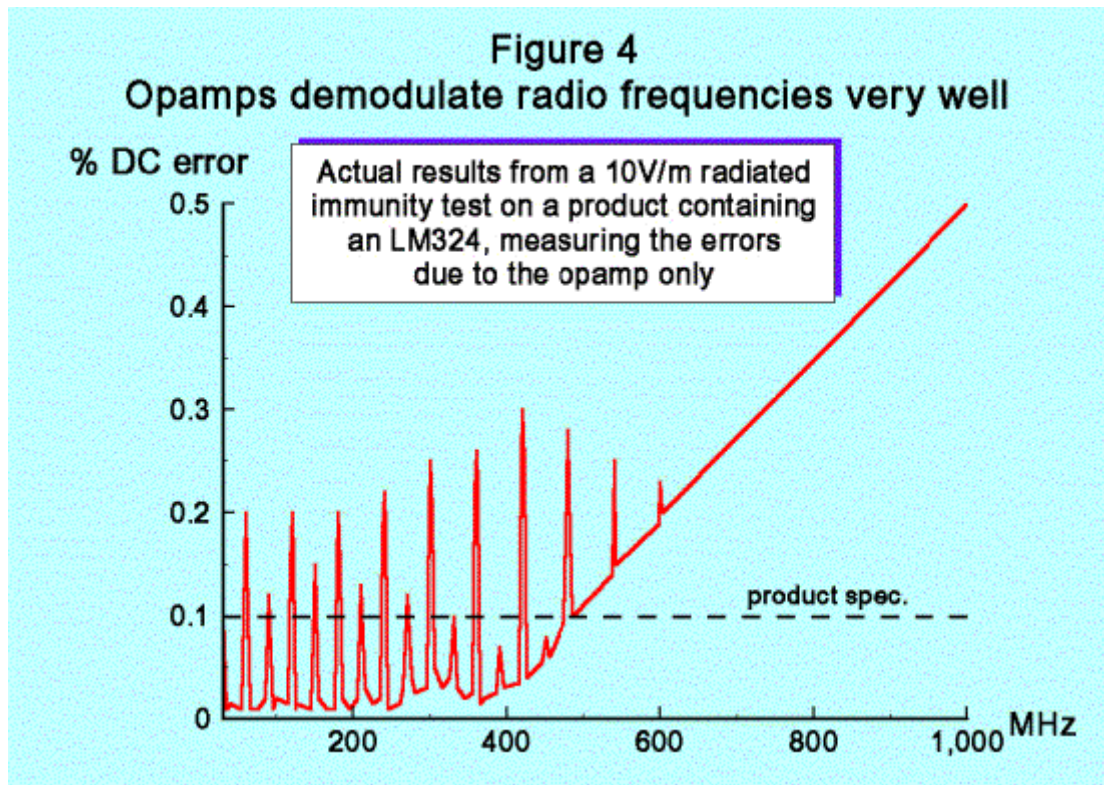
Most of the immunity problems with analogue devices are caused by RF demodulation.

Opamps are very sensitive to RF interference on all their pins, regardless of the feedback schemes employed (see Figure 3).



All semiconductors demodulate RF. Demodulation is more common problem for analogue circuits, but can produce more catastrophic effects in digital circuits (when software gets corrupted).

Even slow opamps will happily demodulate interference up to cellphone frequencies and beyond, as shown by the real product test results of Figure 4. To help prevent demodulation, analogue circuits need to remain linear and stable during interference. This is a particular problem for feedback circuits. Test the stability and linearity of the feedback circuit by removing all input and output loads and filters, then injecting very fast-edged ($<1\text{ns}$ risetime) square waves into inputs (and possibly into outputs and power supplies, via small capacitors). The test signal amplitude is set so that the output pk-pk is about 30% maximum, to prevent clipping. The test signal's fundamental frequency should be near the centre of the intended passband of the circuit.



The circuit's output is observed with a 100MHz (at least) oscilloscope and probes for its slew rate, overshoot and ringing, even for audio or instrument circuits. For higher-speed analogue circuits use an appropriately faster 'scope and take great care to use appropriate high-speed probing techniques.

Feedback circuits should be adjusted so that slew rates are maximised, overshoots are low (heights of more than 50% of the signal's nominal height indicate instability). Any long periods of ringing (say, longer than two cycles) or bursts of oscillation also indicate instability.

Different batches of ICs can have very different stability performance, most easily simulated by cooling and heating the device under test over a wide range of temperatures (say: -30 to + 180oC) and ensuring the circuit is as fast and stable as it is possible to achieve over the whole temperature range.

Testing could use a swept frequency instead, with a spectrum analyser at the output. Take care not to overdrive the spectrum analyser's input.

1.2.3 Other analogue circuit techniques

Achieving good stability in feedback circuits usually requires that capacitive loads be buffered with a small resistance or choke which is outside the feedback loop.

Integrator feedback circuits usually need a small resistor (often around 560Ω) in series with every integrator capacitor larger than about 10pF.

Never try to filter or control RF bandwidth for EMC with active circuits – only use passive (preferably RC) filters outside any feedback loops. The integrator feedback method is only effective at frequencies where the opamp has considerably more open-loop gain than the closed-loop gain required by its circuit. It cannot control frequency response at higher frequencies.

Having achieved a stable and linear circuit, all of its connections might need protecting by passive filters or other suppression methods (e.g. opto-isolators). Any digital circuits in the same product will cause noise on all internal interconnections, and all external connections will suffer from the external electromagnetic environment.

Filtering is covered in Part 3 of this series, and the filters associated with an IC should connect to its local 0V plane. Filter design can be combined with galvanic isolation (e.g. a transformer) to provide

protection from DC to many GHz. Using balanced (differential) inputs and outputs can help reduce filter size while maintaining good rejection at lower frequencies.

Input or output filters are always needed where external cables are connected, but may not be necessary where opamps interconnect with other opamps by PCB traces over a dedicated 0V plane. Any wired interconnections inside unshielded enclosures might need filtering due to their antenna effect, as might wired interconnections inside shielded enclosures which also contain digital processing or switch-mode converters.

Analogue ICs need high-quality RF decoupling of all their power supplies and voltage reference pins, just as do digital ICs. RF decoupling techniques are described later in this volume.

But analogue ICs often need low-frequency power supply bypassing because the power supply noise rejection ratio (PSRR) of analogue parts are usually increasingly poor for frequencies above 1kHz. RC or LC filtering of each analogue power rail at each opamp, comparator, or data converter, may be needed. The corner frequency and slope of such power supply filters should compensate for the corner frequency and slope of device PSRR, to achieve the desired PSRR over the whole frequency range of interest.

Transmission line techniques may be essential for high-speed analogue signals (e.g. RF signals) depending on the length of their connection and the highest frequency to be communicated (see Part 5 of this series). Even for low-frequency signals, immunity will be improved by using transmission line techniques for interconnections, since correctly matched transmission lines of any length behave as very poor antennas and don't resonate.

Not many EMC design guides mention RF design. This is because RF designers are generally very good with most continuous EMC phenomena. However, local oscillators and IF frequencies often leak too much, so may need more attention to shielding and filtering.

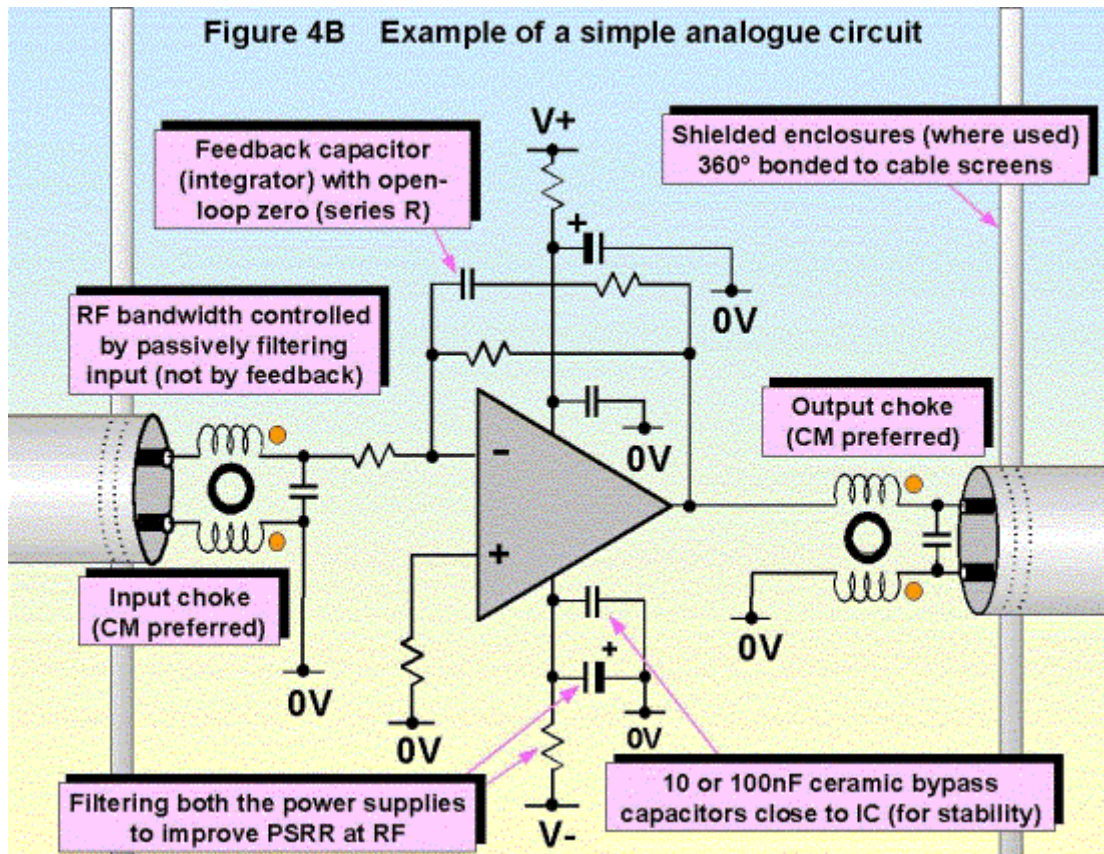
Avoid the use of very high-impedance inputs or outputs. they are very sensitive to electric fields. Because the wave impedance of air is 377Ω , electric fields dominate outside of the near field of an emissions source.

Because most of the emissions from products are caused by common-mode voltages and currents, and because most environmental electromagnetic threats (simulated by immunity testing) are common-mode, using balanced send and receive techniques in analogue circuits has many advantages for EMC, as well as for reducing crosstalk. Balanced circuits drive antiphase (\pm) signals over two conductors, and does not use the 0V system for the return current path. Sometimes called differential signalling.

Comparators must have hysteresis (positive feedback) to prevent false output transitions due to noise and interference, also to prevent oscillation near to the trip point. Don't use faster output-slewing comparators than are really necessary (i.e. keep their dV/dt low).

Some analogue ICs themselves are particularly susceptible to radiated fields. They may benefit from being shielded by their own little metal box soldered to the PCB ground plane (take care to provide adequate heat dissipation too).

Figure 4B shows a simple opamp circuit (inverting amplifier) with some of the techniques described above applied. Even though the circuit uses single-ended signalling (i.e. uses 0V as the signal return) and is not balanced, common mode chokes will generally improve the EMC performance when used in the input and output filters.



Input or output filters are always needed where external cables are connected, but may not be necessary where opamps interconnect with other opamps by PCB traces over a dedicated 0V plane. Any wired interconnections inside unshielded enclosures may also need filtering, as might wired interconnections inside shielded enclosures which also contain digital processing or switch-mode converters.

1.3 Switch-mode design

This technology is inherently electromagnetically noisy and will produce lots of interference if not firmly controlled, as outlined below. These techniques will also help make switch-mode power supplies low-noise enough to power sensitive analogue circuits.

1.3.1 Choice of topology and devices

Always switch power softly rather than abruptly, keeping both dV/dt and dI/dt low at all times. There are a number of circuit topologies which produce minimum emissions by reducing dV/dt and/or dI/dt , whilst also reducing the stresses on the switching transistors. These include ZVS (zero-voltage switching), ZCS (zero current switching), resonant mode (a type of ZCS), SEPIC (single-ended primary inductance converter), Cük (an integrated magnetics topology, named after its inventor), etc.

In traditional (more noisy) topologies, where the power devices are not switched at zero volts or zero current, it is *not* true to say that reducing switching time *always* leads to efficiency improvements. All systems, circuits, and components (especially wound components) have natural resonant frequencies at radio frequencies. When the waveforms used by a circuit contain spectral components close to these natural resonant frequencies their resonances will become 'excited' and cause ringing, unwanted oscillations and emissions, and voltage overshoots that can increase the dissipation in power switching devices and even damage them.

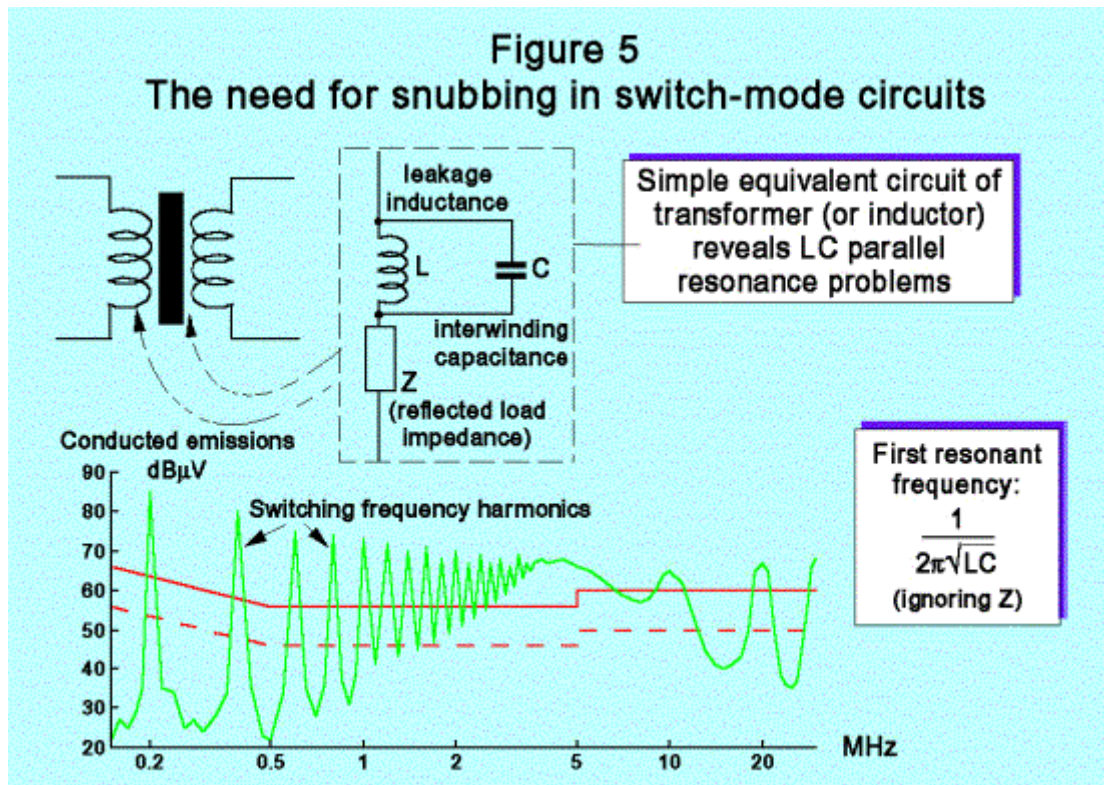
Suppressing these resonances requires snubbing techniques which are usually lossy, as well as requiring costly components and PCB area. So switching at an ever-faster rate (which means increasingly high frequency content) eventually leads to diminishing efficiency and/or worsened reliability. For the most cost-effective design overall – soft-switching techniques trade a percentage point or two of device dissipation for much lower costs and sizes of filtering and shielding, minimum heatsink sizes and good reliability.

From an EMC point of view, faster switching edges means more energy in higher-frequency harmonics, hence larger and more complex filters and shielding. In poorly designed switch-mode power converters, harmonics of up to 1000 times the basic switching rate often cause failure to meet emissions tests.

One of the problems with switching power FETs is that their rate of change of drain voltage is a non-linear function of their gate voltage. Using the 'gate charge model' (which includes the 'Miller effect' from C_{dg}) provides much better accuracy when designing gate drive circuits so that they control the dV/dt at the drain.

1.3.2 Snubbing

Snubbing is usually required to protect the switching transistors from the peak voltages produced by the resonance of stray elements in the circuit components. Figure 5 shows the stray leakage inductance and inter-winding capacitance typical of an isolating transformer.



These form a resonant circuit which causes larger voltage overshoots the more abruptly its current is switched. On an emissions spectrum these resonances are often seen as a regular variation in the envelope of the emissions.

In the case of transformers, snubbers are connected across the winding whose overshoots are to be suppressed. Snubbers come in many types: A resistor and capacitor in series (RC type) is usually the best for EMC but can run hotter than other types.

Be prepared to compromise, and beware of using inductive components in snubbers. Inductance compromises snubber performance, so very low-inductance power resistors and pulse-rated capacitors should be used, with very short leads to the winding concerned.

1.3.3 Heatsinks

Heatsinks have around 50pF of capacitance to the collectors or drains of a TO247 power device, and similar capacitances to other package styles, so are strongly-coupled with the dV/dt of the collector or drain and can create strong emissions of electric fields through their own stray capacitances to other components either inside the product or the outside world. It is usually best to connect primary switching device heatsinks directly to one of the primary DC power rails – taking full account of all safety requirements, including a clear warning on or near the heatsink that it is live.

Heatsinks could be capacitively connected to the hazardous rail to improve safety, and it may even be possible to “tune” the capacitance with the length of its leads and traces to minimise troublesome frequencies.

It is important to return the RF current injected into the heatsink (via its 50pF or so capacitance) as quickly as possible back to its source whilst enclosing the smallest loop area, to avoid replacing an electric-field emissions problem with a magnetic field emissions problem. Always allow for some iteration on a prototype to find the best heatsink suppression method (for instance, which DC rail is the best to connect the heatsink to).

An alternative is to use shielded heat-sink thermal insulators. Their shielded inner layer is connected to the appropriate DC rail. The heatsink itself can remain isolated or else be connected to chassis. Although this is the safest, it is more costly.

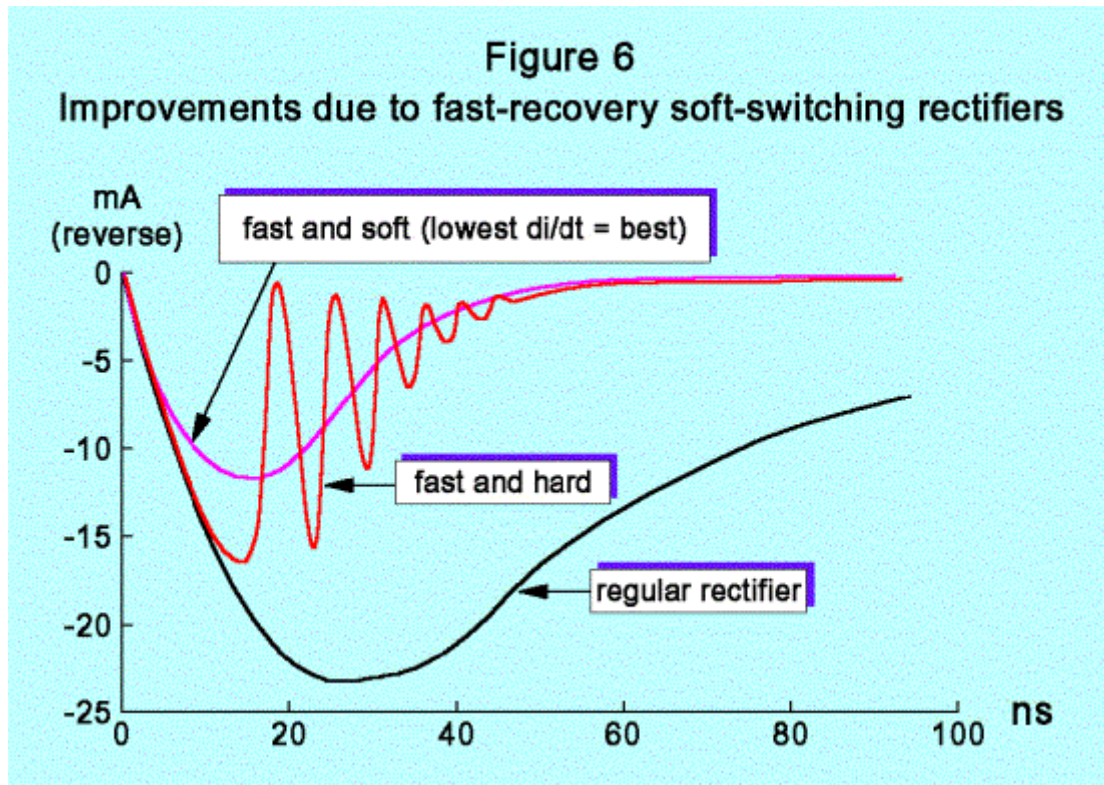
Similar problems afflict the heatsinks of secondary rectifiers, but their heatsinks can usually be connected to their local 0V with no safety worries.

1.3.4 Rectifiers

The rectifiers used for primary flywheels and secondary rectifiers can cause a great deal of noise (hence emissions) due to their reverse current flow.

Faster-switching devices need less reverse charge (current x time) and can cause less noise. But if they are hard-switching types they can excite resonances in the switcher components (especially the isolation transformer) and cause excessive overshoots and emissions.

It is best for EMC to use rectifier types which have fast operation but soft-switching characteristics, as shown by Figure 6.



1.3.5 Problems and solutions relating to magnetic components

Pay particular attention to closing the magnetic circuits of inductors and transformers, e.g. using toroids or gapless cores. Iron powder toroidal cores are available for energy-storage magnetics, these effectively have a distributed air gap and so emit lower fields than gapped cores.

If air gaps have to be used, for instance in C, E or pot cores, an *overall* shorted turn may be needed to reduce the leakage fields. 'Overall' means that it goes around the *entire* body of the transformer, so it is only a shorted turn for the leakage fields.

Primary switching noise is injected via the interwinding capacitance of isolating transformers, creating common-mode noise in the secondaries. These noise currents are difficult to filter, and travel long distances, enclosing large loop areas (to keep Mr Kirchoff happy) thereby creating emissions problems.

Interwinding shields in an isolating transformer can suppress primary switching noise in the secondaries. One shield is a great help, and should be connected to a primary DC rail. Up the five shields is not unheard of, but three is more likely. When using three shields, the shield adjacent to the secondary windings usually connects to the common output ground (if there is one) and the shield in the middle usually connects to chassis. Be prepared to iterate a prototype to find their best connections.

PCB-transformers are becoming increasingly popular, and adding shields to these is simply a matter of adding more PCB layers (making sure that creepage and clearance distances are achieved despite tolerances in PCB manufacture).

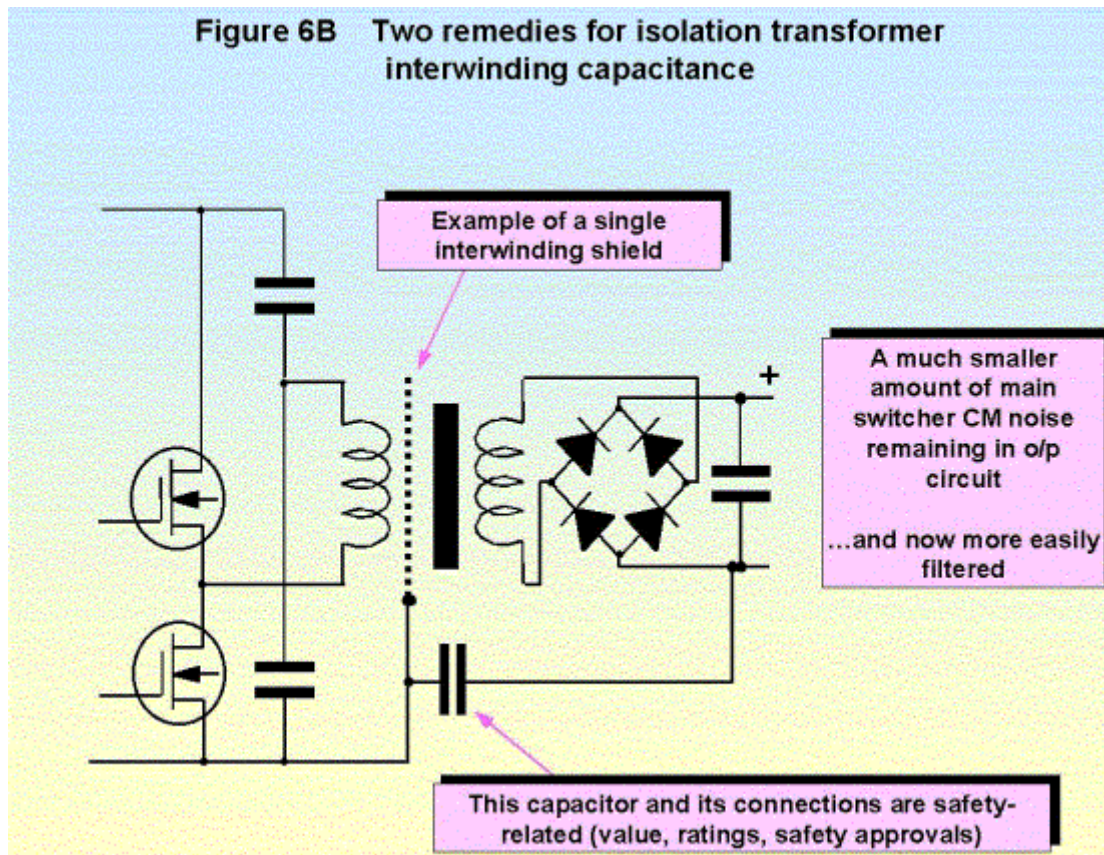
Another powerful technique is to provide a local return path for these currents with small (safety approved!) capacitors connected between the secondary ground and one of the primary power rails.

Make sure that these capacitors don't cause the total earth leakage current to exceed the specification in the relevant safety standard.

These capacitors also help any filters on the secondaries to work much better, by reducing the source impedance of the emissions so that common-mode chokes can function effectively.

The above two techniques also reduce the secondary switching noise which appears at the input, via the isolating transformer's interwinding capacitance. The primary to secondary capacitor also makes filtering at the input more effective.

Figure 6B shows a simple switcher with a single interwinding shield and a primary-secondary bridging capacitor.



1.3.6 Spread-spectrum clocking for switch-mode

'Spread-spectrum clocking' techniques as described in 1.1.5 above can also be used with some switch-mode topologies to spread the emissions spectrum of the individual harmonics so that they measure less on an EMC test. Commercial and industrial conducted emissions tests use a 9kHz bandwidth from 150kHz to 30MHz, so spreading a harmonic by $\pm 90\text{kHz}$ can give reductions of more than 10dB.

The spreading range can often be much larger than 1 or 2%, and some high-power converter manufacturers use almost white noise.

1.4 Signal communication components and circuit design

1.4.1 Non-metallic communications are best

The best communications for EMC purposes are infrared or optical, via free-space (e.g. IRDA) or fibre-optics. Their transmitters must not emit too much, and the receivers must be immune enough, but these are usually easier to control than the EMC of a long cable. Metal-can shielded transmitters and receivers are now readily available. It is often possible to bring metal-free fibre-optic cables right through the walls of shielded enclosures to PCBs or modules inside, without compromising the

enclosure shielding, whereas metallic wires and cables need to be filtered and/or 360° shield bonded at the points where they cross shielded enclosure boundaries.

Wireless communications are another alternative, but because they use the radio spectrum they sometimes cause interference with nearby electronics, and they can also be interfered with by electromagnetic disturbances.

Wires and cables may appear at first sight to be more cost-effective, but by the time their EMC problems have eventually been solved at the end of a project the non-metallic alternatives would often have been preferable for reasons of cost and timescale. Another reason for using non-metallic communications is that galvanic isolation to very high values is automatically achieved, improving product reliability and greatly easing the risks of failing EMC tests.

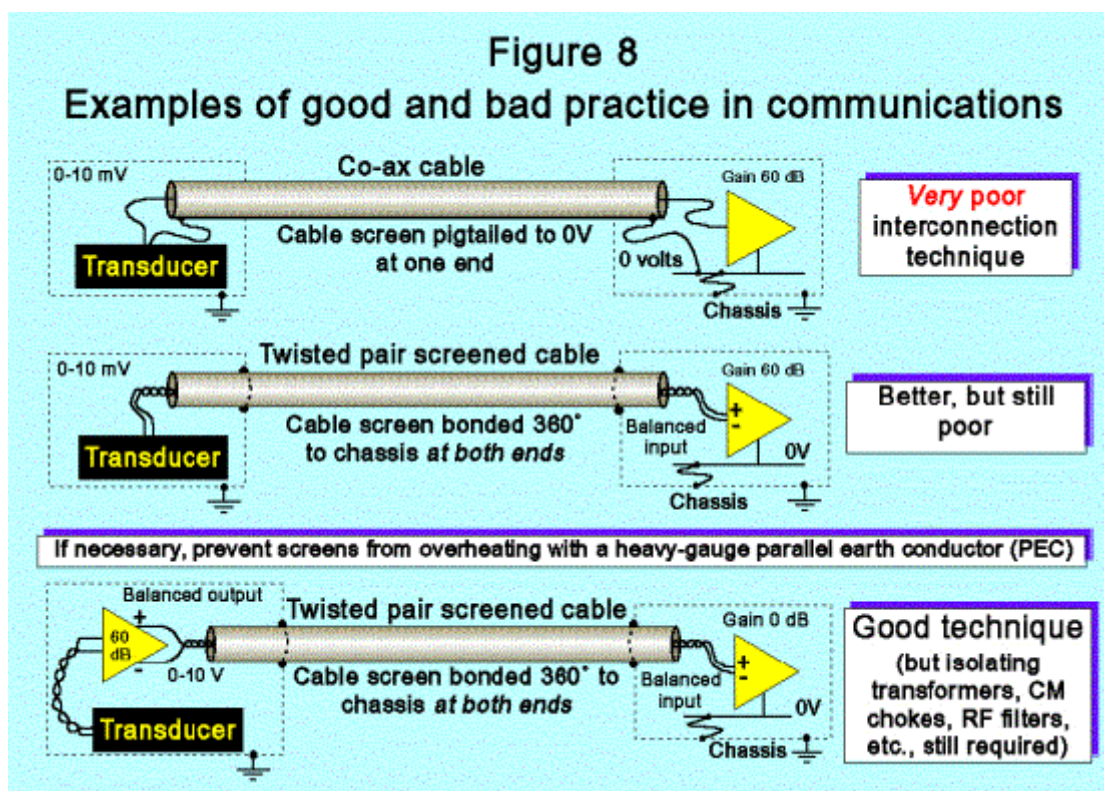
Wires and cables are usually cost-effective within a fully shielded product enclosure, but even then 'internal EMC' problems and the slow propagation velocity in cables can make infra-red or optical alternatives more attractive. (Don't forget to take account of the delays in the infra-red or optical transceivers themselves into account.)

1.4.2 Techniques for metallic communications

Single-ended signal communication techniques have very poor EMC performance for both emissions and immunity, and are best restricted to low frequency, low data rate, or short distance applications. They are usually all right as long as they remain on a PCB with a solid ground plane under all the tracks and don't go through any connectors or cables, which means that the single-PCB product is often the most cost-effective.

High-frequency or long-distance signals should be sent/ received as balanced signals (sometimes even on PCBs) for good signal integrity and EMC, and this is going to be a main issue in this sub-section.

Figure 8 shows examples of good and bad practices when connecting a millivolt output transducer to an amplifier via a cable.



In general, connecting a cable shield to a circuit's 0V is very bad practice, as is the use of pigtails and grounding cable screens at one end only. Some older textbooks divide cables up into low and high frequency types, with different shield-bonding rules for each. But the electromagnetic environment is now so polluted with RF threats (and as was shown earlier, even 'slow' opamps will demodulate

>500MHz), and so many signals are polluted with RF common-mode noise from digital processors inside their products, that all cables should now be treated as high-frequency.

The three schemes in figure 8 show a hierarchy from a poor system for connecting to a transducer, through a better one, to a good system. Fitting an A/D converter in the transducer enclosure and sending high-level encoded data (with error-correction) over the cable to the product for decoding would be better than the best shown opposite. A perfect system would send the digital data over a fibre-optic instead of a metallic cable, and such systems are increasingly used in industry.

Concerns about cable shield heating in large or industrial premises are best dealt with by running the communications cable over a parallel earth conductor (PEC) to divert the majority of the heavy low-frequency currents (which will prefer to follow paths with lower *resistance*) and not by 'lifting' a shield connection at one end – which ruins the cable's shielding benefits at that end. Fitting a capacitor in series with the shield at one end is also not recommended as a design technique, although it may be useful as a remedial technique, because it is very difficult to make a capacitive bond work effectively over the full range of frequencies. PECs and other installation cabling and earthing techniques are discussed in detail in [2] [3] and [4].

For low frequency signals (say, under 100kHz) higher voltage levels in the communication link are better, for reasons of immunity. Where signal frequencies are above 10MHz (say) high voltages can lead to high levels of emissions – lower voltages are often preferred as the best compromise (e.g. as used by ECL, LVDS, USB). The signal frequency at which lower voltages are preferred depends on the length of cable and its type and EMC performance (especially its longitudinal conversion loss) and the design of the transmit and receive circuits.

Transmission line techniques may be essential for high-speed analogue or digital signals, depending on the length of their connection and the highest frequency to be communicated (see Part 5 of this series). Even for low-frequency signals, immunity will be improved by using transmission line techniques for their interconnections.

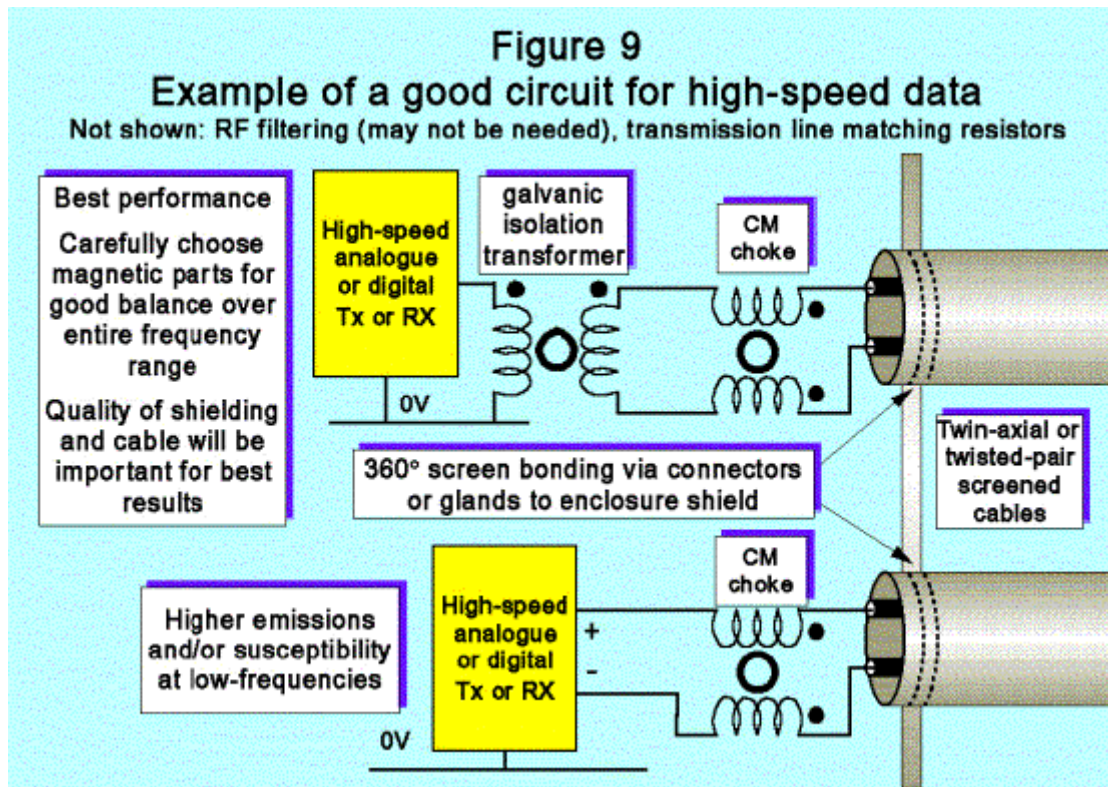
The best type of cable for EMC usually has a dedicated return conductor associated with each signal conductor, and any cable shields are used only to control interference. Co-axial cable is generally not preferred. Some cables need individually shielded signal pairs. It is very important to achieve a good *balance* over the whole frequency range, as this means a good common-mode rejection ratio (CMRR) and hence improved emissions and immunity. Balanced send / receive ICs are good, but isolation transformers have the benefit of adding galvanic isolation (up to the point where they flash-over) and also extending the common-mode range well beyond the DC supply rails.

Balanced construction twisted-pair or twinaxial cables usually give the best and most cost-effective emissions and immunity performance and very small differences in twist (and even the dielectric constants of the pigments used to colour their insulation) can be important. Balance is so important that in high-performance circuits even a physically balanced (mirror-image) PCB layout will be needed, using the same PCB layers.

Transformers and balanced send/receive ICs all suffer from degraded balance at RF. They generally require a common-mode choke in series to maintain good balance over the whole frequency range of interest. The CM choke always goes closest to the cable or connector at the boundary of the product.

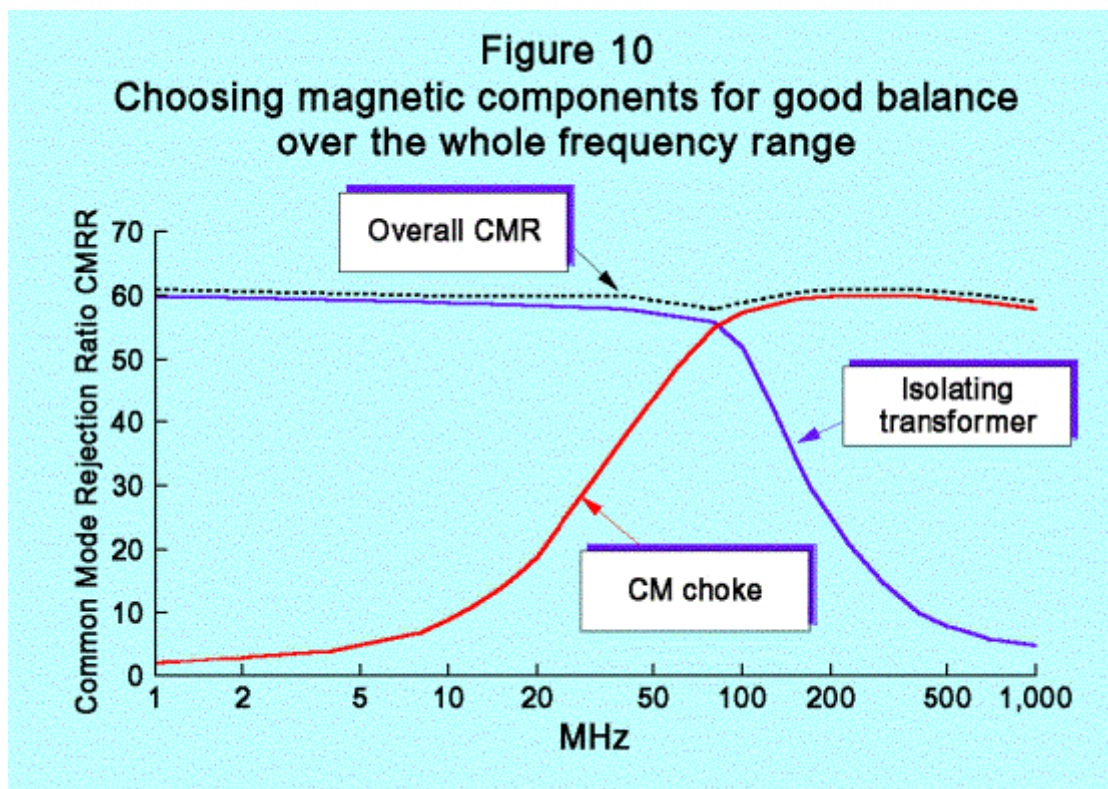
Transformer isolation, balanced drive and receive, and CM chokes, all help to get the best EMC performance from a cable.

Figure 9 shows two examples, both equally applicable to providing good emissions and immunity for digital or analogue signalling (communications) of any speed or frequency range.



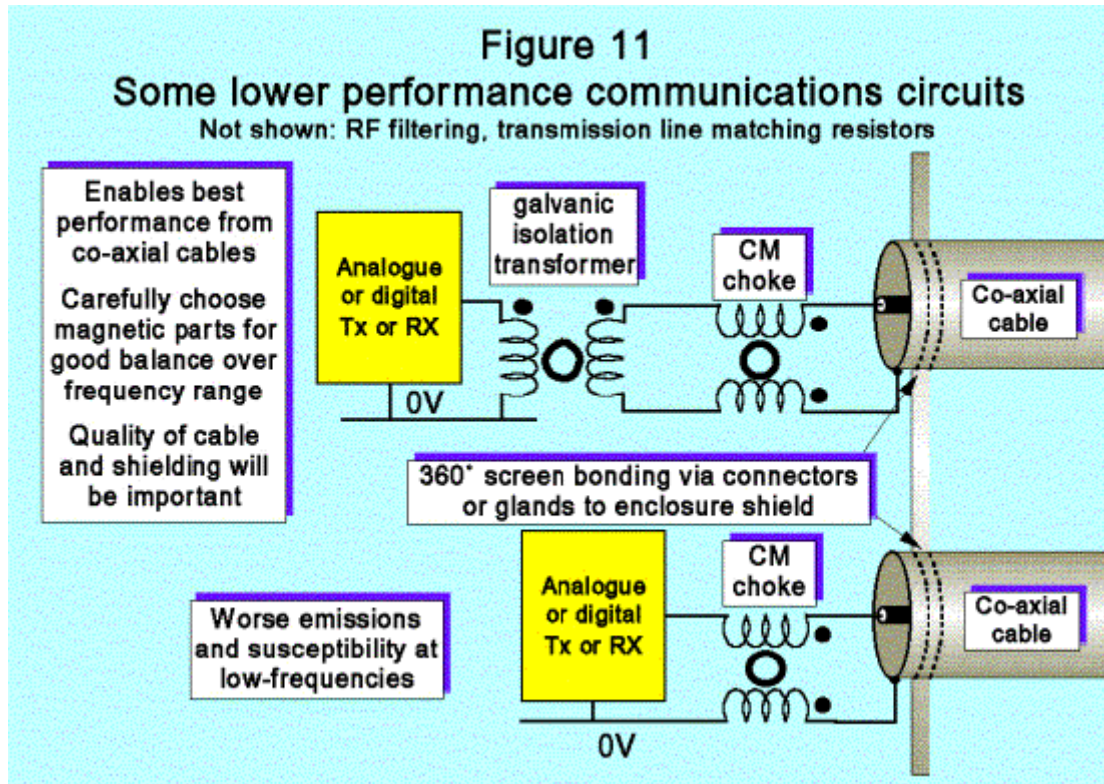
These circuits are ideal, in that a balanced send or receive circuit (in one case from a transformer, in the other an IC with balanced output or input) is connected to a balanced communications medium (the twin-axial or twisted-pair cable) via a CM choke.

Figure 10 shows how the CMRR of the choke is tailored to suit the transformer to give good balance over the whole frequency range, for a high-speed data example such as Ethernet. A similar design technique is used for the balanced IC.



For a professional audio communication link the signal frequencies extend to 20Hz or less, so the isolating transformer will be large. Its large interwinding capacitance rolls its CMRR off to zero before 1MHz, so the CM choke then needs to be larger to provide CMRR down to 100 kHz or less. It is difficult to find a choke that has good CMRR from 100kHz to 1,000 MHz, so two chokes with different specifications may be needed in series to cover the range.

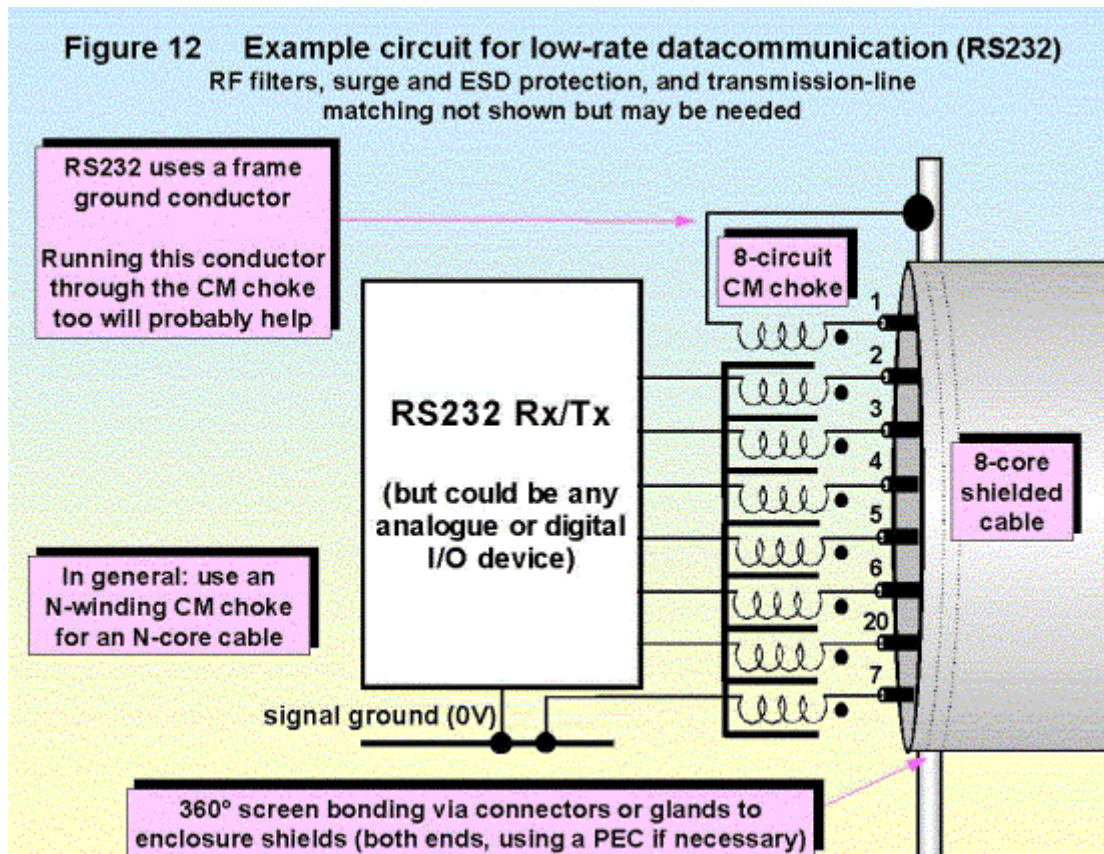
Where co-axial cables are used instead of twisted-pairs or twin-ax, EMC and signal integrity will suffer and the techniques shown in Figure 11 will help to achieve the best possible performance from the cables used.



The circuit without the isolation transformer will generally suffer from poorer immunity at lower frequencies.

Many communications are still low frequency or low rate, and their signals are not particularly prone to causing emissions or suffering from interference. E.g. analogue to/from 8-bit converters will not be as sensitive as that from 12-bit converters, whereas 16 and higher number of bits will be very sensitive indeed.

Such signals are often sent down single wires in multiconductor cables to save cost, as shown by Figure 12 (an example of an RS232 application).



Where a conductor has N cores, it is best to connect it to the electronics at each end with a CM choke with N windings. Figure 12 shows a seven winding choke used for an eight-core cable, because one of the conductors is dedicated to “frame ground” according to the RS232 standard. (The frame ground lead is not likely to carry heavy currents and require a PEC because RS232 is only used for short-distances.)

RS232 only suits short distances because its single-ended signals lose their integrity rapidly as they radiate their energy as emissions. So although figure 12 (and the bottom circuit in figure 11) looks easy enough, the use of single-ended signals will require attention to CM choke and/or cable and/or connector quality. (Cable and connector types and qualities are discussed in the 2nd part of this series.)

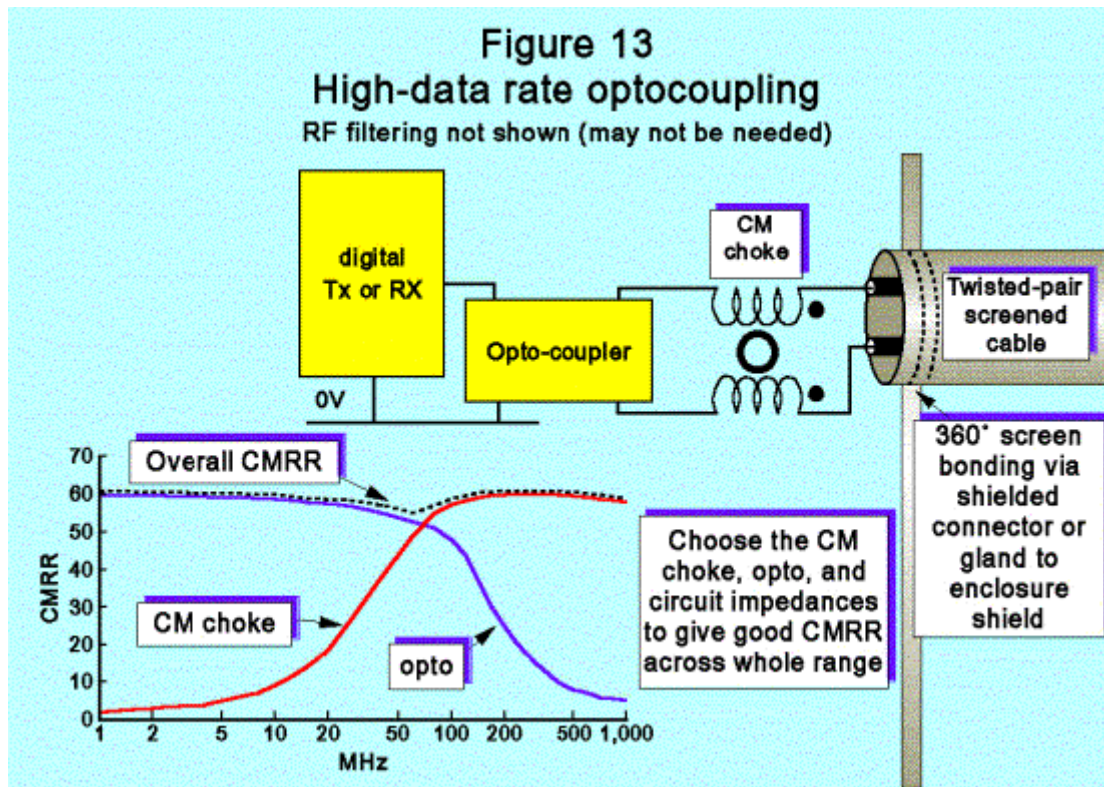
Using drivers with very slow output edges (preferably slew-rate limited) can ease emissions problems significantly. Alternatively, standard drivers can be passively filtered to reduce their high-frequency content.

1.4.3 Opto-isolation

Opto-isolation is a common technique for digital signals, but the input-output capacitance of typical opto-coupler is around 1 pF – this creates a low enough impedance at frequencies above 10MHz to interact with the circuit impedances and destroy the balance of the signals in the cable.

As before, the selection of a suitable common-mode choke will restore the balance at high frequencies, allowing fast-edged signals to be communicated with fewer emissions or immunity problems.

Figure 13 shows an example of good EMC practices in a high-speed optically isolated link.



Similar to the previous examples, the CMRR of the CM choke is chosen to compensate for the fall-off in the balance of the opto-isolator at high frequencies, so that a good balance (equal to a good CMRR) is maintained across the full frequency range (DC to 1GHz in this example).

In many cases the CM choke can be replaced by two individual ferrite beads, and sometimes no choke or ferrites at all prove to be necessary.

But if they are not placed and routed on the PCB Murphy's Law predicts that they *will* be needed, and furthermore it is likely that there will be no room for them, no doubt making a wholesale redesign of the product necessary, including its plastic enclosure.

If the cable needs to be shielded, it must be 360° bonding via a shielded connector or gland to enclosure shield at both ends, using a PEC if necessary (see IEC 61000-5-2). But where galvanic isolation is needed bonding the shield at both ends may be forbidden. In this case a capacitive bond at one end may be used (the capacitor rated for the full voltage, and probably safety-approved too) - or the shield left unterminated at one end, which is liable to have poor EMC performance.

Analogue signals can now benefit also from opto-isolation with up to 0.1% linearity (e.g. using IL300 and the like). This can save having to use voltage-frequency converters (and vice-versa) in many opto-coupled applications.

Because of the common drawing practice of not showing power rails in full, it sometimes happens that both sides of an opto-isolator are powered from the same DC power rails, seriously compromising the isolation achieved and the RF performance. The RF performance of opto-isolators can only be as good as the RF isolation between their power supplies.

1.4.4 External I/O protection

External I/O is exposed to the full range of electromagnetic phenomena. The better circuits in the above figures should need less filtering or protection, for a given signal and semiconductors.

All the above communication circuits may need additional filtering for emissions or immunity with continuous EMC phenomena.

For ESD, transient, and surge phenomena the upper circuits of figures 9 and 11, and figure 13, are well-protected – providing their isolating transformers or opto-couplers will withstand the voltage stresses applied. RF filtering can also give some protection against ESD or fast transients.

The above circuits without isolating transformers or opto-couplers will almost certainly need overvoltage protection with diodes or transient suppressors, although heavy filtering might be adequate if data rates or frequencies are very low. For control signals a series 10k or 100k resistor closest to the connector followed by a 100 nF or 10 nF capacitor to the PCB ground plane makes a marvellous barrier against almost all EMC phenomena, but does not allow rapid changes in logic state.

Digital communications generally need a robust digital protocol (see below) to prevent data corruption, as protection devices only prevent actual damage to the semiconductors.

Allow for additional protection devices on a prototype board, and test it as early as possible to see which are needed.

1.4.5 “Earth – free” and “floating” communications

Another name for galvanic isolation is “earth free” or “floating”, but these terms are often misunderstood or misused.

The above circuits using isolating transformers or opto-couplers are all “earth-free” and “floating”, because no currents from the communications devices are assumed to flow between Tx and Rx via the 0V or chassis. This is true even though their cable screens are bonded at *both* ends to local chassis (enclosure shield). In fact, leakage currents flow through parasitic capacitances, and when CMRR is poor they can reach surprisingly large values.

The terms “earth-free” and “floating” are also sometimes applied to electronically balanced inputs or outputs, such as the lower circuit of figure 9. Although good CMRR performance will still give low leakage via 0V or chassis, such circuits are not galvanically isolated and are intrinsically more vulnerable to surges. Electronically balanced circuits also have a reputation for suffering from instability when one of the two lines is accidentally connected to ground.

Don't forget that the quality of the isolation achieved in practice is limited by the isolation performance of the power supplies supplying each side.

Never try to achieve “earth-free” operation by removing the protective earth from any equipment – this creates serious safety hazards and immediately contravenes several mandatory laws. If “ground loops” are a problem, use the proper circuit and installation techniques (e.g. PECs) and never compromise safety.

It is best to avoid jargon phrases like “earth-free” and “floating”, instead state what is actually required or meant in plain circuit terms.

When screens *cannot* be connected at both ends

In some applications it is mandatory not to connect equipment grounds via cable screens or other conductors. The equipment concerned is still connected to main supply system's earth, but the earthing system is controlled in a special way. This does *not* help to achieve EMC at low cost. A screen connection at only one end will make the balance of the circuit and its conductors more important, and it will be more difficult and expensive to achieve a given EMC performance for a given signal.

Attention to creepage and clearances will also be important for safety reasons. In larger installations: when screens are not bonded at both ends, surges can cause arcing at the unconnected end possibly causing fire or toxic fumes. People can also receive shocks if they happen to be touching the screen and other equipment when a surge arrives. Clearly, not connecting the screens at both ends must place extra electrical and EMC stresses on some of the circuit components and cables, making surge, transient, and ESD damage more likely.

1.4.6 Hazardous area and intrinsically safe communications

Special barrier devices to limit the maximum power available in normal and fault conditions, and other restrictions, may be required. The EMC performance of these devices, which are made by specialist companies, is crucial. Further discussion is beyond the scope of this series.

1.4.7 Communication protocols

The data protocols used for digital communications are vital for both emissions and immunity, and it is much better to purchase chips that implement proven protocols than to try to develop them yourself. Simple protocols are easy, but they are very poor for EMC. Chips implementing CAN, MIL-STD-1553, LONWORKS, etc, have hundreds of man-years experience with interference control built into them, which no normal project team can ever hope to equal. Spend the extra few dollars on robust protocols, it will be worth it. Protocols are not discussed further in this series.

1.5 Choosing passive components

All passive components contain parasitic resistance, capacitance, and inductance. At the high frequencies at which many EMC problems occur these parasitic elements often dominate, making the components behave completely differently. E.g.: at high frequencies a film resistor becomes either a capacitor (due to its shunt C of around 0.2pF) or an inductor (due to its lead inductance and spiral tolerancing). These two can even resonate to give even more complex behaviour. Wire-wound resistors are useless above a few kHz, whereas film resistors under 1k usually remain resistive up to a few hundred MHz. A capacitor will resonate due to the effect of its internal and lead inductances, and above its first resonance it will have a predominantly inductive impedance.

Surface mounted components are preferred for good EMC because their parasitic elements are much lower and they provide their nominal value up to a much higher frequency. E.g. SMD resistors under 1k are usually still resistive at 1,000 MHz.

All components are also limited by their power handling capacity (especially for surges handling), dV/dt capacity (solid tantalum capacitors go short-circuit if their dV/dt is exceeded), dI/dt, etc. Passive components can also suffer severe temperature coefficients, or need de-rating. SMD parts have lower power ratings than leaded, but since most power occurs at lower frequencies it is often possible to use leaded parts in those areas, although taking care to minimise lead length.

For capacitors, ceramic dielectrics usually give the best high frequency performance, so SMD ceramics are often excellent. Some ceramic dielectrics have strong temperature or voltage coefficients, but COG or NPO dielectric materials have no tempco or voltco to speak of and make very stable and rugged high-quality high-frequency capacitors. They tend to be larger and cost more than other types, for values above 1nF.

Magnetic parts should have closed magnetic circuits, as has been described above. This is important for immunity as well as for emissions. Rod-cored chokes or inductors must be used with great care, if they cannot be avoided altogether (what shape is the ferrite antenna of a radio receiver?). Even the mains transformers used in linear power supplies can give better EMC performance if they have an interwinding screen connected to protective earth.

All these imperfections in passive components makes filter design very much more complicated than the circuits in textbooks and on simulator screens might suggest. Where a passive component is to be used with high frequencies (e.g. to decouple interfering currents up to 1,000MHz to a ground plane) it helps to know all about its parasitic elements and to do a few simple sums to work out their effects. Helpful manufacturers of quality components publish parasitic data, even sometimes impedance performance over a broad range of frequencies (often revealing their self-resonances).

Some passive components will need to be rated for safety, especially *all* those connected to hazardous voltages, of which the AC supply is often the worst case. It is best to only use parts here which have been approved to the correct safety standard(s) at the correct ratings by an accredited third-party laboratory and allowed to carry their distinguishing mark (SEMKO, DEMKO, VDE, UL, CSA, etc.). But the presence of the mark on the component means nothing. Much better is to get a copy of all the test labs' certificates for the safety approved parts and check they cover all they should.

The use of components with unknown parasitics for high-speed signals and/or EMC purposes makes it more likely that the number of product design iterations will be high and time-to-market delayed.

1.6 References:

- [1] Tim Williams, *EMC for Product Designers* 3rd edition, Newnes 2001, ISBN: 0-7506-4930-5, www.newnespress.com
- [2] IEC 61000-5-2:1997 Electromagnetic Compatibility (EMC) – Part 5: Installation and mitigation guidelines – Section 2: Earthing and cabling, www.iec.ch.
- [3] Tim Williams and Keith Armstrong, *EMC for Systems and Installations*, Newnes 2000, ISBN 0 7506 4167 3 www.newnespress.com, RS Components Part No. 377-6463.
- [4] Keith Armstrong, *EMC for Systems and Installations Part 2 – EMC techniques for installations*, EMC+Compliance Journal, April 2000, pp8 – 17. All UK EMC Journal and EMC+Compliance Journal articles are available electronically from the magazine archive at www.compliance-club.com .

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该套装是迄今国内最全面、最权威的 ADS 培训教程,共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解,并多结合设计实例,由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS,迅速提升个人技术能力,把 ADS 真正应用到实际研发工作中去,成为 ADS 设计专家...



课程网址: <http://www.edatop.com/peixun/ads/13.html>



HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程,是迄今国内最全面、最专业的 HFSS 培训教程套装,可以帮助您从零开始,全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装,更可超值赠送 3 个月免费学习答疑,随时解答您学习过程中遇到的棘手问题,让您的 HFSS 学习更加轻松顺畅...

课程网址: <http://www.edatop.com/peixun/hfss/11.html>

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出,是最全面、系统、专业的 CST 微波工作室培训课程套装,所有课程都由经验丰富的专家授课,视频教学,可以帮助您从零开始,全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装,还可超值赠送 3 个月免费学习答疑...

课程网址: <http://www.edatop.com/peixun/cst/24.html>



HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书,课程从基础讲起,内容由浅入深,理论介绍和实际操作讲解相结合,全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程,可以帮助您快速学习掌握如何使用 HFSS 设计天线,让天线设计不再难...

课程网址: <http://www.edatop.com/peixun/hfss/122.html>

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程,培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合,全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作,同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习,可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试...

详情浏览: <http://www.edatop.com/peixun/antenna/116.html>



我们的课程优势:

- ※ 成立于 2004 年,10 多年丰富的行业经验,
- ※ 一直致力并专注于微波射频和天线设计工程师的培养,更了解该行业对人才的要求
- ※ 经验丰富的一线资深工程师讲授,结合实际工程案例,直观、实用、易学

联系我们:

- ※ 易迪拓培训官网: <http://www.edatop.com>
- ※ 微波 EDA 网: <http://www.mweda.com>
- ※ 官方淘宝店: <http://shop36920890.taobao.com>