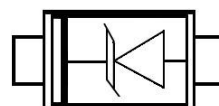


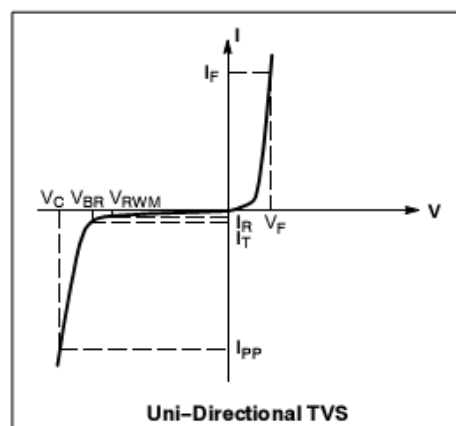
Description

The PESDNC9D5VU ESD protector is designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, lower operating voltage, lower clamping voltage and no device degradation when compared to MLVs. The PESDNC9D5VU protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. The PESDNC9D5VU is available in a SOD-923 package with working voltages of 5 volt. It gives designer the flexibility to protect one unidirectional line in applications where arrays are not practical. Additionally, it may be "sprinkled" around the board in applications where board space is at a premium. It may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge)



Feature

- 100 Watts peak pulse power ($t_p = 8/20 \mu\text{s}$)
- Transient protection for data lines to
 - IEC 61000-4-2 (ESD) $\pm 25\text{kV}$ (air), $\pm 10\text{kV}$ (contact)
 - IEC 61000-4-4 (EFT) 40A (5/50ns)
 - IEC 61000-4-5 (Lightning) 24A (8/20 μs)
- Small package for use in portable electronics
- Suitable replacement for MLVs in ESD protection applications
- Protect one I/O or power line
- Low clamping voltage
- Stand off voltages: 5V
- Low leakage current
- Solid-state silicon-avalanche technology
- Small Body Outline Dimensions: $0.8\text{mm} \times 0.6\text{mm} \times 0.5\text{mm}$
- Equivalent to 0402 package



Applications

- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDA's)
- Notebooks, Desktops, and Servers
- Portable Instrumentation
- Cordless Phones
- Digital Cameras
- Peripherals
- MP3 Players

Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Working Voltage	V_{RWM}				5	V
Breakdown Voltage	V_{BR}	$I_t = 1\text{mA}$	6	6.8	7.2	V
Reverse Leakage Current	I_R	$V_{RWM} = 5\text{V}$		0.005	1	μA
Forward Voltage	V_F	$I_F = 10\text{mA}$		0.8		V
Clamping Voltage	V_C	$I_{PP} = 1\text{A}$ $t_P = 8/20\mu\text{S}$			9.0	V
Clamping Voltage	V_C	$I_{PP} = 5\text{A}$ $t_P = 8/20\mu\text{S}$			11.0	V
Junction Capacitance	C_j	$V_R = 0\text{V}$ $f = 1\text{MHz}$		30	40	pF
Junction Capacitance	C_j	$V_R = 2.5\text{V}$ $f = 1\text{MHz}$		22	30	pF

Absolute maximum rating@25°C

Rating	Symbol	Value	Units
Peak Pulse Power ($t_P = 8/20\mu\text{S}$)	P_{pp}	100	W
Lead Soldering Temperature	T_L	260 (10 sec)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Applications Information

➤ Device Connection Options

- PESDNC9D5VU is designed to protect one data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode dot should be placed towards the line that is to be protected.

➤ Circuit Board Layout Recommendations for Suppression of ESD.

- Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:
- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible, for multilayer printed-circuit boards, use ground vias.
- Keep parallel signal paths to a minimum.
- Avoid running protection conductors in parallel with unprotected conductor.
- Minimize all printed-circuit board conductive loops including power and ground loops.
- Avoid using shared transient return paths to a common ground point.

Typical Characteristics

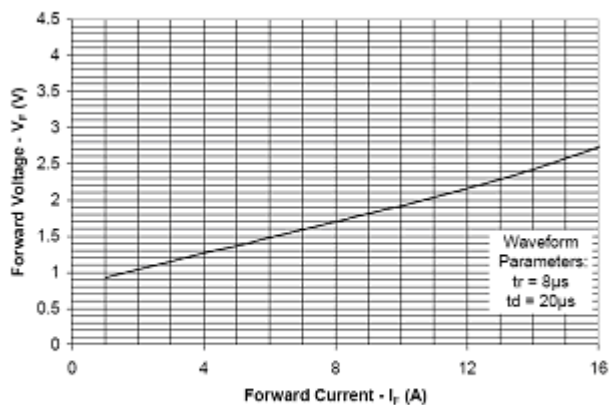


Figure 1 .
Forward Voltage vs. Forward Current

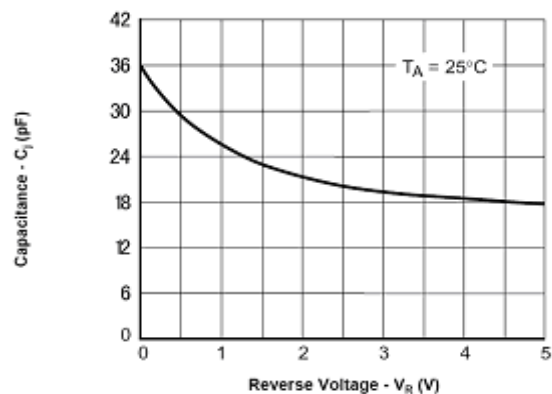


Figure 2.
Junction Capacitance vs. Reverse Voltage

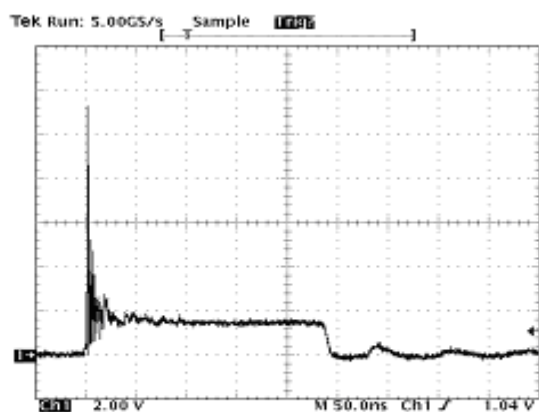
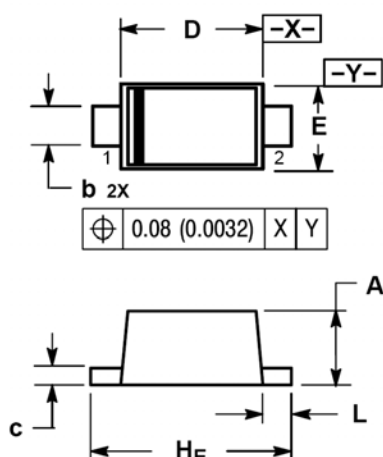


Figure 3. ESD Clamping
(8kV Contact per IEC 61000-4-2)

Product dimension



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.36	0.40	0.43	0.014	0.016	0.017
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
H _E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

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