Board Design Guidelines for LVDS Systems

This white paper explains the basic PCB layout guidelines for designing low-voltage differential signaling (LVDS) boards using Altera® FPGAs.

Introduction

LVDS is a high-speed, low-voltage, low-power, and low-noise general-purpose I/O interface standard. The low-voltage swing and differential current mode outputs significantly reduce electromagnetic interference (EMI). These outputs have fast edge rates that cause signal paths to act as transmission lines. Therefore, ultra-high-speed board design and differential signal theory knowledge is especially useful for designing a board containing Altera FPGAs that integrate LVDS. In addition, a number of factors, such as differential traces, impedance matching, crosstalk, and EMI, have to be considered while designing an LVDS board.

Differential Traces

LVDS utilizes a differential transmission scheme, which means that every LVDS signal uses two lines. The voltage difference between these two lines defines the value of the LVDS signal. For successful transmission of LVDS signals over differential traces, the following guidelines should be followed while laying out the board.

- To ensure minimal reflections and maintain the receiver's common mode noise rejection, run the differential traces as closely as possible after they leave the driving IC. Also, to avoid discontinuities in the differential impedance, the distance between the differential LVDS signals should remain constant over the entire length of the traces.
- To minimize skew, the electrical lengths between the differential LVDS traces should be the same. Arrival of one of the signals before the other creates a phase difference between the signal pair, which impairs the system performance by reducing the available receiver skew margin (RSKM).
- Minimize the number of vias or other discontinuities on the signal path.
- Any parasitic loading, such as capacitance, must be present in equal amounts to each line of the differential pair.
- To avoid signal discontinuities, arcs or 45° traces are recommended instead of 90° turns.

Impedance Matching

Due to the high speed of LVDS, impedance matching is very important, even for very short runs. Any discontinuities in the differential LVDS traces will cause signal reflections, thereby degrading the signal quality. These discontinuities also increase the common mode noise and will be radiated as EMI. The LVDS outputs, being current mode outputs, need a termination resistor to close the loop and will not work without the resistor termination. The value of this

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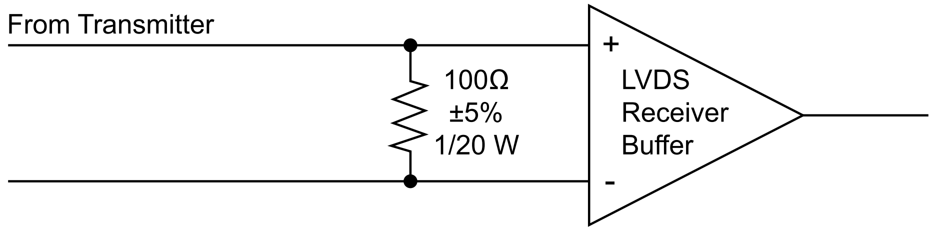
termination resistor (RT) is chosen to match the differential impedance of the transmission line and can range from 90Ω to 110Ω (typically 100Ω). Figure 1 shows the correct usage of the termination resistor.

Figure 1. LVDS Termination Scheme



The following guidelines should be used when selecting the termination resistor for an LVDS channel.

- Place the termination resistor at the far end of the differential interconnect from the transmitter. A single 100Ω resistor is sufficient.
- Use surface-mount thick-film 0603- or 0805-size chip resistors.
- Install the termination resistor within 7 mm of the receiver, as close to the receiver as possible.

Crosstalk Between LVDS and Single-Ended Signals

To reduce crosstalk between LVDS and single-ended signals such as LVTTL, SSTL-3, SSTL-2, and similar standards, the differential LVDS signals must be isolated from single-ended signals. If the LVDS and single-ended signals are not placed sufficiently apart from one another, the single-ended signals may cause some interference on the differential pair. The LVDS signal that runs closest to the single-ended signal trace will be affected more than the farther one, creating a difference that will not be rejected by the LVDS receiver as common mode noise. This interference is unlikely to cause the LVDS receiver to falsely trigger; however, it will degrade the signal quality of the LVDS signal, thereby reducing the noise margin. On the same PCB layer, the single-ended signals should be placed at least 12 mm from the LVDS signals to avoid crosstalk effects. The VCC and ground planes can also be used to isolate the LVDS signal layers from the single-ended signal layers. Figure 2 shows the shielding of the LVDS layers from the single-ended layers using the power planes.

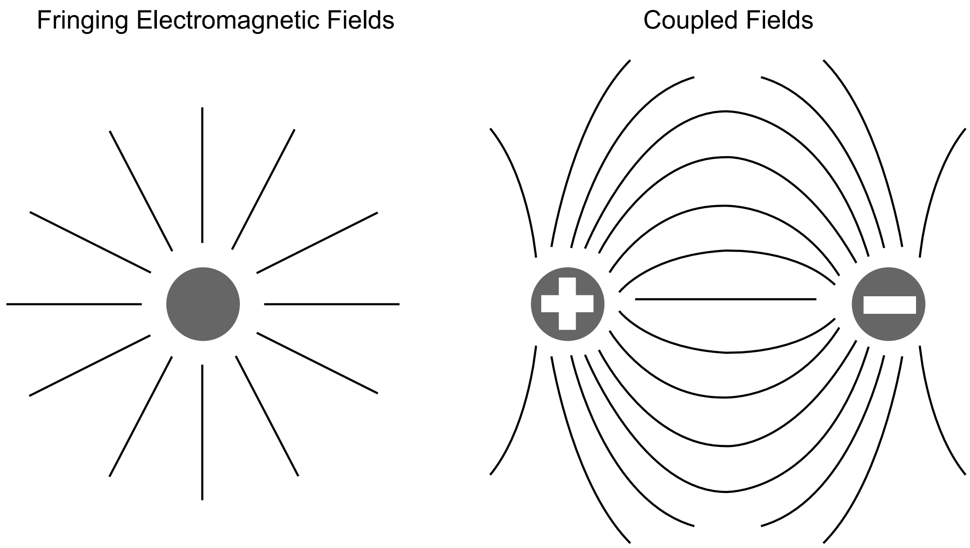
Figure 2. Power Planes

Electromagnetic Interference

Electromagnetic radiation is usually a cause for concern for designers because this radiation can propagate through transverse electromagnetic (TEM) waves. These waves can escape through shielding, causing a system to fail electromagnetic compliance (EMC) tests. With single-ended transmission such as CMOS or TTL, almost all of the field lines are free to radiate away from the conductor. Some of these field lines can travel as TEM waves, which may escape the system and thereby cause EMC problems.

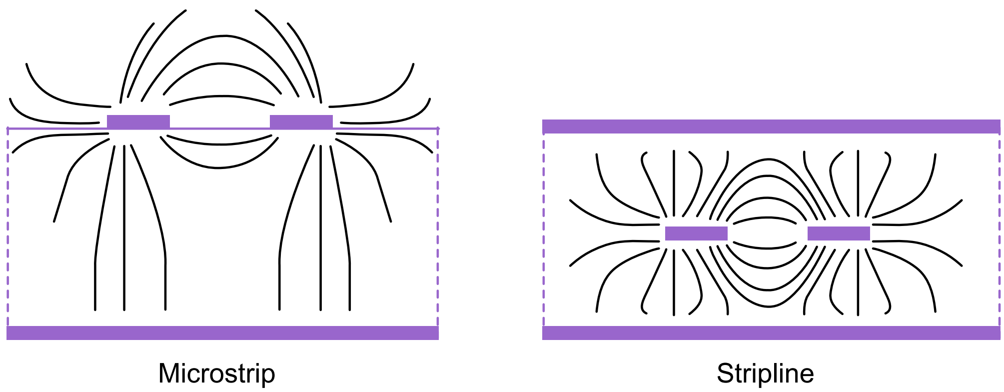
For LVDS differential signals, field lines tend to cancel each other out, and the electric fields tend to couple. These coupled fields are tied up with each other and thus are not allowed to escape. Only a few fringing fields escape out of this coupling. Therefore, LVDS, being a differential transmission system, generates less EMI compared to CMOS or TTL signals. Figure 3 shows the electromagnetic field effects in single-ended traces and differential pairs.

Figure 3. Electromagnetic Field Effects



LVDS signals can be routed on the PCB microstrip (external layers) and stripline (middle layers). Figure 4 shows the electromagnetic field radiation for LVDS stripline and microstrip traces.

Figure 4. Microstrip and Stripline Differential Pair Dimensions

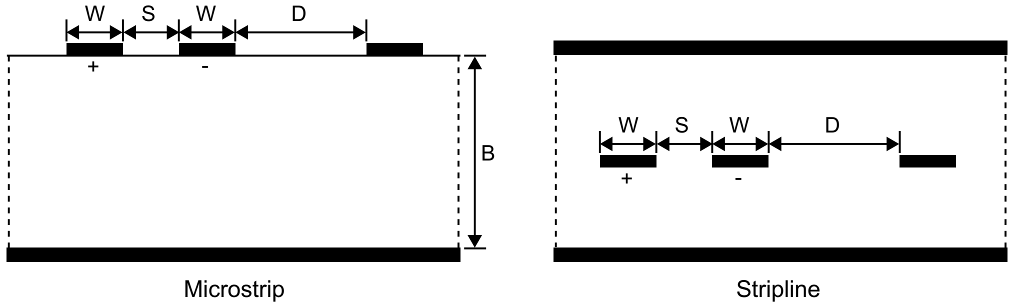


For microstrip, the ground plane below couples additional field lines, thereby tying up more field lines and reducing the EMI effects. Stripline couples all of the field lines, thereby reducing EMI significantly, but it also has the following penalties:

- Considerably higher (typically one and a half times) propagation times than that of microstrip
- Needs additional vias
- Needs more layers
- Difficulty in achieving 100Ω differential impedance accurately

In order to have maximum coupling of the magnetic field lines, the space between two conductors of a differential pair should be kept to a minimum. Figure 5 shows the dimensions of a stripline and microstrip pair.

Figure 5. Microstrip and Stripline Differential Pair Dimensions



For better coupling within a differential pair, make $S < 2W$, $S < B$, and $D = 2S$ where:

- W = width of a single trace in a differential pair
- S = space between two traces of a differential pair
- D = space between two adjacent differential pairs
- B = thickness of the board

For good coupling between two conductors of a differential pair, the following rules should be followed:

- Space between the conductors should not be more than twice the width ($S < 2W$)
- Thickness of the board should be more than the space between the conductors ($B > S$)
- Space between two adjacent differential pairs should be greater than or equal to twice the space between the two individual conductors. ($D > 2S$)

General PCB Guidelines

This section lists general PCB layout and supply voltage guidelines.

- The commonly used FR-4 material works well for low frequency (500 to 600 MHz) applications. G-TEK or Teflon can be considered for high-speed designs.
- Estimate the number, value, and type of decoupling capacitors required to develop an efficient PCB decoupling strategy during the early design phase, without going through extensive pre-layout simulations. Altera's Power Delivery Network (PDN) tool provides these critical pieces of information.

For further information about the PDN tool that targets your FPGA, refer to the Power Distribution Network Design Tool webpage.

- When using LVDS devices, all the `VCC_CKLK` and `VCC_CKOUT` pins should be bypassed with a 0.1-, 0.01-, and 0.001 µF mica, ceramic or polystyrene 0805-size surface-mount chip capacitors connected in parallel. These capacitors should be placed immediately underneath the pins. In addition to these capacitors, another 2.7 µF capacitor should be placed close to the pin.
- Keep the LVDS drivers and the receiver as close to any connectors as possible.
- The physical length of each trace between the transmitter outputs and the connector should be matched to within 5 mm of each other to reduce data skew.
- Isolate LVDS signals from TTL signals to reduce crosstalk (preferably on different layers).
- Separate LVDS ground and supply planes.
- Always use high-impedance, low-capacitance scope probes with a wide bandwidth scope.
- Keep stub lengths as short as possible.
- Multiple vias should be used to connect to power and ground planes.

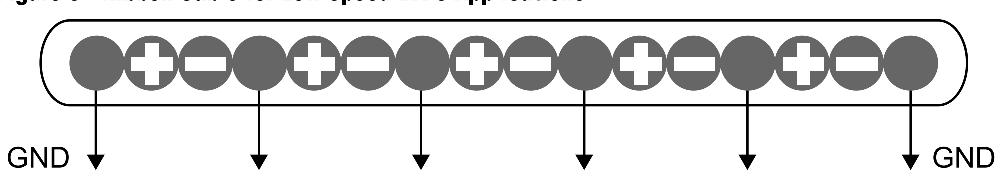
LVDS Cables

Cables can be used to transfer the LVDS signals from one board to another. However, due to the specific impedance matching and low skew requirements, typical cables may not be suitable for LVDS. Use the following guidelines to select cables for LVDS applications:

- The cables must fulfill the “matched impedance” requirement of LVDS.
- Cables should have very low skew.
- The conductor pairs must be balanced (i.e., both of the conductors should incur the same delay while going through the cable).

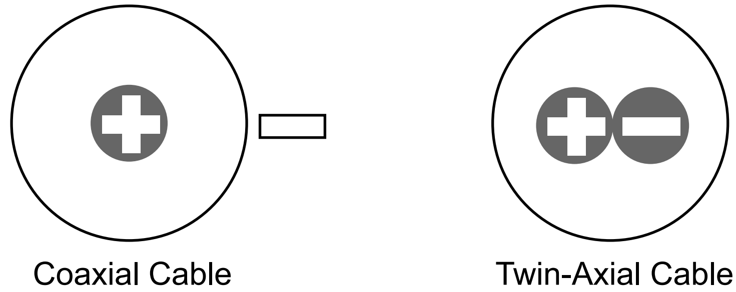
For low speed and very short runs, ribbon cables can be used. For longer runs and high speed, use twisted-pair cables (balanced twisted-pair cables work well in this application). If you use ribbon cables, the signal pairs must be separated by the ground wires, and the edge conductors of the ribbon cable should not be used to carry signals. Figure 6 shows a ribbon cable used for LVDS application.

Figure 6. Ribbon Cable for Low Speed LVDS Applications



Twin-axial cables can also be used for LVDS applications, as they are far more balanced then coaxial cables. In contrast to coaxial cables, twin-axial cables generate far less EMI due to the field cancellation effects. The coaxial and twin-axial cables are shown in Figure 7.

Figure 7. Coaxial and Twin-Axial Cables

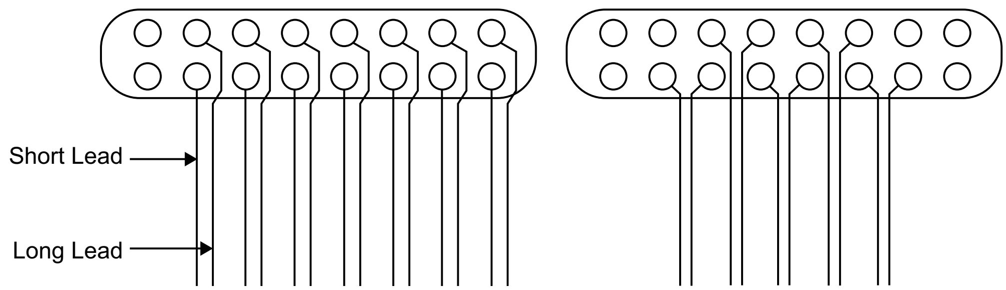


For optimum performance, use twisted-pair cables, because the LVDS receiver rejects whatever small common-mode electromagnetic radiation these cables pick up. For small distances (approximately 0.5 m), the CAT3 balanced twisted-pair cables work well. For distances greater than 0.5 m and data rates greater than 500 MHz, use CAT5 balanced cables.

LVDS Connectors

Connectors can be used to connect the LVDS signals from one board to another. Figure 8 shows good and bad examples of the LVDS connectors. In the right example, the differential pairs are the same length; in the left example, signals of the same differential pair have different lengths, thereby causing skew.

Figure 8. "Bad" (left) and "Good" (right) LVDS Connectors



Use the following guidelines while selecting connectors to be used for LVDS applications.

- Connectors must have low skew with matched impedance.
- Connectors with same length leads should be selected for lower skew and crosstalk.
- The two members of the same differential pair must be placed adjacent to each other on the connector.
- Ground pins should be placed between differential pairs.
- End pins of the connectors should preferably be grounded and must not be used for high-speed signals.
- All the unused pins of the connector should be properly terminated.

Summary

To benefit from the high speed and low noise of LVDS, designers must ensure that differential trace conductors, both on-board and going through connectors or cables, are closely coupled so as to have low noise and are well balanced for low skew and impedance matching.

Further Information

- Power Distribution Network Design Tool: www.altera.com/technology/signal/power-distribution-network/sgl-pdn.html

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
September 2010	2.1	■ Minor text edit to Impedance Matching.
July 2010	2.0	■ Updated General PCB Guidelines. ■ Removed LVDS in APEX Devices, Figure 6. ■ Minor text edits.
July 2000	1.0	Initial release.

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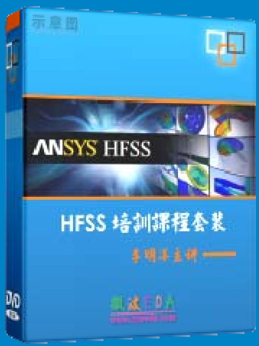

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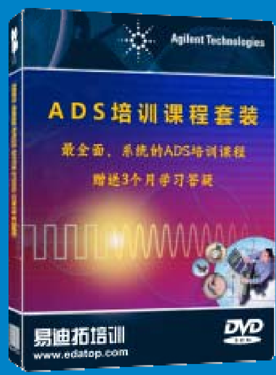

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