

PCB Design for EMI/EMC Compliance

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WEMPEC Seminar

21 July 2000

References

Unless noted otherwise, everything is from the 1st two references

- *PCB Design Techniques for EMC and Signal Integrity* Short Course, 27-29 June, UW-Madison, Mark Montrose, Instructor
- *Printed Circuit Board Design Techniques for EMC Compliance*, Mark Montrose, 1996 IEEE Press
- *Electronic Manufacturing*, Sheldon Kohen and Michael Rose, 1982 Reston Publishing Company
- *Linear Design Seminar*, Analog Devices, October 1987
- *Electronic Manufacturing Processes*, Thomas Landers, William Brown, Ernest Fant, Eric Malstrom and Neil Schmitt, 1994 Prentice Hall
- *Electronics Assembly Handbook*, Keith Brindly, 1990 Newnes

Presentation Overview

- Definitions
- PC Board Materials & Construction
- EMC Fundamentals
- EMI Suppression
- Signal Integrity
- Bypassing & Decoupling
- Trace Routing
- ESD Protection

Definitions

- *Printed Circuit Board (PCB)* Also known as a Printed Wire Board (PWB). A device used to mechanically hold components while providing electrical interconnection via a transmission line. It consists of one or more layers of an insulating material and one or more layers of a conductive foil.
- *land* The part of a PCB trace allocated for the connection to a component.
- *via* A hole in the PCB with conductive plating on the inside and which connects to one or more conductive layers.
- *Through-hole Technology (THT)* “Standard” leaded components which are mounted by inserting the leads into vias and then filling the vias and surrounding land/pad with solder.
- *Surface-mount Technology (SMT)* Leadless components which are soldered directly onto the lands located on the surface of the PCB.

- **Electromagnetic Compatibility (EMC)** The capability of electrical and electronic systems, equipment, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design levels of performance, without suffering or causing unacceptable degradation as a result of electromagnetic interference. (ANSI C64.14-1992)
- **Electromagnetic Interference (EMI)** The process where disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths.
 - **Radiated Emissions** The component of RF (roughly 10kHz to 100GHz) energy transmitted through a medium, usually free space (air), as an electromagnetic field.
 - **Conducted Emissions** The component of RF energy transmitted as a propagating wave generally through a wire or interconnect cable. LCI (Line conducted interference) refers to RF energy in the power cord.
- **Susceptibility** The measure of a device's ability to be disrupted or damaged by EMI exposure.

- *Immunity* The measure of a device's ability to withstand EMI exposure and still operating at a designated level.
 - *Electrostatic Discharge (ESD)* A transfer of electric charge between bodies of different electrostatic potential in proximity or through direct contact.
 - *Radiated Immunity* The ability to withstand electromagnetic energy which is propagated through free space.
 - *Conducted Immunity* The ability to withstand electromagnetic energy which enters through external cables and connections (power or signal).
- *Containment* Keeping RF energy inside of an enclosure by providing a metal shield or plastic housing with RF conductive paint. Similarly, external RF energy can be kept out.
- *Suppression* Design techniques which reduce or eliminate RF energy from entering or leaving without using a secondary method like a shield or metal chassis.

Board Materials and Construction

- The base material or core
- Copper Layers
- 2-Layer boards
- Multilayer boards
- Types of Traces
- Transmission Line Calculations

Core Materials

The most common material is a fiberglass resin called FR-4.

Material	ϵ'_r	CTE ppm/ oC	Loss Tangent (δ)	Cost per sq. ft.
FR-4 glass	4.1-4.8	+250	0.02-0.03	\$2.5
GTEK	3.5-4.3	+250	0.012	\$3.5
woven glass/ceramic loaded	3.38	+40	0.0027	\$9.50
PTFE/ceramic (Teflon)	2.94	0	0.0012	\$100.00

Copper Layers

The conductive layer of a PCB is usually a sheet of copper which has been etched to form the circuit traces. The copper sheet's nominal thickness is designated by the weight of 1 square foot of copper of the nominal thickness.

Copper Thicknesses*

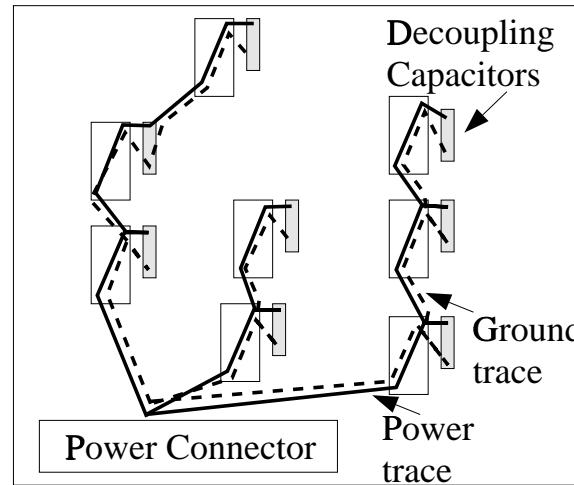
Weight (oz)	Thickness (in)	Weight (oz)	Thickness (in)
1/8	0.00017	4	0.0056
1/4	0.00035	5	0.0070
1/2	0.0007	6	0.0084
1	0.0014	7	0.0098
2	0.0028	10	0.0140
3	0.0042	14	0.0196

* *Electronic Manufacturing*



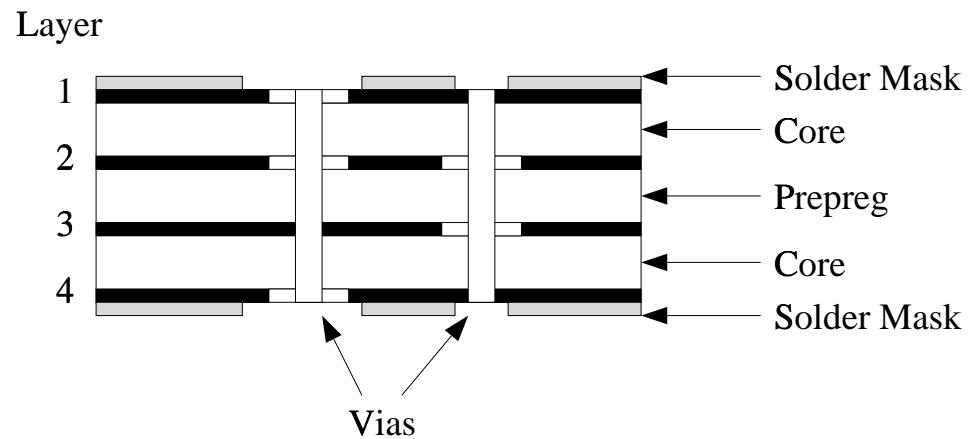
2-layer Boards

- Route power traces *radially* from the power supply
- Route power and ground traces parallel to each other
- Signal flow should parallel the ground paths.
- Don't create current loops by tieing different branches together.



Multilayer Boards

Multilayer boards are formed by etching several double-sided boards and then gluing them together with a material called *prepreg*. The thickness and material for both the core and the prepreg can be specified and controlled. *Vias* are holes which are electroplated after drilling and connect the different layers.



Types of Traces

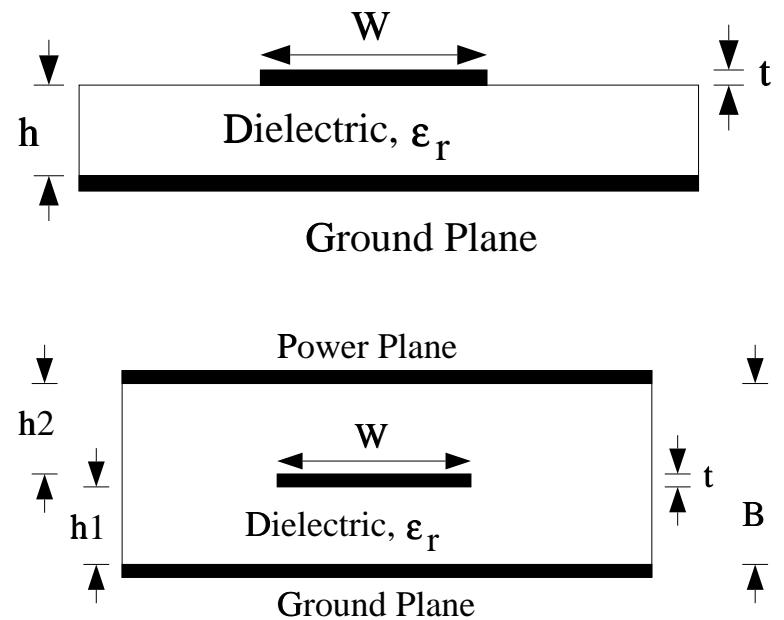
There are two basic types of trace topology: Microstrip and Stripline.

- Microstrip

Faster signals possible due to lower capacitive coupling, but greater radiated RF

- Stripline

Greatly reduced RF emissions, but slower signals



Impedance & Delay Calculations

- Microstrip[†]

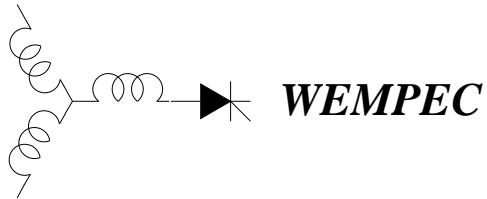
$$Z_0 = \left(\frac{87}{\sqrt{\epsilon_r' + 1.414}} \right) \ln \left(\frac{5.98h}{0.8W + t} \right)$$

$$t_{pd} = 85 \sqrt{0.475\epsilon_r' + 0.67} \quad (\text{ps/in})$$

$$C_0 = \frac{0.67(\epsilon_r' + 1.414)}{\ln \left(\frac{5.98h}{0.8W + t} \right)} \quad (\text{pF/in})$$

$$L_0 = Z_0^2 C_0 = 5071.23 \ln \left(\frac{5.98H}{0.8W + t} \right) \quad (\text{pH/in})$$

[†]see also *Lines and Electromagnetic Fields for Engineers* in the WEMPEC Library



- **Stripline[‡]**

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon'_r}} \right) \ln \left[\frac{4h}{0.67\pi W \left(0.8 + \frac{t}{W} \right)} \right]$$

$$t_{pd} = 85\sqrt{\epsilon'_r} \quad (\text{ps/in})$$

$$C_0 = \frac{1.41\epsilon'_r}{\ln \left(\frac{3.81h}{0.8W+t} \right)} \quad (\text{pF/in})$$

$$L_0 = Z_0^2 C_0 \quad (\text{pH/in})$$

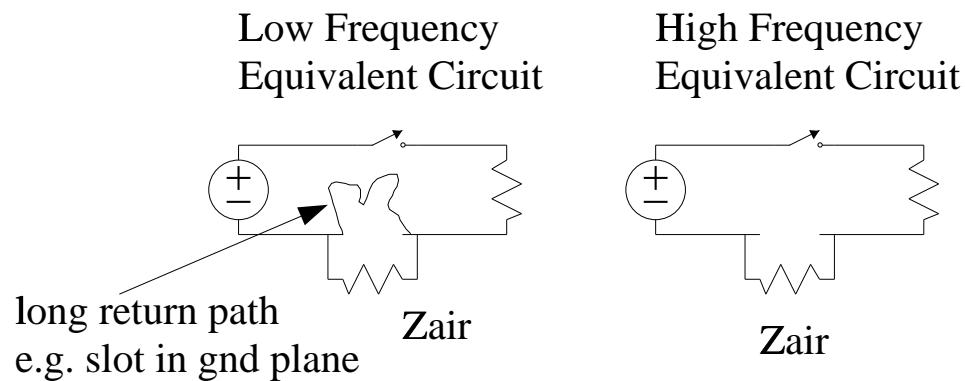
[‡]see also *Lines and Electromagnetic Fields for Engineers* in the WEMPEC Library

EMC Fundamentals

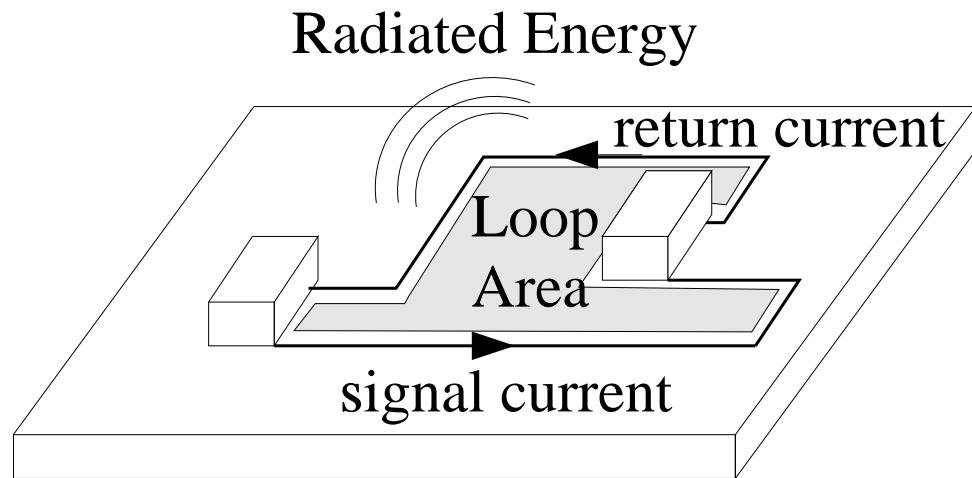
- The coupling path is frequency dependent
 - High frequencies are radiated
 - Low frequencies are conducted
 - The boundary is typically about 30 MHz
- There are 5 aspects to EMC when finding the problem
 - Frequency - Where in the spectrum is the problem observed?
 - Amplitude - How strong is the energy source?
 - Time - Is it continuous or intermittent with operation?
 - Impedance - What is the Z of the source and receiver?
 - Dimensions - What are the physical dimensions of the device which will allow emissions? (RF currents will leave through openings which are fractions of a wavelength!)

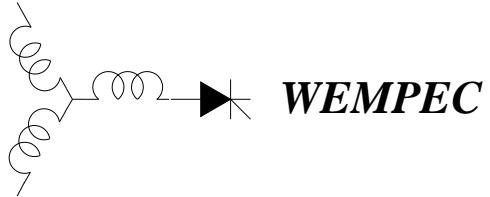
How PCB's Radiate RF Energy

- Digital signals with fast rise/fall times contain very high frequency components even for low clock frequencies! $F_{max} = \frac{1}{\pi t_r}$
- The RF currents from the switching choose the low impedance path
- The Z_0 of air is about 377Ω .
- Discontinuities in the RF return path $Z_{PCB}^{RF} \gg 377\Omega$
- RF current leaves the board in favor of the air = EMI



Radiated Emissions





EMI Suppression

- Image Planes
- The 20-H Rule
- System Level Grounding
- Partitioning

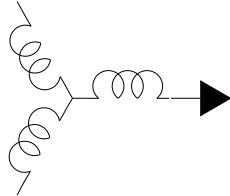


Image Planes

An image plane is a layer of copper (either a voltage or a ground plane) which physically adjacent to the signal routing plane. The image plane provides a low impedance path for the RF currents and reduces the EMI emissions since the RF currents use the plane instead of the air.

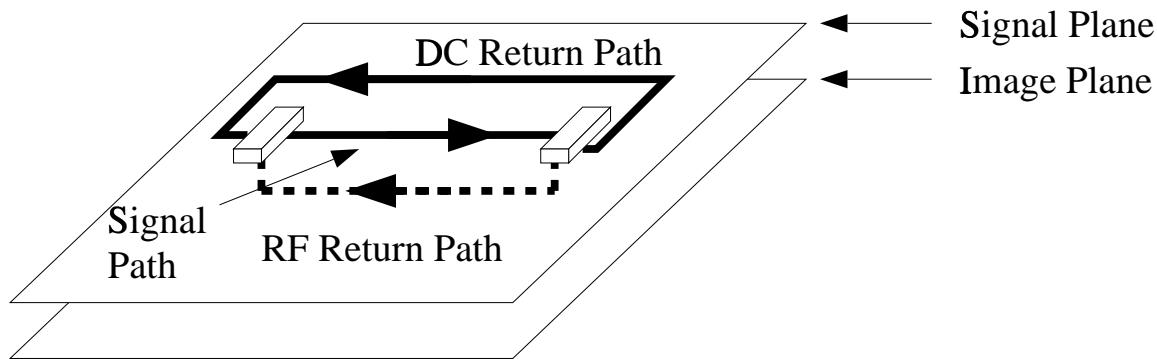
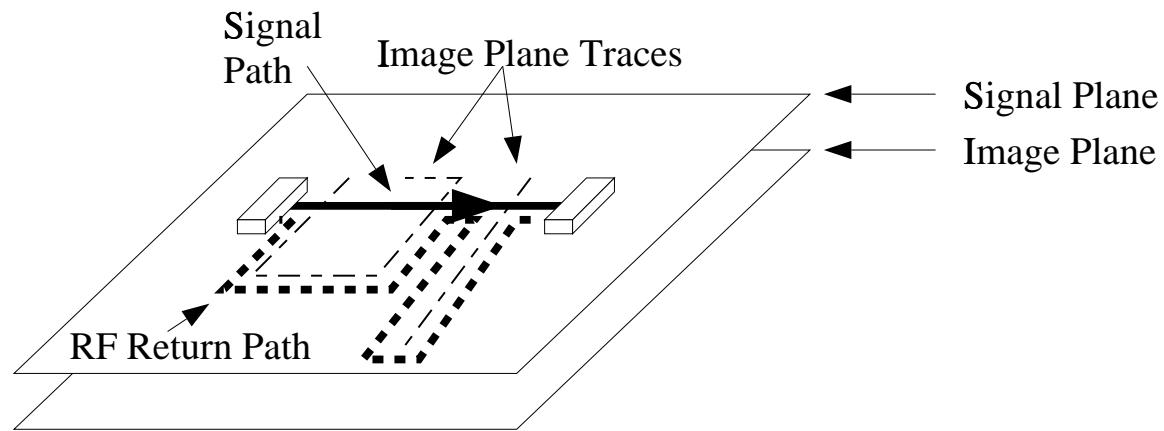




Image Plane Violations

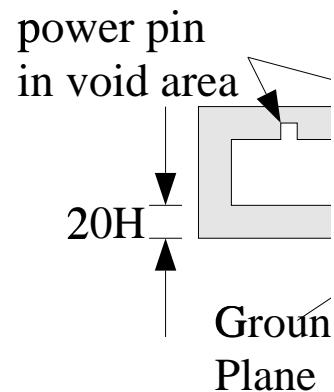
Routing traces in the image plane will create slots in the RF return path and create a large loop area and potential EMI!!



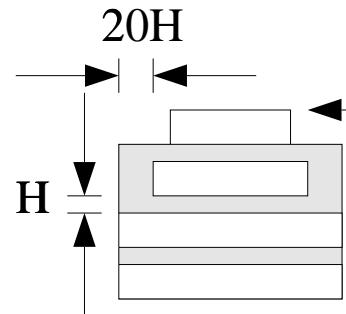
The 20-H Rule

- RF currents fringing between the power and ground planes at the edge of the board can result in RF emissions.
- Reducing the size of the power plane with respect to the ground plane will reduce these emissions.
- This increases the intrinsic self-resonant frequency of the PCB.
- The ground plane should exceed the power plane by $20 \cdot H$ where H is the total thickness between the power and ground planes
- 20-H provides for approximately a 70% reduction of the fringing flux and changing to 100-H will provide about a 98% reduction.

The 20-H Rule in Action



Board top view



Board side view

If a power pin needs to be located near the edge of the board, then it is ok for the plane to extend into the 20-H void to surround the pin.

System Level Grounding

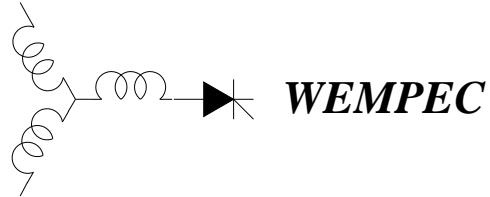
There are three main system grounding methods

- Single-Point Grounding
 - Either Series or Parallel
 - Best for frequencies below 1 MHz
 - Has the largest amount of ground loop currents
- Multi-point Grounding
 - Preferred for frequencies above 1 MHz.
 - Minimizes loop currents and ground impedance of planes.
 - Lead Lengths must be kept extremely short
 - Provides for maximum EMI suppression at the PCB level

- Hybrid
 - A mixture of both Single-Point and Multi-Point Grounding in the same system.
- Ground loops cause RF energy to be radiated when high inductance returns are provided.
- Note: Do not count on mounting screws to provide low inductance connections. They are highly inductive and can act as helical antennae at high frequencies (100 MHz-1 GHz)!! (Use conductive gaskets in addition to the screws.)
- In a Multi-point ground system, the distance between the screws should not exceed $\lambda/20$ of the highest edge rate on the PCB.

Partitioning

Partitioning consists of breaking a board up into functional areas with respect to the bandwidth of the functional block. Grounding connections are made around the perimeter of each functional block using spring finger, screws, gaskets, etc, provided that the method has a sufficiently low inductance between the ground plane and the chassis ground.



Signal Integrity

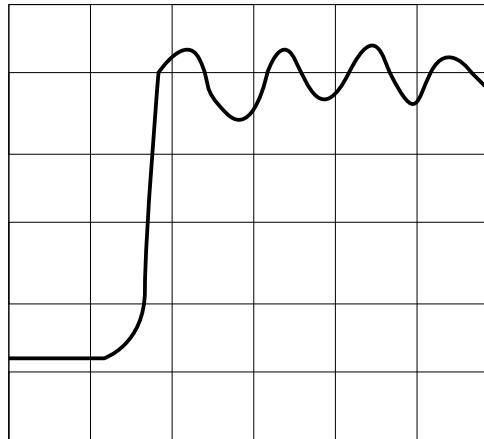
- Ringing and Reflection
- Cross-Talk
- Power and Ground Bounce

Ringing and Reflection

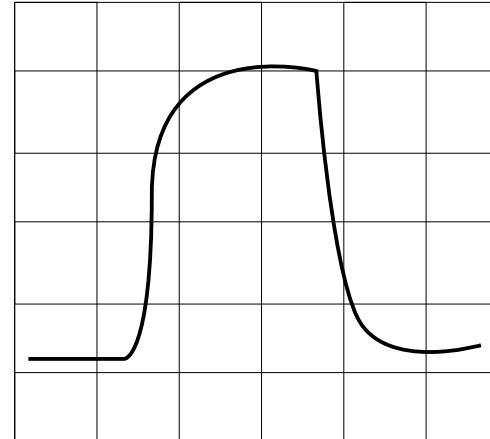
Transmission line properties which occur between the source and load. Possible causes:

- Changes in trace width
- Improperly matched termination networks
- Lack of terminations
- T-stubs, branched or bifurcated traces
- Varying loads and logic families
- Large power plane discontinuities
- Connectior transitions
- Changes in trace impedance

Signal Distortion



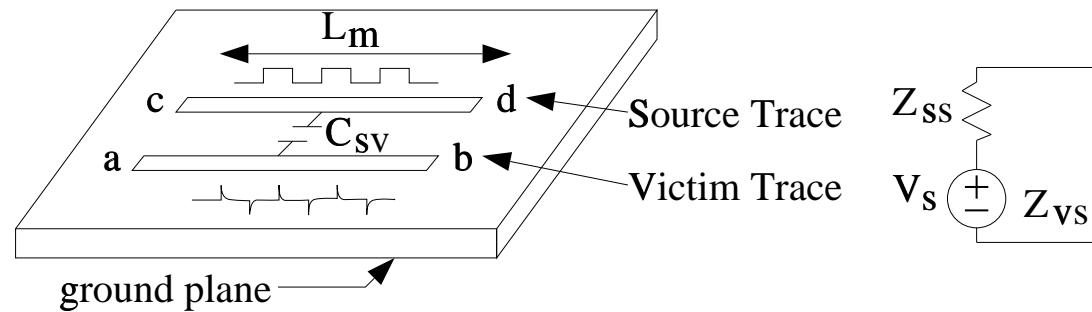
Ringing means reflections (due to excessive inductance)



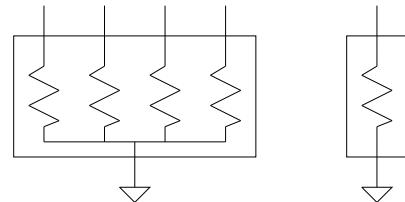
Rounding is due to excessive capacitance or trace resistance

- Ringing is minimized by proper terminations (e.g. series R)
- Rounding means the net is overdamped. Don't forget about the shunt capacitance of the trace as well as the load capacitance.

Cross-Talk (aka Board-level EMI!)



- cross-talk requires a 3-wire circuit!
- Terminating resistors with a common pin susceptible!



Preventing Cross-Talk

First, note the following observations:

- Decreasing the trace separation increases the mutual capacitance C_m and the cross-talk.
- With parallel traces, longer parallel lengths increase the mutual inductance L_m and the cross-talk.
- Decreasing the rise time of the signal, increases the cross-talk.

Some Solutions are:

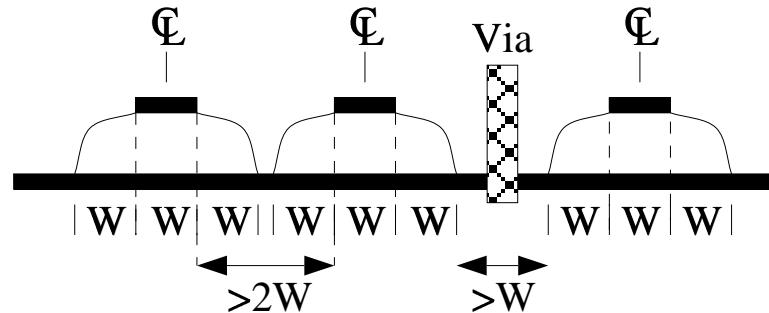
1. Group and locate logic devices according to functionality.
2. Minimize routed distance between components
3. Minimize parallel routed trace lengths

4. Locate components away from I/O interconnects and *other areas susceptible to data corruption*.
5. Provide proper terminations on impedance controlled traces or routed traces rich in harmonic energy
6. Avoid routing traces parallel to each other. Provide sufficient separation between traces to minimize inductive coupling (The 3 W Rule) or use *guard traces*.
7. Route adjacent signal layers orthogonal to reduce capacitive coupling between the layers.
8. Reduce signal-to-ground reference distance separation
9. Reduce trace impedance and/or signal drive level
10. Isolate signal layers which must be routed in the same axis with a solid planar structure.

The 3-W Rule[§]

This rule for trace separation will reduce the cross-talk flux by approximately 70%.
(For a 98% reduction, change the 3 to 10.)

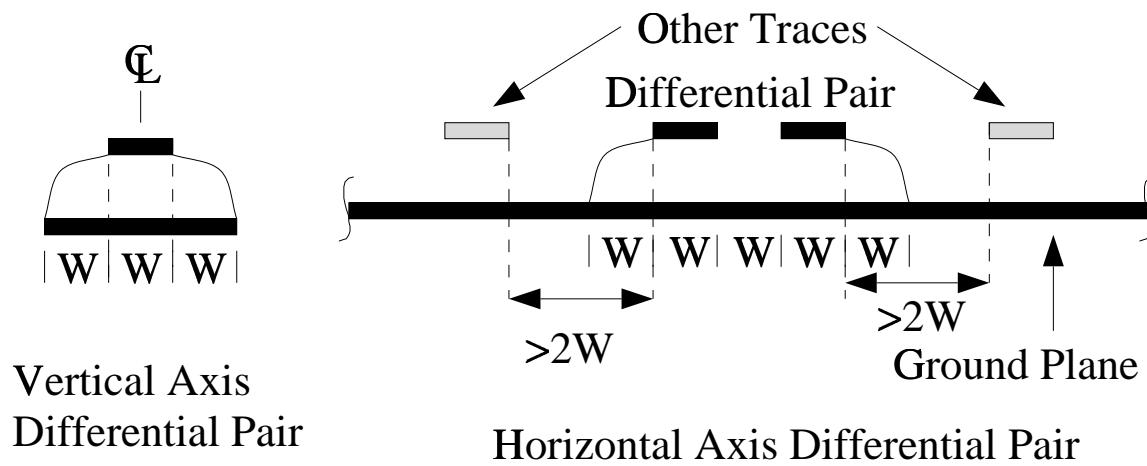
The distance of separation between traces must be three times the width of the traces, measured center-line to center-line.



Note that the traces near the edge of the plane need to be $> 1W$ from the edge!

[§]First described by W. Michael King

For Differential Pair Traces

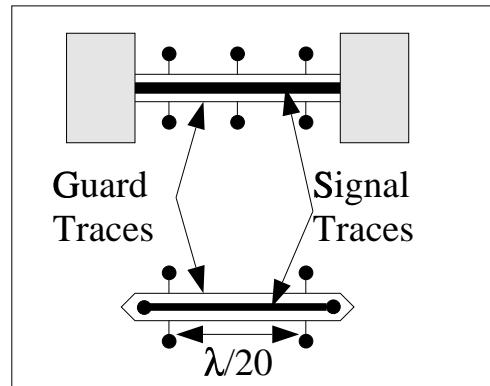


Guard/Shunt Traces

- Guard traces surround the high-threat traces (clocks, periodic signals, differential pairs, etc.) and are connected to the ground plane. *They are very useful in 2-layer boards.*
 - The guard trace should be *smallest, tolerable manufacturable spacing* from the signal.
 - The guard trace is connected to ground.
 - If a ground plane is available, make ground connections no farther than $\lambda/20$ apart.
- Shunt traces are traces located immediately above a high-threat trace and follow the trace along the entire route. They are best used in multi-layer (6 or more) boards.

$$\lambda = \frac{1}{10f_{max}}$$

Guard & Shunt Trace Examples

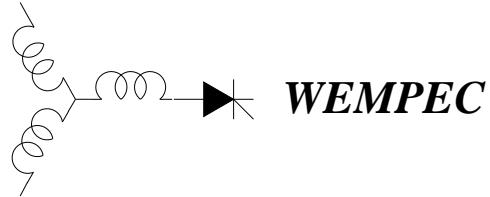


Guard Trace

Shunt Trace

Power and Ground Bounce

- Ground bounce is caused by the simultaneous switching of drivers in an IC package and may cause functionality as well as EMI concerns. Ground bounce presents a situation where the ground reference system is not at a constant 0 V reference value.
- Be sure to provide a separate ground connection for each ground pin directly to the ground plane. *Connecting two ground terminals together with a trace to a single via defeats the purpose of having independent ground leads on the device package!*
- Also, choose component packaging carefully: use devices with a ground reference in the center of the device to reduce the L_{gnd} (4nH vs 15nH). Surface mount devices are preferred over through-hole packages for this reason.



Bypassing and Decoupling

- Capacitor Usage and Resonance
- Parallel Capacitors
- Placement

Types of capacitor usage

There are three primary uses for capacitors:

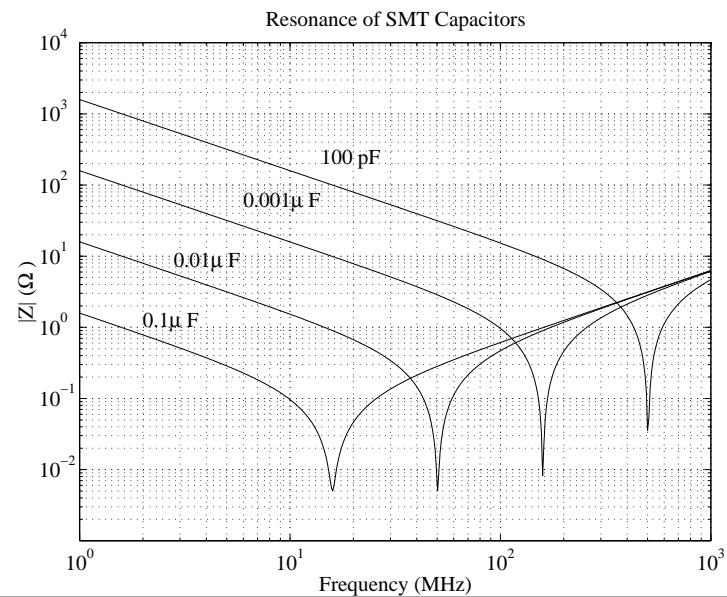
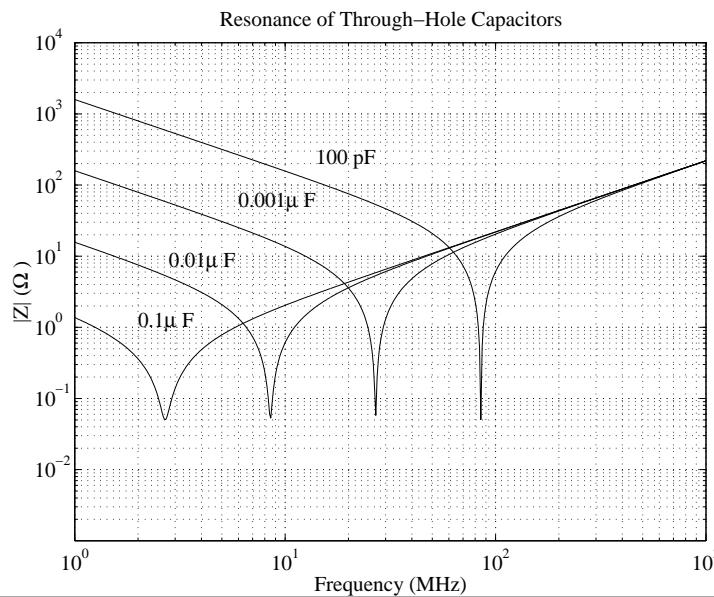
1. *Bulk* Used to maintain constant DC voltage and currents when all signal pins switch. Also prevents power drop out due to dI/dt current surges from the components.
2. *Bypassing* Removes unwanted common-mode RF noise from components or cables by placing an AC-short to ground. This keeps the unwanted energy from entering a protected area as well as limiting the bandwidth. Bypassing is also used to divert RF energy from one area to another.
3. *Decoupling* Removes RF energy injected into the power planes from high frequency components consuming power at the device's switching speed. They also provide a small amount of energy to function as localized bulk capacitors.



Resonance Effects

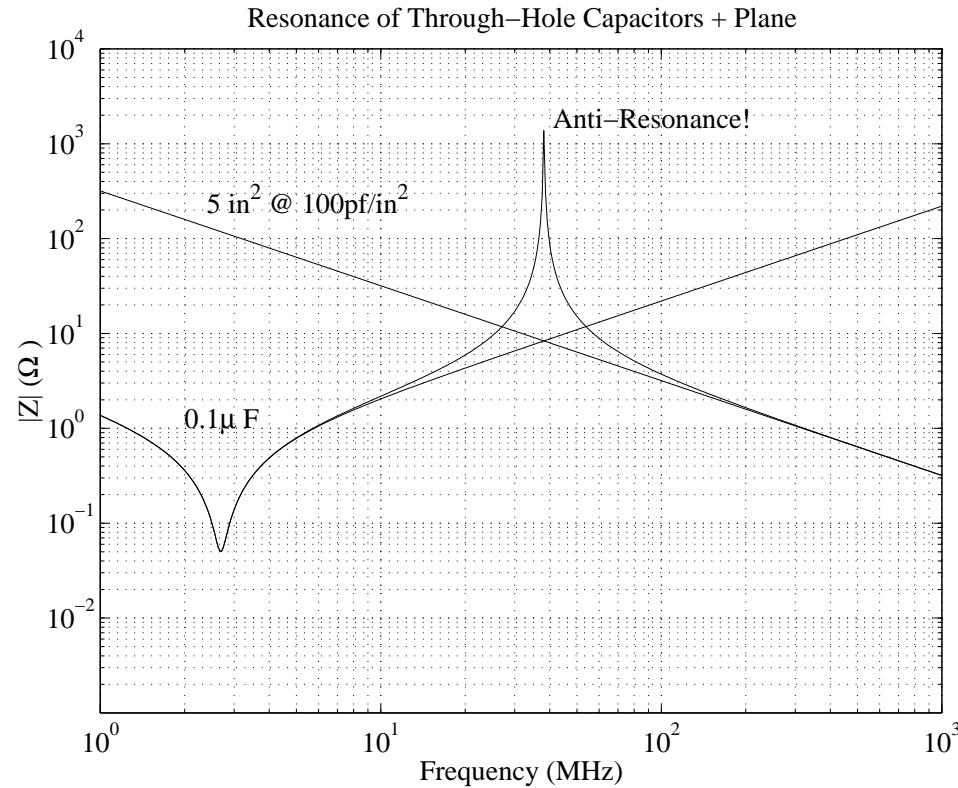
Remember, the capacitors really have an ESL and ESR.

- Through-hole: $ESL \approx 35\text{nH}$ and $ESR \approx 50\text{m}\Omega$
- Surface Mount: $ESL \approx 1\text{nH}$ and $ESR \approx 5\text{m}\Omega$



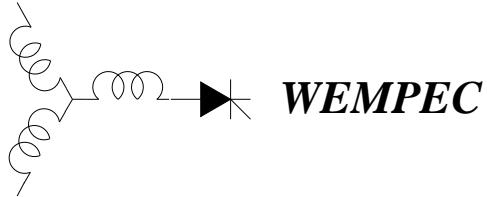
Parallel Capacitors

Remember that the power planes form a capacitor.



Tips on Parallelizing Capacitors

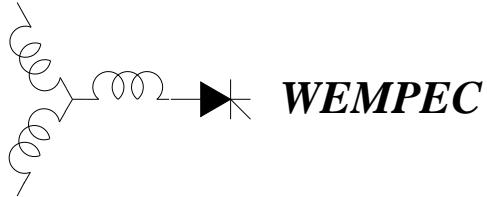
- Parallel capacitors of the same value will increase the net capacitance and reduce the ESL and ESR. The reduction of the ESL and ESR is the most important property. Improvements of 6dB have been observed (replacing one capacitor with multiple smaller ones).
- Be careful to remember that the values will be different and anti-resonance will occur.
- Choose values such that the anti-resonance will not occur at a harmonic of a generated signal (either a switching *or* transition frequency).
- See *Printed Circuit Board Design Techniques for EMC Compliance*, pg. 55 for capacitor value design procedure. (Giri's book)



Capacitor Placement

Key idea is to reduce path inductance

- location location location
- the location of the components is limited by mechanical constraints
- SMT parts can be closer than THT parts
- trace inductance will be 3-10x larger than plane inductance
- each via adds 1-3 nH of inductance



Trace Routing

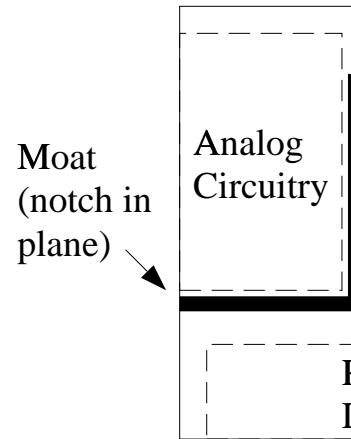
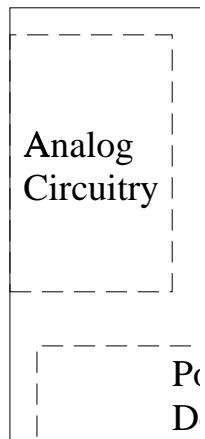
- Keep signal traces AWAY from high frequency devices, e.g. clocks.
- Do *NOT* use auto routers since they typically choose the *worst* possible layout for EMI/EMC concerns...
- Remember the 3-W rule
- Remember the 20-H rule
- Use isolation (moats) in conjunction with the partitioning

Isolation/Moating

Intentionally introducing breaks in the power and/or ground planes.

WHY???

Consider the following:^{||}

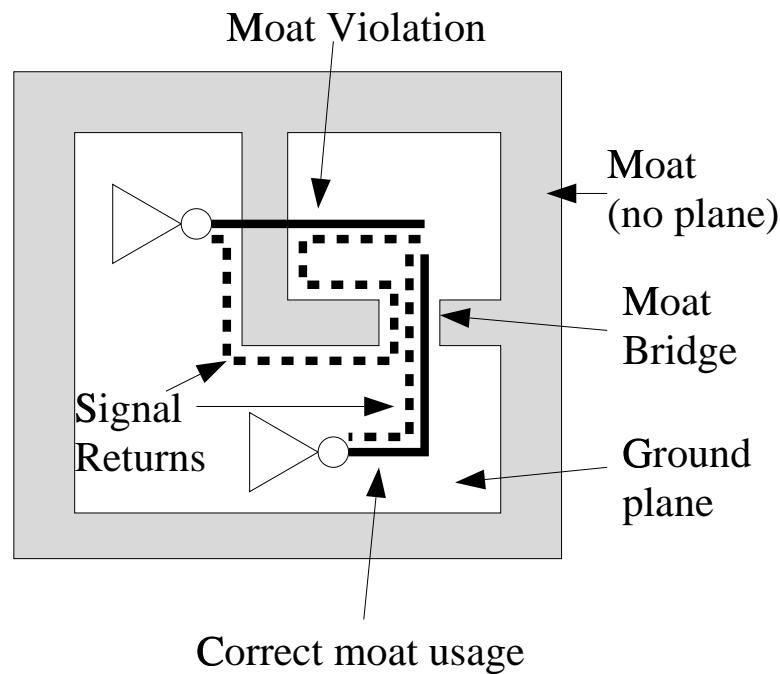


^{||}*Linear Design Seminar*



Moat Violations

Moat violations will virtually always generate lots of EMI, even if the violating trace is “quiet.”



Bridging Moats

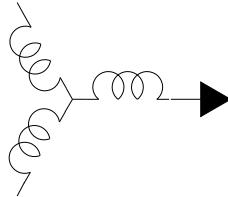
- Make the bridge wide enough for just the required traces (observing 3W)
- Use a ferrite to provide filtering in the *power* trace, but do not put one in the ground traces.
- If a violation *must* occur, place a bypass capacitor across the moat as close to the violation as possible. (capacitor is connected ground to ground).
 - choose for proper filtering bandwith (RF return current)
 - Peak surge voltage capability for ESD protection

ESD Protection

- Provide good shielding with the chassis and connectors
- Provide good grounding connections; wire braid with a 5:1 width:height aspect ratio is good (Solder wick works nicely!).
- Avoid pigtail wiring harnesses. (they make good RF antennae!)
- Filling un-used signal plane with a ground fill helps prevent ESD, not EMI.
- Guard Bands

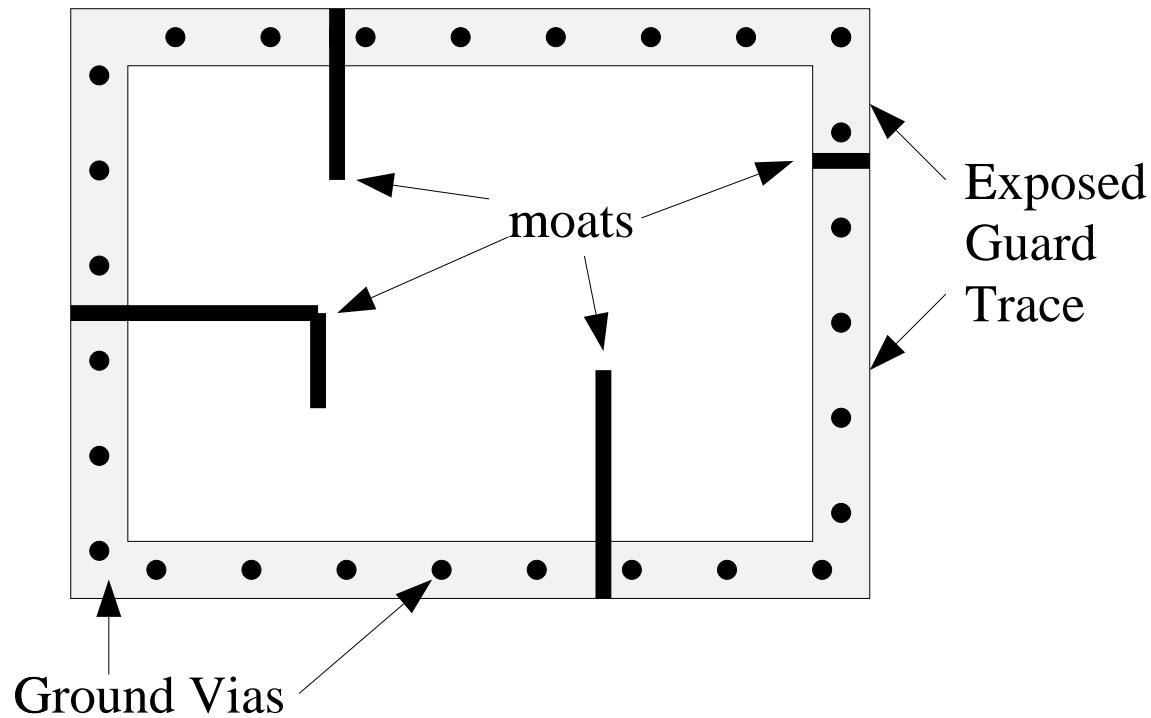
Guard Bands

- Different from guard, shunt or ground traces
- Prevents ESD damage from handling of PCB
- A **NON**-continuous trace around the edge of the PCB on both the top and bottom layers (introduce some moats to prevent ground loops!).
- Should not be covered with the soldermask and should frequently be connected to the ground reference with vias.



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A Guard Band



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课程网址：<http://www.edatop.com/peixun/rfe/110.html>

手机天线设计培训视频课程

该套课程全面讲授了当前手机天线相关设计技术，内容涵盖了早期的外置螺旋手机天线设计，最常用的几种手机内置天线类型——如 monopole 天线、PIFA 天线、Loop 天线和 FICA 天线的设计，以及当前高端智能手机中较常用的金属边框和全金属外壳手机天线的设计，通过该套课程的学习，可以帮助您快速、全面、系统地学习、了解和掌握各种类型的手机天线设计，以及天线及其匹配电路的设计和调试…

课程网址：<http://www.edatop.com/peixun/antenna/133.html>



WiFi 和蓝牙天线设计培训课程

该套课程是李明洋老师应邀给惠普 (HP) 公司工程师讲授的 3 天员工内训课程录像，课程内容是李明洋老师十多年工作经验积累和总结，主要讲解了 WiFi 天线设计、HFSS 天线设计软件的使用，匹配电路设计调试、矢量网络分析仪的使用操作、WiFi 射频电路和 PCB Layout 知识，以及 EMC 问题的分析解决思路等内容。对于正在从事射频设计和天线设计领域工作的您，绝对值得拥有和学习！…

课程网址：<http://www.edatop.com/peixun/antenna/134.html>



CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出, 是最全面、系统、专业的 **CST** 微波工作室培训课程套装, 所有课程都由经验丰富的专家授课, 视频教学, 可以帮助您从零开始, 全面系统地学习 **CST** 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装, 还可超值赠送 3 个月免费学习答疑…

课程网址: <http://www.edatop.com/peixun/cst/24.html>



HFSS 学习培训课程套装

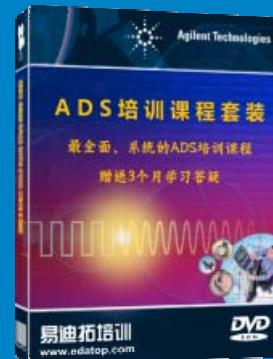
该套课程套装包含了本站全部 **HFSS** 培训课程, 是迄今国内最全面、最专业的 **HFSS** 培训教程套装, 可以帮助您从零开始, 全面深入学习 **HFSS** 的各项功能和在多个方面的工程应用。购买套装, 更可超值赠送 3 个月免费学习答疑, 随时解答您学习过程中遇到的棘手问题, 让您的 **HFSS** 学习更加轻松顺畅…

课程网址: <http://www.edatop.com/peixun/hfss/11.html>

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 **ADS** 培训教程, 共包含 10 门 **ADS** 学习培训课程。课程是由具有多年 **ADS** 使用经验的微波射频与通信系统设计领域资深专家讲解, 并多结合设计实例, 由浅入深、详细而又全面地讲解了 **ADS** 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 **ADS**, 迅速提升个人技术能力, 把 **ADS** 真正应用到实际研发工作中去, 成为 **ADS** 设计专家…

课程网址: <http://www.edatop.com/peixun/ads/13.html>



我们的课程优势:

- ※ 成立于 2004 年, 10 多年丰富的行业经验,
- ※ 一直致力并专注于微波射频和天线设计工程师的培养, 更了解该行业对人才的要求
- ※ 经验丰富的一线资深工程师讲授, 结合实际工程案例, 直观、实用、易学

联系我们:

- ※ 易迪拓培训官网: <http://www.edatop.com>
- ※ 微波 EDA 网: <http://www.mweda.com>
- ※ 官方淘宝店: <http://shop36920890.taobao.com>