Emissions from power switching circuits

Section 7

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Outline

EMAC services

- **emissions from switching circuits**
- **coupling paths**
  - differential mode conducted
  - common mode conducted
  - radiated
- **construction techniques**
  - screens
  - transformers

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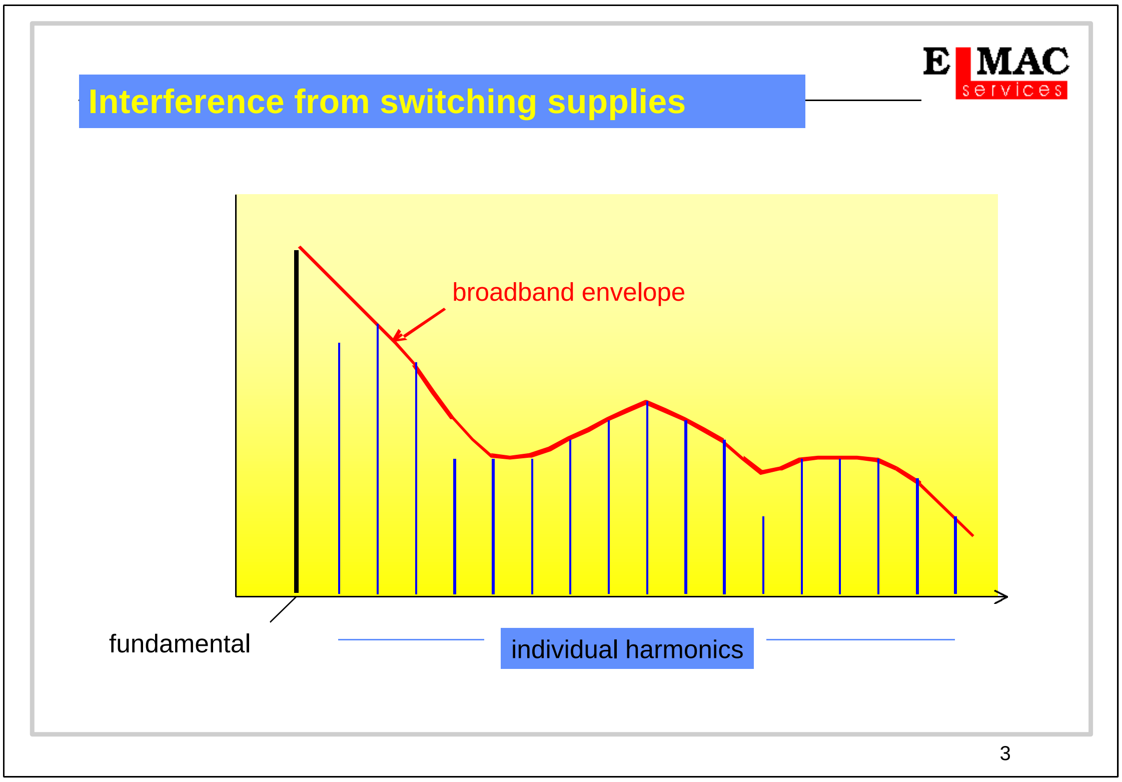
The switching power supply is a serious cause of interference in the low frequency range since it is essentially a high-power squarewave oscillator. Depending on the type of circuit and the power levels involved, high di/dt loops or high dV/dt nodes will be present in the circuit and will couple to the external environment via several routes, often involving stray reactances. The trend to higher power efficiencies means faster switching speeds, which increase di/dt and dV/dt further for a given power level, and extend the upper frequency emissions into the VHF range.

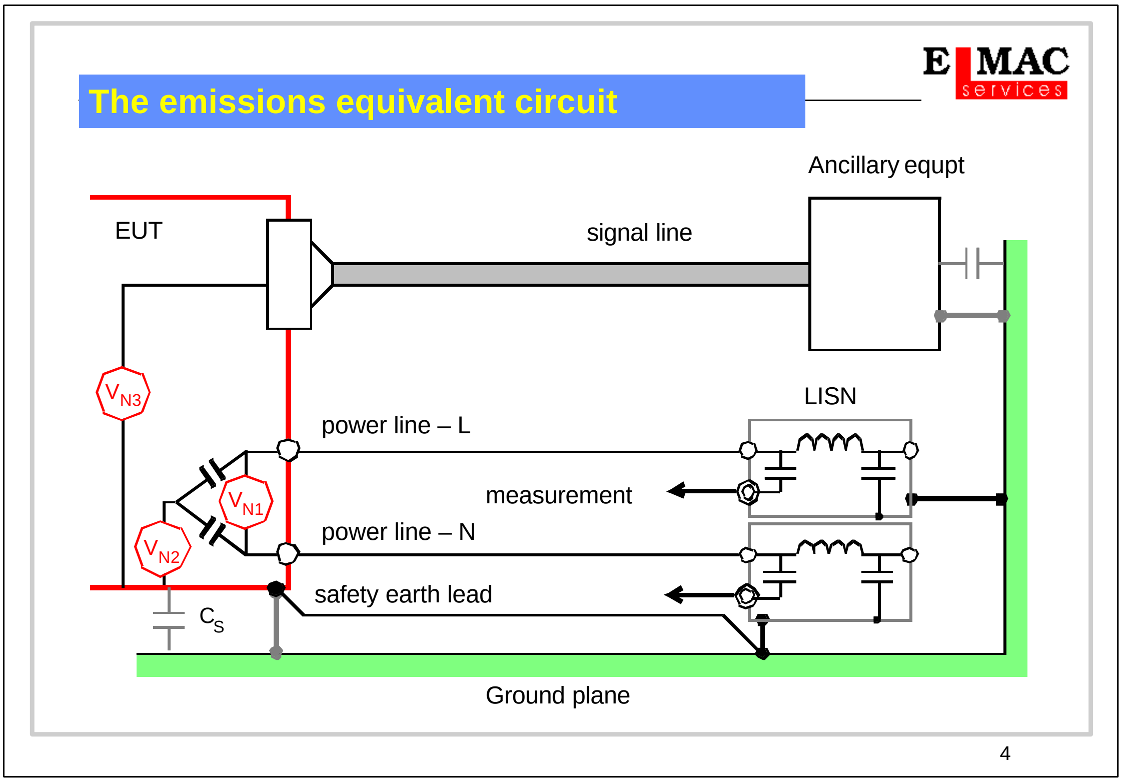
Switching supply design becomes a trade-off between high volumetric and power efficiency on the one hand, and low emissions on the other, with cost an important factor.



The major component of SMPS noise emission is due to the switching frequency and its harmonics. Asymmetry of the switching waveform normally ensures that except at the lowest orders both odd and even harmonics are present.

If the fundamental frequency is well defined then a spectrum of narrowband emissions is produced which can extend beyond 30MHz when the waveform transition times are fast. A measurement bandwidth of 9kHz means that individual harmonics can be distinguished if the fundamental frequency is greater than about 20kHz. Designs in which the frequency is not stable will normally show modulation due to input or output ripple which has the effect of broadening individual harmonic lines so that an emission “envelope” is measured.

A further cause of broadband noise may be due to reverse recovery switching of the input rectifier diodes.

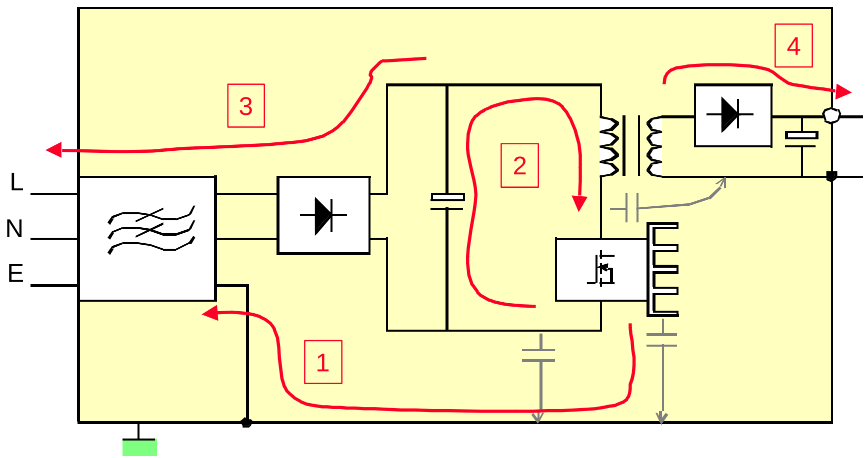


The LISN measurement for conducted emissions uses the ground plane as reference, with the noise signal being picked off either live or neutral wire. The EUT contains multiple noise sources. VN1 appears differentially across L and N; part of this voltage will be measured on the live wire, part on the neutral, their relative amplitudes depending on the relative impedances to earth.

VN2 appears in common mode between the power lines and the enclosure of the EUT. A metallic enclosure grounded via a safety earth lead is referred back to the ground reference plane at the LISN. If the enclosure is non-metallic and there is no safety earth, the common-mode coupling is dominated by stray capacitance CS between the EUT and the ground plane.

As well as the noise directly coupled to the power leads, noise voltages at VN3 drive current through any output lines. Although the signal line emissions are not measured directly, such current can flow through the impedances which are common to the power line measurement circuit (CS and/or the safety earth) and therefore contribute to emissions measured on the power lines.

The switchmode supply – coupling paths



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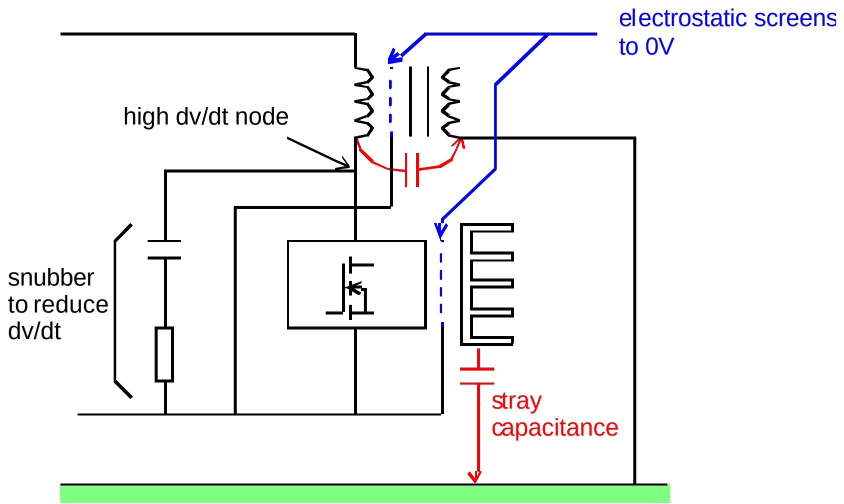
Switching supplies present extreme difficulties in containing generated interference. Typical switching frequencies of 50 - 200kHz can be emitted by both differential and common-mode mechanisms. Lower frequencies are more prone to differential-mode emission while higher frequencies are worse in common mode. Major emission routes are as shown:

- (1) capacitive coupling to earth (E-field radiation)
- (2) H-field radiation from high di/dt loops and magnetics
- (3) differential-mode conducted through DC link
- (4) conducted and/or radiated on output

Most standards regulate conducted emissions above 150kHz. Some relief can be obtained by operating just below this frequency so that the fundamental is unregulated and the third harmonic frequency is high enough for simple filtering to be effective.

Capacitive coupling to earth



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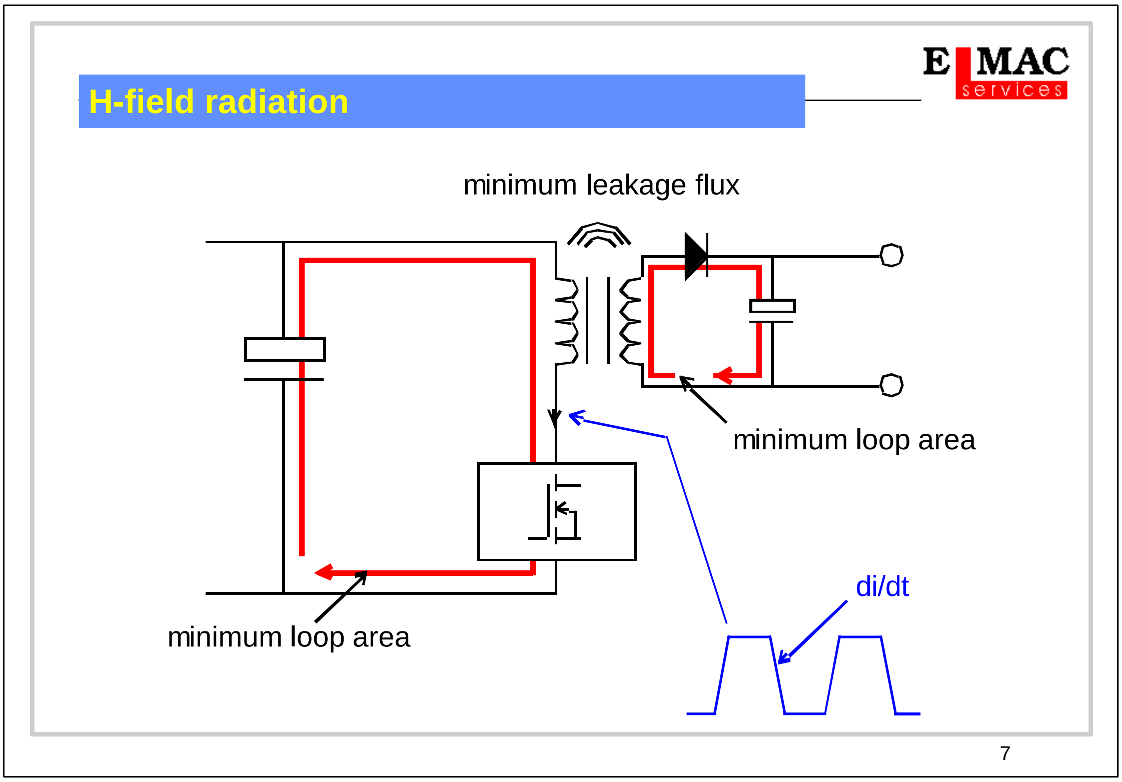
High dv/dt at the switching point (the collector or drain of the switching transistor) will couple capacitively to ground and create common-mode interference currents. The solution is to minimize dv/dt, and minimize coupling capacitance or provide a preferential route for the capacitive currents.

dv/dt is reduced by a snubber and by keeping a low transformer leakage inductance and di/dt. These objectives are also desirable to minimize stress on the switching device, although they increase power losses. Capacitive coupling is reduced by providing appropriate electrostatic screens, particularly in the transformer and on the device heatsink. Note the proper connection of the screen, to return circulating currents to their source, not to earth. Physical separation of parts carrying high dv/dt is desirable, or the offending component(s) can be given extra screening.

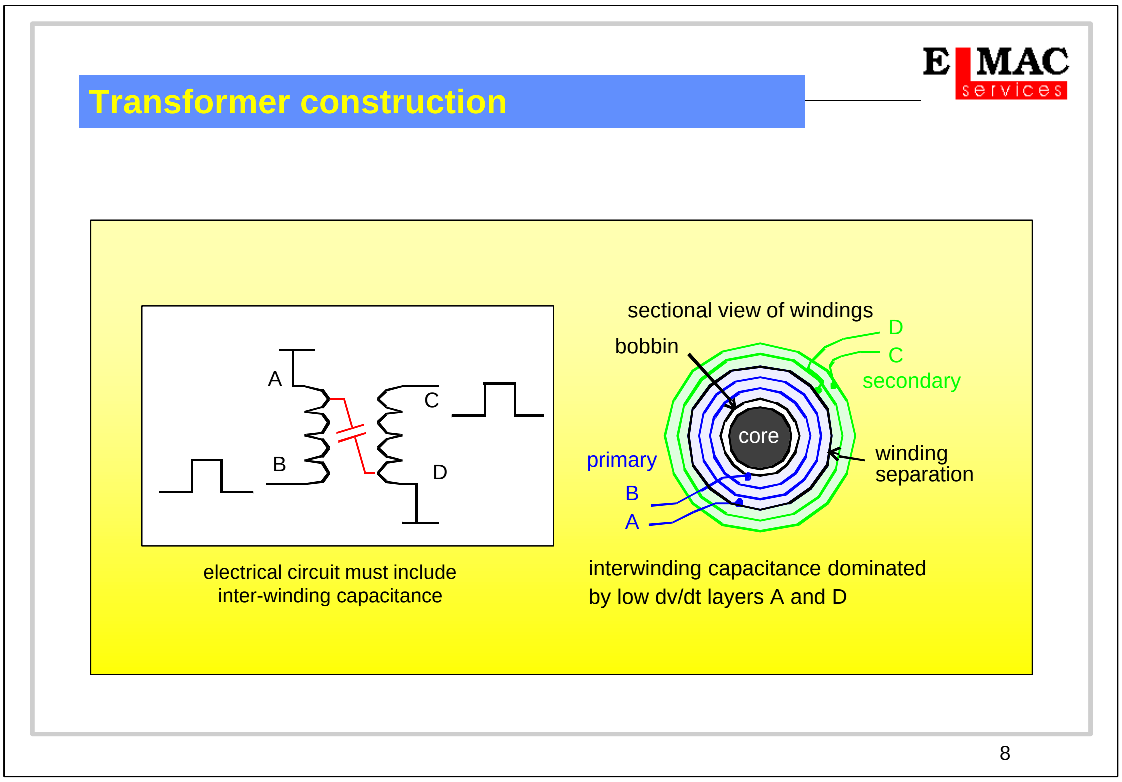
Screening of the whole unit will ensure that capacitive coupling from individual nodes is referred to the screen rather than to the external environment.



Magnetic field radiation from a loop which is carrying a high di/dt can be minimized by reducing the loop area or by reducing di/dt. Loop area is a function of layout and physical component dimensions. di/dt is a tradeoff against switching frequency and power losses in the switch. It can to some extent be controlled by slowing the rate-of-rise of the drive waveform to the switch, although the trend towards minimizing power losses and increasing frequencies goes directly against this requirement.

The leakage flux from the transformer or inductor can also be significant and is affected by the placement, orientation and construction of the core. No sensitive components or tracks should be routed near to this component.

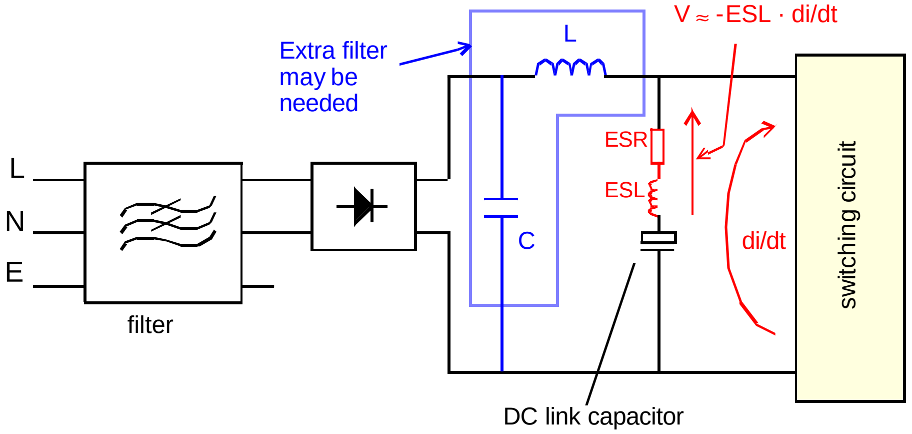
Screening will have little effect on the magnetic field radiation although it will reduce the associated electric field. The output circuit is often at a lower voltage than the input and therefore carries a higher di/dt; it is therefore as important, if not more so, to pay attention to the output circuit loop area.



Even if the transformer is not screened, its construction can aid or hinder capacitive coupling from primary to secondary. Separating the windings onto different bobbins reduces their capacitance but increases leakage inductance. Coupling is greatest between nodes of high dv/dt; so the end of the winding which is connected to VCC or ground can screen the rest of the winding in a multi-layer design.

Screening will not affect the magnetic field radiation from the transformer although it will reduce the electric field associated with the outer windings. The transformer (or inductor) core should be in the form of a closed magnetic circuit in order to restrict magnetic radiation from this source. A toroid is the optimum from this point of view, but may not be practical because of winding difficulties or power losses; if you use a gapped core such as the popular E-core type, the gap should be directly underneath the windings since the greatest magnetic leakage flux is to be found around the gap.

Differential-mode interference



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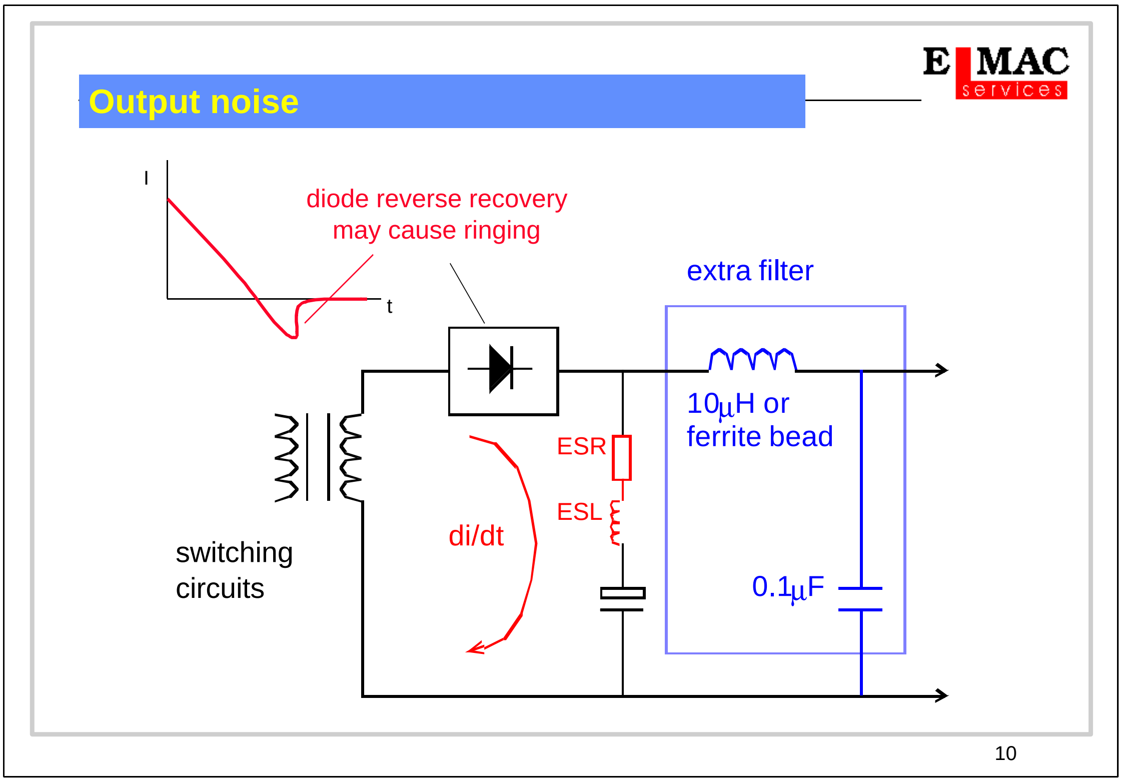
Differential-mode interference is caused by the voltage developed across the finite impedance of the reservoir or DC link capacitor at high di/dt. Careful choice of the capacitor type can reduce the value of its internal impedance but its physical size will mean that there is always significant inductance across which high frequency interference components will appear.

Extra series inductance and parallel capacitance on the input side will attenuate the voltage passed to the input terminals. When a bank of parallel input capacitiors are used, it is often possible to separate these into two sections with a small inductor. Series inductors of more than a few tens of microhenries are difficult to realize at high dc currents (remembering that the inductor must not saturate at the peak ripple current, which is much higher than the dc average current), and multiple sections with smaller inductors will be more effective than a single section since their self resonance frequencies will be higher. A separate mains input filter, if present, will offer some differential-mode rejection.



Switching spikes are a feature of the dc output of all switching supplies, partly because of the finite impedance of the output reservoir and partly because of capacitive coupling through the transformer. Such spikes are conducted out of the unit on the output lines in both differential and common mode, and may re-radiate onto other leads or be coupled to the ground connection and generate common-mode interference.

A low-ESL reservoir capacitor is preferable, but good suppression in differential mode can be obtained, as with the input, with a high frequency L-section filter. 20-40dB is obtainable with a ferrite bead and 0.1µF capacitor above 1MHz.

The abrupt reverse recovery characteristic of the output rectifier diode(s) can create extra high frequency ringing and transients, due to the very fast di/dt at turn-off exciting the resonant circuits of the output transformer and filters. The spectrum extends well into the VHF range and it often appears as broadband noise, apparently unrelated to the switching frequency. These can be attenuated by using soft recovery diodes or by paralleling the diodes with a capacitor or an RC or snubber, but this is often directly in opposition to the need for power efficiency.

Layout and design

- shield or separate high dv/dt sources
- keep all critical circuit loop areas small
- avoid coupling to magnetic components
- lay out circuit logically to avoid common impedances
- use minimum acceptable dv/dt and di/dt

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Layout of SMPS units is critical to maintaining their EMC. Since many of the coupling paths are via near field induction, where coupling varies markedly over short distances, special attention must be paid to such details.

Loop areas can be minimized by running signal/power tracks immediately next to and parallel to their return tracks. Sensitive tracks or wires should not be run near to inductors or transformers, especially their magnetic flux leakage points; if necessary, orientate such tracks for minimum pickup. Unfiltered or “clean” circuits must be kept separate from noise sources, and large area sources of high dv/dt (e.g. live heatsinks or large transformer windings) should be screened or separated from other components and circuits. All ground and power rails should be carefully checked to ensure they do not offer common impedance routes within or outside the unit.

End of this section

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