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PROTECTION PRODUCTS

Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SR series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge **(ESD)**, electrical fast transients **(EFT)**, and **lightning.**

The unique design of the SR series devices incorporates eight surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The SRV05-4 has a low typical capacitance of 3pF and operates with virtually no insertion loss to 1GHz. This makes the device ideal for protection of high-speed data lines such as USB 2.0, Firewire, DVI, and gigabit Ethernet interfaces.

The low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Features

◆ ESD protection for high-speed data lines to
 IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
 IEC 61000-4-4 (EFT) 40A (5/50ns)
 IEC 61000-4-5 (Lightning) 12A (8/20µs)
◆ Array of surge rated diodes with internal TVS Diode
◆ Small package saves board space
◆ Protects four I/O lines
◆ Low capacitance: **3pF** typical
◆ Low clamping voltage
◆ Low operating voltage: 5.0V
◆ Solid-state silicon-avalanche technology

Mechanical Characteristics

◆ JEDEC SOT-23 6L package
◆ Molding compound flammability rating: UL 94V-0
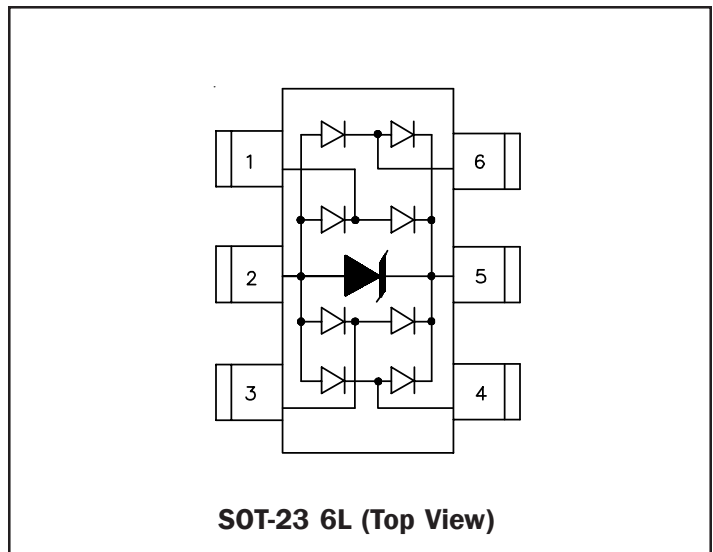◆ Marking : V05
◆ Packaging : Tape and Reel per EIA 481

Applications

◆ USB 2.0 Power and Data Line Protection
◆ Video Graphics Cards
◆ Monitors and Flat Panel Displays
◆ Digital Video Interface (DVI)
◆ 10/100/1000 Ethernet
◆ Notebook Computers
◆ SIM Ports
◆ ATM Interfaces
◆ IEEE 1394 Firewire Ports

Circuit Diagram
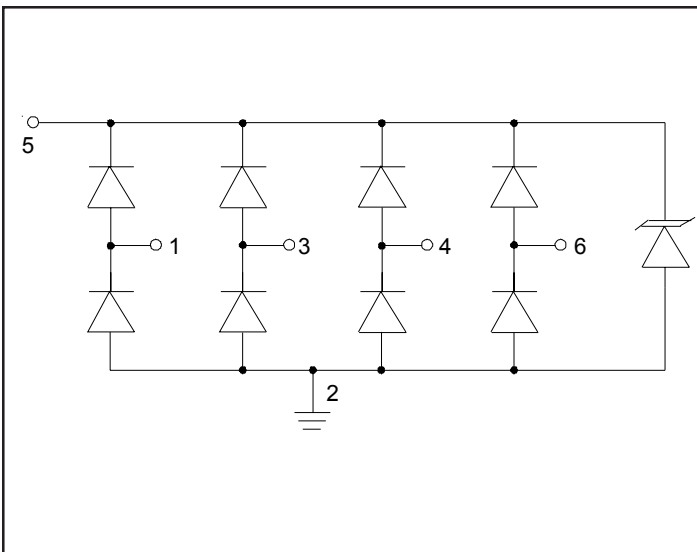
Schematic and PIN Configuration

SOT-23 6L (Top View)

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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	300	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	12	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

SRV05-4						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to 2			5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Pin 5 to 2	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C Pin 5 to 2			5	µA
Forward Voltage	V_F	I_f = 15mA			1.2	V
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs Any I/O pin to Ground			12.5	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs Any I/O pin to Ground			17.5	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Any I/O pin to Ground		3	5	pF
		V_R = 0V, f = 1MHz Between I/O pins		1.5		pF

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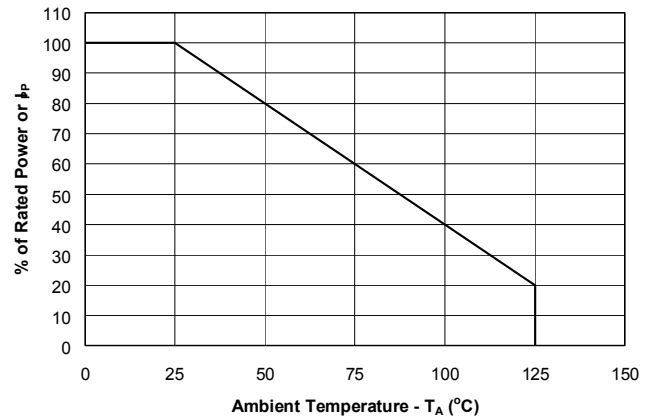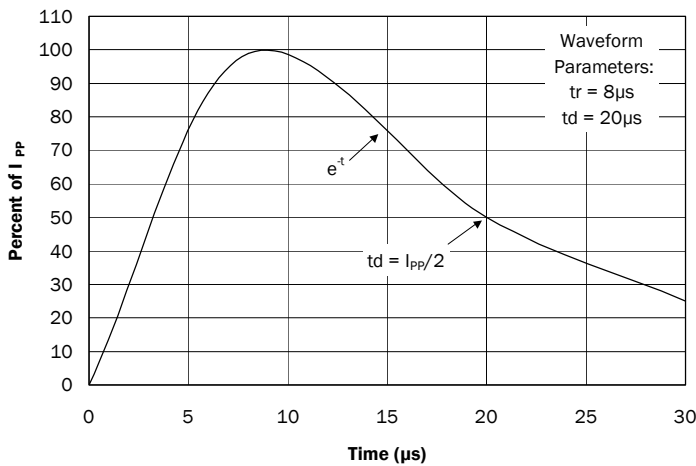
Typical Characteristics

Non-Repetitive Peak Pulse Power vs. Pulse Time
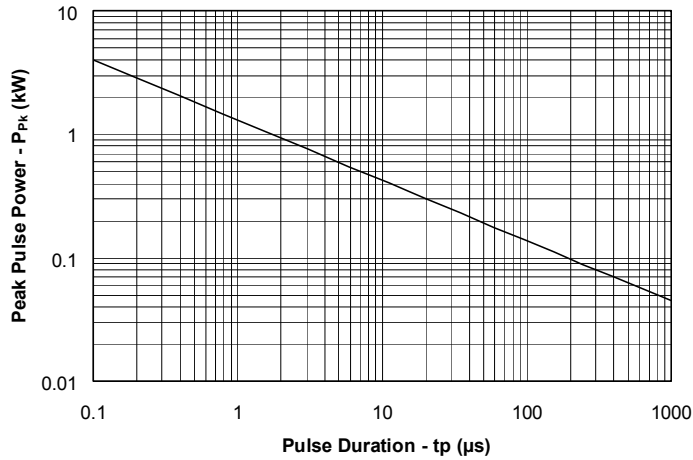
Power Derating Curve

Pulse Waveform

Waveform Parameters:
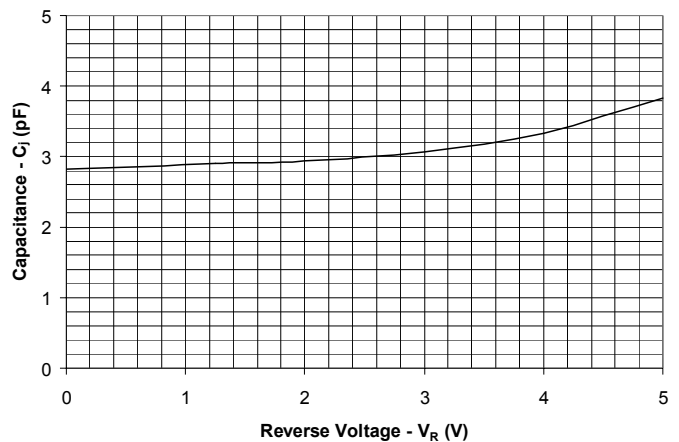tr = 8μs
td = 20μs

e^{-t}

td = $I_{PP}/2$

Clamping Voltage vs. Peak Pulse Current

Waveform Parameters:
tr = 8μs
td = 20μs
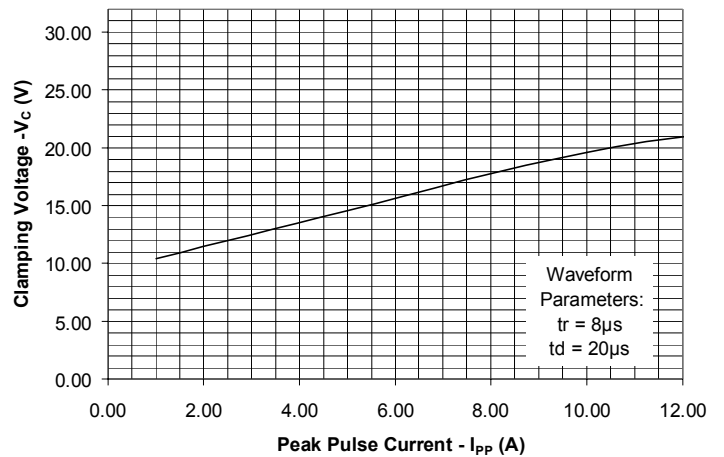
Forward Voltage vs. Forward Current

Waveform Parameters:
tr = 8μs
td = 20μs
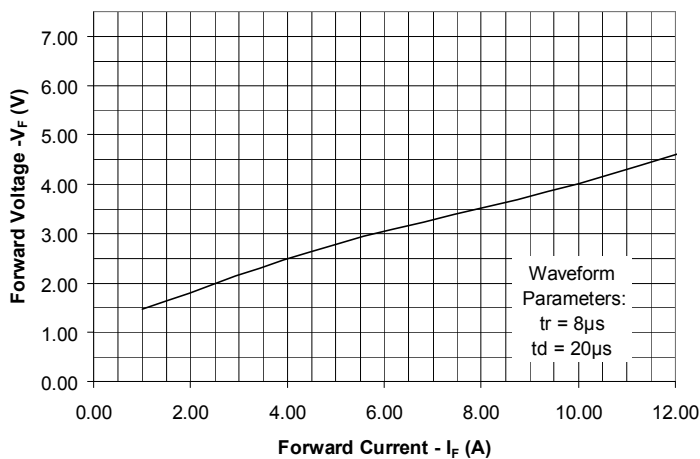
Capacitance vs. Reverse Voltage

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Insertion Loss S21

CH1 S21 LOG 3 dB/ REF 0 dB

START .030 000 MHz STOP 3 000.000 000 MHz

Analog Cross Talk

CH1 S21 LOG 20 dB/ REF 0 dB

START .030 000 MHz STOP 3 000.000 000 MHz

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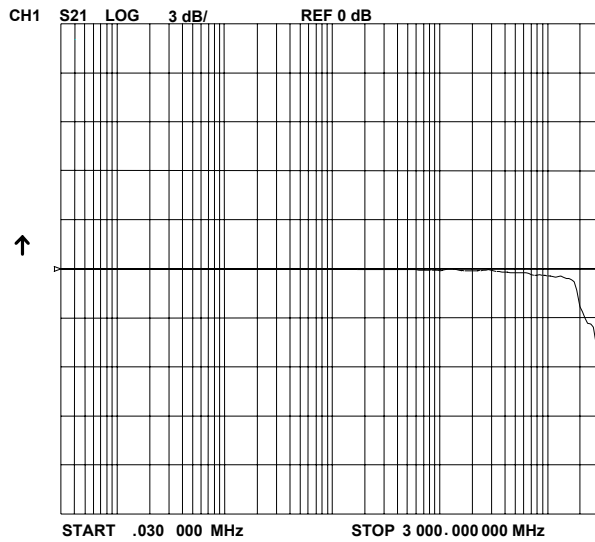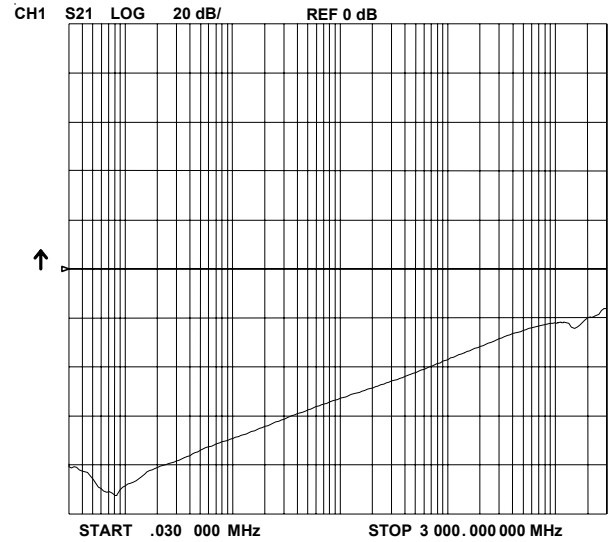
Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

The SRV05-4 TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. The negative reference (REF1) is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (REF2) is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. The SRV05-4 can be isolated from the power supply by adding a series resistor between pin 5 and V_{CC}. A value of 100kΩ is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

ESD Protection With RailClamps®

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 1 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds

Data Line and Power Supply Protection Using Vcc as reference
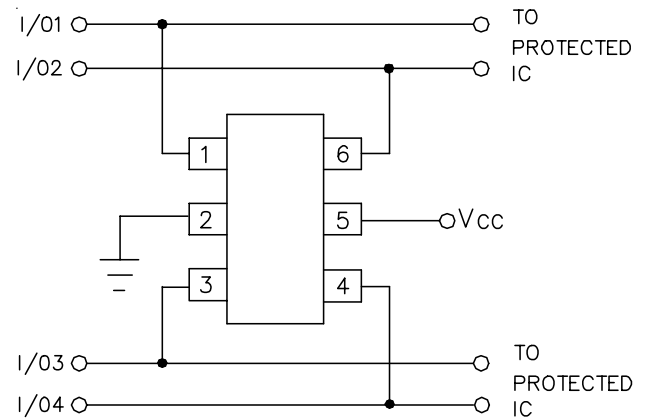
Data Line Protection with Bias and Power Supply Isolation Resistor
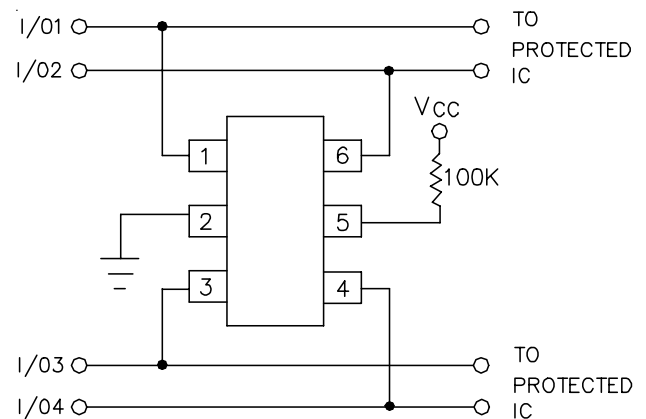
Data Line Protection Using Internal TVS Diode as Reference

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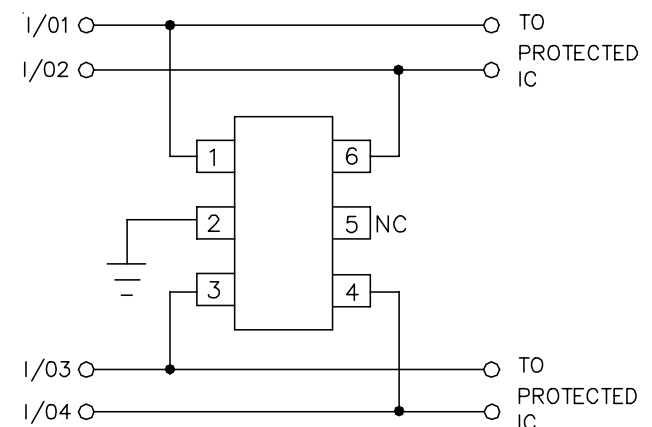
Applications Information *(continued)*

the reference voltage plus the V_F drop of the diode. For negative events, the bottom diode will be biased when the voltage exceeds the V_F of the diode. At first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$V_C = V_{CC} + V_F$ (for positive duration pulses)
$V_C = -V_F$ (for negative duration pulses)

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$V_C = V_{CC} + V_F + L_P \, di_{ESD}/dt$ (for positive duration pulses)
$V_C = -V_F - L_G \, di_{ESD}/dt$ (for negative duration pulses)

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$V = L_P \, di_{ESD}/dt = 1\text{X}10^{-9} \, (30 \, / \, 1\text{X}10^{-9}) = 30V$

Example:
Consider a V_{CC} = 5V, a typical V_F of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$V_C = 5V + 30V + (10nH \text{ X } 30V/nH) = 335V$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note that it is not uncommon for the V_F of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode
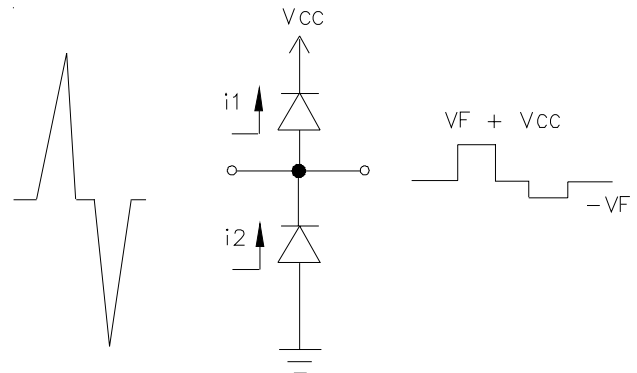

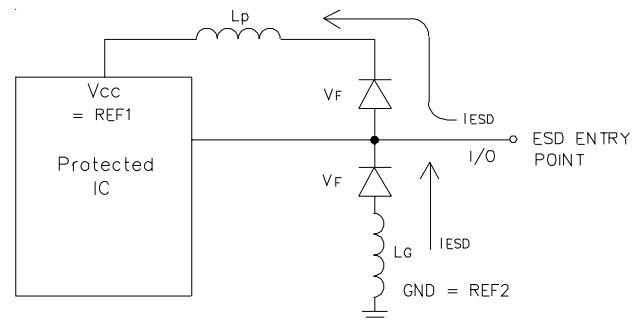**Figure 1 - "Rail-To-Rail" Protection Topology (First Approximation)**

Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection
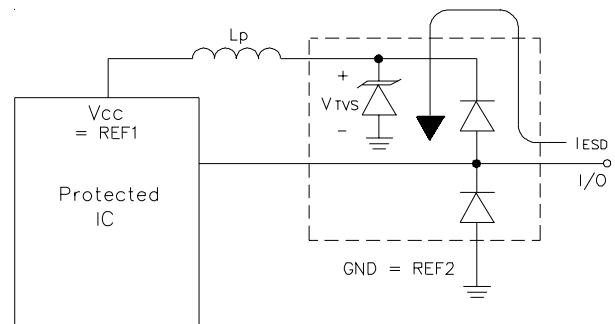

Figure 3 - Rail-To-Rail Protection Using RailClamp TVS Arrays

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PROTECTION PRODUCTS

Applications Information *(continued)*

helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The maximum voltage seen by the protected IC due to this path will be the clamping voltage of the device.

Video Interface Protection

Video interfaces are susceptible to transient voltages resulting from electrostatic discharge (ESD) and "hot plugging" cables. If left unprotected, the video interface IC may be damaged or even destroyed. Protecting a high-speed video port presents some unique challenges. First, any added protection device must have extremely low capacitance and low leakage current so that the integrity of the video signal is not compromised. Second, the protection component must be able to absorb high voltage transients without damage or degradation. As a minimum, the device should be rated to handle ESD voltages per IEC 61000-4-2, level 4 (±15kV air, ±8kV contact). The clamping voltage of the device (when conducting high current ESD pulses) must be sufficiently low enough to protect the sensitive CMOS IC. If the clamping voltage is too high, the "protected" device may latch-up or be destroyed. Finally, the device must take up a relatively small amount of board space, particularly in portable applications such as notebooks and handhelds. The SRV05-4 is designed to meet or exceed all of the above criteria. A typical video interface protection circuit is shown in Figure 4. All exposed lines are protected including R, G, B, H-Sync, V-Sync , and the ID lines for plug and play monitors.
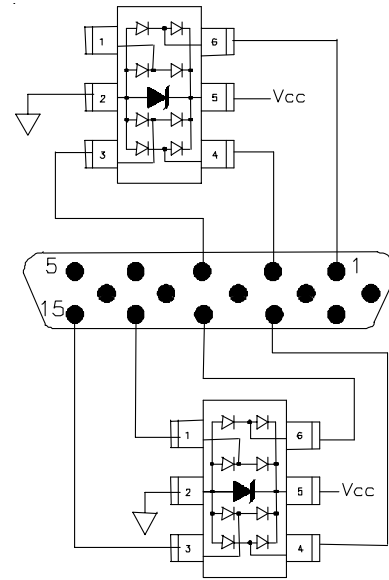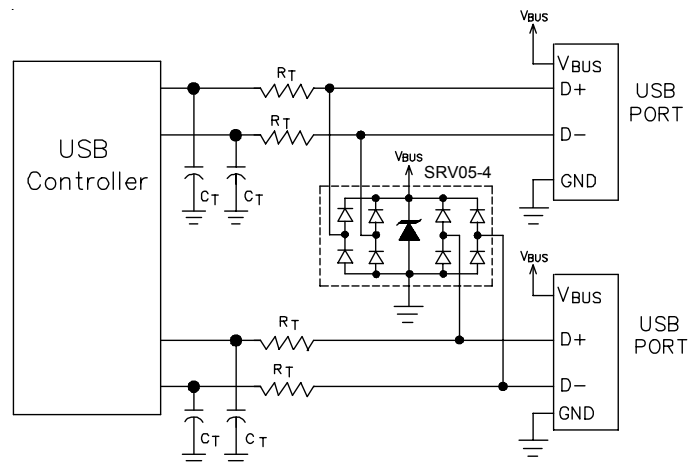
Universal Serial Bus ESD Protection

The SRV05-4 may also be used to protect the USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to two USB ports (Figure 5). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.
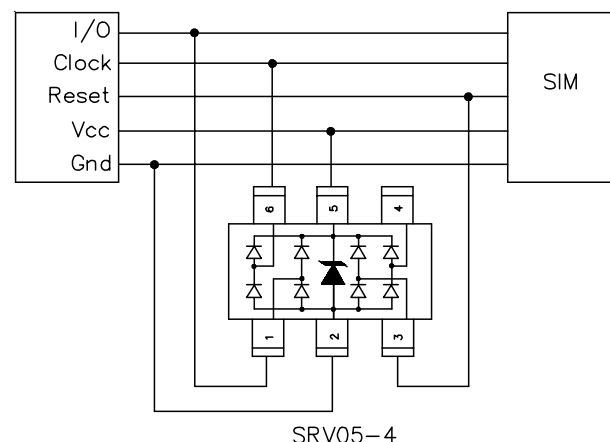

Figure 4 - Video Interface Protection

Figure 5 - Dual USB Port Protection

Figure 6 - SIM Port

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PROTECTION PRODUCTS

DVI Protection

The small geometry of a typical digital-visual interface (DVI) graphic chip will make it more susceptible to electrostatic discharges (ESD) and cable discharge events (CDE). Transient protection of a DVI port can be challenging. Digital-visual interfaces can often transmit and receive at a rate equal to or above 1Gbps. The high-speed data transmission requires the protection device to have low capacitance to maintain signal integrity and low clamping voltage to reduce stress on the protected IC. The SRV05-4 has a low typical insertion loss of <0.4dB at 1GHz (I/O to ground) to ensure signal integrity and can protect the DVI interface to the 8kV contact and 15kV air ESD per IEC 61000-4-2 and CDE.

Figure 7 shows how to design the SRV05-4 into the DVI circuit on a flat panel display and a PC graphic card. The SRV05-4 is configured to provide common mode and differential mode protection. The internal TVS of the SRV05-4 acts as a 5 volt reference. The power pin of the DVI circuit does not come out through the connector and is not subjected to external ESD pulse; therefore, pin 5 should be left unconnected. Connecting pin 5 to Vcc of the DVI circuit may result in damage to the chip from ESD current.

10/100 ETHERNET PROTECTION

Ethernet ICs are vulnerable to damage from electro-static discharge (ESD). The internal protection in the PHY chip, if any, often is not enough due to the high energy of the discharges specified by IEC 61000-4-2. If the discharge is catastrophic, it will destroy the protected IC. If it is less severe, it will cause latent failures that are very difficult to find.

10/100 Ethernet operates at 125MHz clock over a twisted pair interface. In a typical system, the twisted-pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver, with the transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmit or receive line pair and is capacitively coupled through the transformer to the Ethernet chip. Figure 8 shows how to design the SRV05-4 on the line side of a 10/100 ethernet port to provide differential mode protection. The common mode isolation of the transformer will provide common mode protection to the rating of the transformer isolation which is usually >1.5kV. If more common mode protection is needed, figure 9 shows how to design the SRV05-4 on the IC side of the 10/100
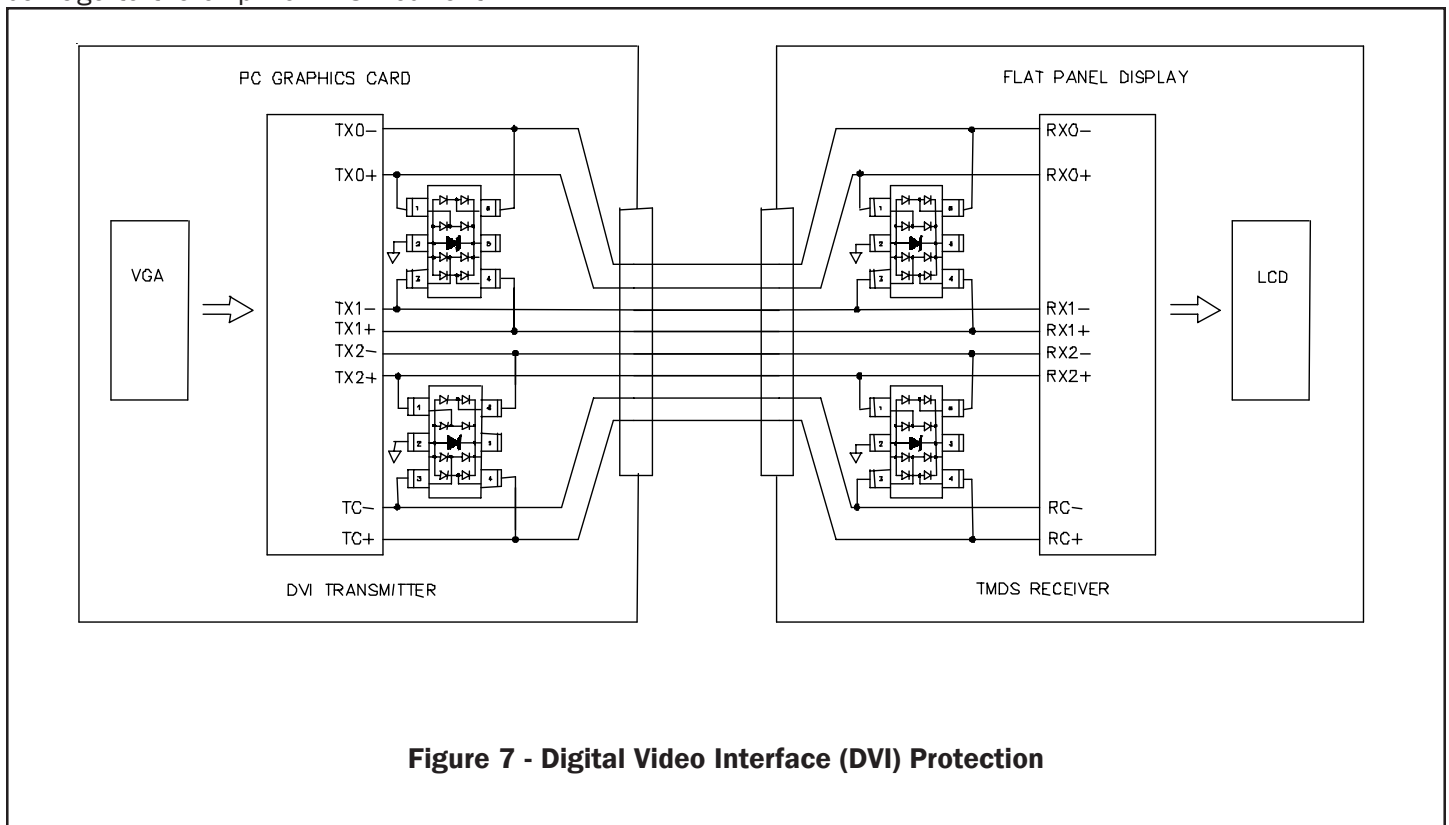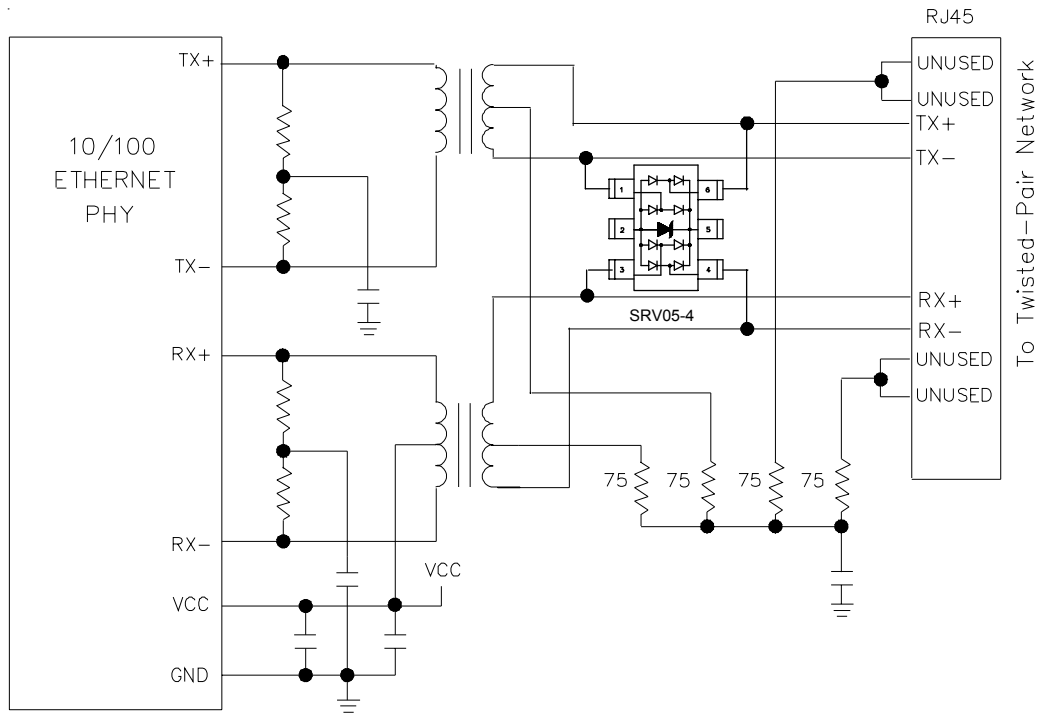

Figure 7 - Digital Video Interface (DVI) Protection

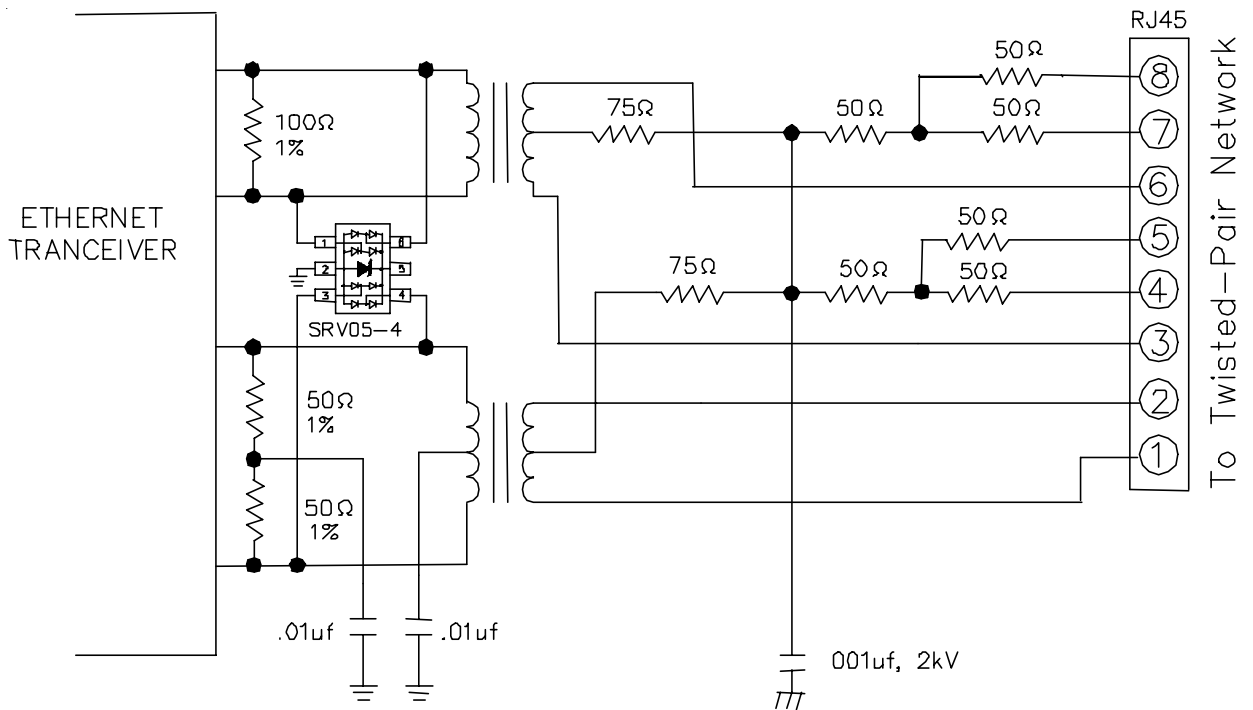**Figure 8 - 10/100 Ethernet Differential Protection**

**Figure 9 - 10/100 Ethernet Differential and Common Mode Protection**

![SEMTECH]

10/100 ETHERNET PROTECTION CONT'

Ethernet circuit to provide differential and common mode protection. The SRV05-4 can not be grounded on the line side because the hi-pot test requires the line side not to be grounded.

GIGABIT ETHERNET PROTECTION

The clock rate of gigabit Ethernet is the same 125MHz as the 10/100 Ethernet. However, it uses a complex five level signaling and transmits at a faster data rate that makes it more susceptible to capacitance and insertion loss. The low capacitance and low insertion loss of the SRV05-4 allow it to sit on the gigabit Ethernet line without loss of signal integrity. Figure 10 shows how to connect the SRV05-4 into a gigabit ethernet on the IC side for common and differential mode protection. Notice that pin 5 of the SRV05-4 is not connected. Some may be tempted to connect it to Vcc. In the ethernet application, the Vcc lines does

not come out through the connector and does not need to be protected. Figure 10 shows the LC03-3.3 on the line side for the secondary line protection to Bellcore 1089 intrabuilding. If the designer only needs to meet ESD, CDE and low level lightning, the LC03-3.3 can be omitted.


Figure 10 - Gigabit Ethernet Protection for Bellcore 1089 Intra-Building Protection
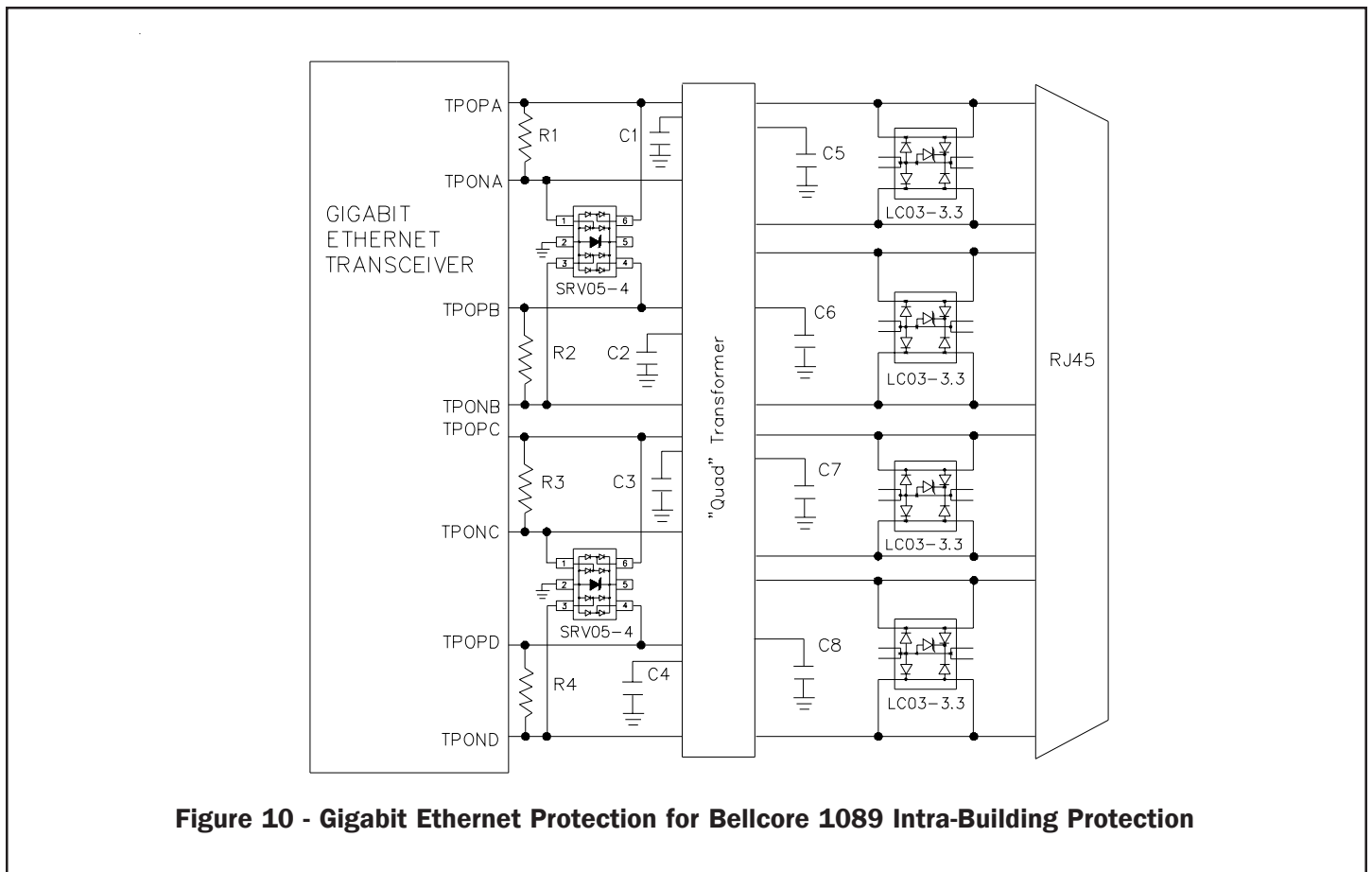
PROTECTION PRODUCTS

Outline Drawing
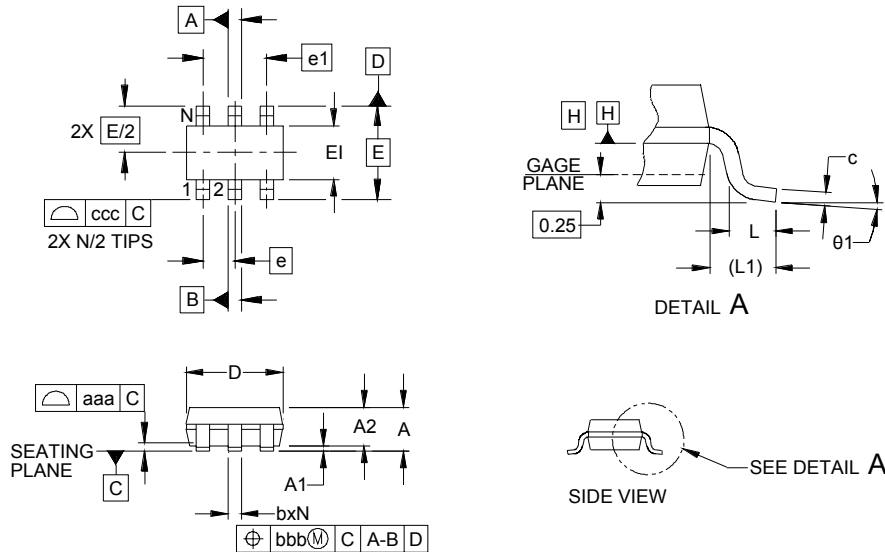
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.118	2.80	2.90	3.00
E1	.060	.063	.069	1.50	1.60	1.75
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(.024)			(0.60)		
N	6			6		
θ1	0°	-	10°	0°	-	10°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		

DETAIL A

SIDE VIEW

SEE DETAIL A

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern
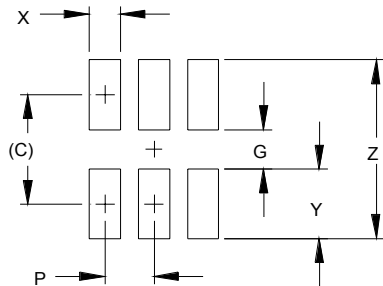
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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Marking Codes

V05
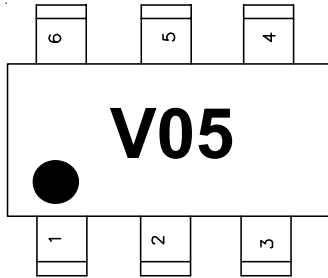
Part Number	Marking Code
SRV05-4	V05

Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SRV05-4.TC	SnPb	3,000	7 Inch
SRV05-4.TCT	Pb free	3,000	7 Inch

Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804

射 频 和 天 线 设 计 培 训 课 程 推 荐

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课程网址：http://www.edatop.com/peixun/antenna/134.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com