



PADS 9.3.1 Release Notes

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Contractor/manufacturer is:

Mentor Graphics Corporation

8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

Telephone: 503.685.7000

Toll-Free Telephone: 800.592.2210

Website: www.mentor.com

SupportNet: supportnet.mentor.com/

Send Feedback on Documentation: supportnet.mentor.com/doc_feedback_form

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Chapter 1

PADS® 9.3.1 Release Notes

Tracking Service Requests, and DRs

If you are a registered SupportNet user, you can always open a new Service Request (SR) and view the status of your own SRs, including the detailed status of any attached Defect Report (DR). The DR number appears as a link in the SR record. You can also view all Service Requests for your site, including all associated DRs.

In addition, all publicly accessible DRs are available on SupportNet. If you would like to know the status of a DR that is not attached to any of your or your company's Service Requests, go to the "[Advanced Search](#)" page on SupportNet, select your product, choose the "Defect Report" TechNotes options, and then enter your query.

Note



Some defects may not be made public for various technical or business reasons; this is determined on a case-by-case basis.

To be kept informed of the progress of a particular DR, open a service request and indicate the DR number you are interested in.

Enhancement Requests

Enhancement requests are made on the Mentor Ideas for PADS site. Post your ideas, vote on others' ideas, and add comments or suggestions.

Please visit the Mentor Ideas for PADS site to offer your unique insight. We look forward to hearing from you!

<http://mentoridea.brightidea.com>

PADS Install

Take a tour of the re-designed PADS Installation program over at technote [mg540524](#).

Tips:

- For frequently asked questions about installation, see technote [mg58662](#) on SupportNet.
- You must have administrative privileges on your system to install the PADS Software, and to run the configurator.

Known Problems and Workarounds

- **Problem** (DR 707525): The PADS Flow 9.3.1 installation is very slow to start when the User Account Control (UAC) is enabled. Occurs only on Windows Vista and Windows 7.

Workaround (TechNote [MG540527](#)): It can take Windows (Vista or 7) up to a few minutes to scan the 1.5GB installation executable before prompting for elevated permissions via the UAC prompt. You can tell it's the UAC causing the delay, and that the installation is still functioning, when you can see a `consent.exe` running in Task Manager (processes tab) and the amount of CPU it is using is greater than 0.

To reduce this time, if you are installing from a DVD or across a network share, copy the file local before executing. As an additional step (to further reduce the time) - right click on the "Command Prompt" icon in the Start Menu (under Accessories) and select "Run as Administrator"; and run the "PADS9.3.1_mib.exe" from the command line.

Alternatively, turn off the UAC temporarily (Control Panel > User Accounts > User Accounts > Change User Account Control Settings), which requires a reboot before the change becomes active.

- **Problem:** PADS install sometimes crashes after the "Unpacking Mentor Installation Program" dialog

Workaround (TechNote [MG551247](#)):

1. Run the Mentor Install Program (MIP) manually, from the following Start Menu location:
Start menu > Programs > Mentor Graphics > Mentor Install
2. Select the **Install Products** option/button
3. In the **Select a source** field, click the **Search...** button and browse to the installation executable (PADS9.3.1_mib.exe).
4. In the **Select a target location**, accept the default and recommended **C:\MentorGraphics** target, or browse to an alternate location.
5. Click **Next >>** and follow the dialogs to complete the installation

- **Problem (DR 739597):** Microsoft Visual C++ 2005 SP1 Redistributable package prompts for a reboot during the PADS9.3.1 installation. Should I reboot or wait until the installation completes?

Workaround (TechNote [MG540526](#)): Press “No” to postpone the reboot. Once the installation completes, reboot your computer. After the reboot, run the Configurator from the following Start Menu shortcut:

Start menu > **Programs** > **Mentor Graphics SDD** > **The MGC SDD Configurator**

- **Problem:** The PADS installer may ask you to reboot to install the Microsoft Visual C++ 2008 Redistributable software.

Workaround: The PADS 9.3.1 release uses the Microsoft Visual C++ 2008 compilers which have a runtime compatibility requirement. During installation of PADS 9.3.1, your system is automatically checked to see if it meets these requirements. If not, the Microsoft Visual C++ 2008 SP1 Redistribution software will be installed.

In some cases, this will require your system be rebooted. If a reboot is required, a message appears where you must click **OK**. Installation cannot be successfully completed until after a reboot has occurred. Once the system has been rebooted, you must restart the Mentor Installation Program and continue your installation of PADS 9.3.1.

Tip: You can avoid this potential reboot by pre-installing the Microsoft Visual C++ 2008 SP1 Redistribution package before you install the PADS 9.3.1 release.

Note: If you are performing batch or third party distributed installations of PADS 9.3.1, it is strongly recommended that you install the Microsoft Visual C++ 2008 Redistributable package on all systems first, reboot, and then install the PADS 9.3.1 release. The Microsoft Visual C++ 2008 Redistributable package may be obtained from Microsoft:

<http://www.microsoft.com/downloads/details.aspx?familyid=A5C84275-3B97-4AB7-A40D-3802B2AF5FC2&displaylang=en>

- **Problem (DR 780489):** iCDB Server Manager and Monitor crashes on Uninstall scripts on Vista

Workaround: Close the iCDB Server Monitor and/or Manager before uninstalling. It may still crash, although it will be removed.

Problems Fixed

- **DR 742717**—Usertools.ini is not re-read when changing from one project to another
- **DR 627380**—Partlister arguments are order specific
- **DR 751987**—EDIF Schematic exports crashes on the attached project
- **DR 732612**—Substitute symbol crashes DxDesigner
- **DR 727597**—Some REFDES are not promoted to schematic
- **DR 729788**—DxDesigner crashes when ICT is invoked
- **DR 746792**—Can not open schematic page when Automatic Back is checked in Setup Settings
- **DR 751164**—Design is in read only mode for some reason
- **DR 746937**—Value to be character string in netlist.prp
- **DR 754303**—TERMINAL pin type causes the crash in ICT Viewer
- **DR 726421**—Import CADStar does not maintain label inversion
- **DR 743827**—PADS Logic Library to DxDesigner translation causes crash
- **DR 619479**—DxDesigner doesn't allow the user to import a LineSIM schematic containing multiple transmission lines
- **DR 744982**—Opening schematic sheet causes crash
- **DR 743833**—Cannot migrate attached project in PADS 9.2
- **DR 739327**—Getting different decals for some parts in PADS Layout
- **DR 534126**—iCDB Partlister is missing the REFDES Sort feature that was available in 2005 Architecture
- **DR 530861**—There is no possibility to change the order of field "ITEM", "QTY", and "REFERENCE"
- **DR 542505**—Line Thickness option is missing from Print dialog in PADS 2007.4
- **DR 757457**—Undesired behaviors and crash in DxDesigner 9.3 on print preview
- **DR 669046**—Offer a way to keep or not refdes during a copy between pages or between projects

- **DR 751509**—Need an icdb_admin.pdf guide tailored for PADS Flow
- **DR 721347**—DxDesigner needs a time-based autosave feature. Autobackup only saves on exit
- **DR 591611**—The WDIR search order is not used to find the netlist.prp file, and instead the file in standard folder is used
- **DR 138600**—Still no way to enable 2.0 output format in partslister
- **DR 199611**—variable field length in partlister
- **DR 220918**—Change component does not maintain refdes
- **DR 244246**—Tab delimited Partslist
- **DR 273141**—Partlister should read partliter.ini from active project or from <mentor_inst>\2005EXP\standard directory .
- **DR 323900**—Open DxDesigner project is very slow if 20 libraries are placed in the remote drive (~15 minutes)
- **DR 331689**—Want Changes made through the DxDataBook Properties dialog box saved in a file instead of registry
- **DR 374537**—Partlister should be implemented as tool to make bill of materials instead of icdb2bom
- **DR 461610**—There is no possibility to change the order of field "ITEM", "QTY", and "REFERENCE"
- **DR 461965**—Archive leaves temporary files after running
- **DR 464416**—[SilkTest] Font and color settings are ignored - defined in prp file
- **DR 487122**—Edif schematic: Schematic is not exported when sheets have different name than 1,2,3...
- **DR 501743**—Ref Designator Instance Value does not show up in EDIF netlist
- **DR 505705**—The new part lister does not allow some outputs which were possible with the previous version (EE2005.x)
- **DR 510917**—In DxDesigner offer a way to keep or not refdes during a copy between pages or between projects
- **DR 521706**—iCDBPartlister is missing the REFDES Sort feature that was available in 2005 Architecture
- **DR 572481**—Migration of hierarchical designs from PADS2007.4 to PADS 9.0 changes hierarchical net names.
- **DR 579515**—File->Print-> Range in DxDesigner only prints the first and last page
- **DR 585107**—Request ability to scale symbol in the symbol editor

- **DR 597100**—Using Undo after moving bus elements, leaves the ripper bit number in the wrong position.
- **DR 598235**—Line Thickness option is missing from Print dialog in EE2007.1
- **DR 599256**—Symbol Update fails - 'Can't load symbol file block. Symbol block is not read from iCDB.'
- **DR 599506**—Line Thickness option is missing from DxPDF dialog in EE2007.3
- **DR 623982**—Tie Dots aren't written to CCZ output from DxDesigner
- **DR 627380**—Partlister argumenst are order specific
- **DR 627765**—Documentation is needed for the commands and options that appear in the Dx Output window.
- **DR 628522**—LineSimLink Does not recognize POWER (Global) Nets
- **DR 634775**—Add new option to decide if OUT-ANALOG connections should be ignored.
- **DR 636564**—Parts Lister - need to be able to define one Ref Desg per line using standard Ref Designator in GUI
- **DR 642380**—Add Exclude Sheet command on RMB
- **DR 643328**—Standard Definition columns remain checked when a custom ipl file is opened with the columns unselected.
- **DR 643348**—Documentation: Dxdb.ini is still referenced in documentation even though it has been removed from the tool support
- **DR 654828**—Application.ActiveView.ActiveBlock.SheetSize=VDSHEET_A3_SIZE does not update the "Drawing Size" value in the GUI
- **DR 671398**—Type-o in DxDesigner User's manual page 138
- **DR 671763**—Connectivity lost on rippers when Undo is used
- **DR 677153**—Part Lister - support for variants
- **DR 677549**—Ability to setup both the RefDes start and the RefDes Suffix on a block symbol or RefDesStart and RefDes Prefix
- **DR 692022**—White objects should export as black when colors on white option used for Export PDF
- **DR 692562**—Need to document the behavior when renaming nets on the Navigator Tree as opposed to renaming nets on a sheet.
- **DR 695568**—System Scalable Font mapping option causes the misalignment of texts (properties & labels) in the pdf output than in DxDesigner.
- **DR 699135**—System Scalable Font mapping option causes symbol level property strings to appear 20-25% wider in the pdf output than in DxDesigner.

- **DR 634067**—fixed font mapping only for schematic level text.
- **DR 708365**—DxPDF ignores Scale Factor in Setup>Settings>Font Mappings, .pdf Text not scaled, does not match schematic
- **DR 710950**—The PCB Interface does not use the config file setting from the project file
- **DR 715862**—Grid On/Off button and setting is not controlled by DxDesigner.xml setting
- **DR 716163**—The wrong slot symbol is created on a new sheet in PCB Interface
- **DR 717761**—RB cannot be dissolved
- **DR 718458**—Improvement for description of Connections method (Net object)
- **DR 719142**—Hierarchical Port deleted when "/" is used in netname
- **DR 721568**—@DATETIME property remains on the design in DxDesigner2007.
- **DR 721942**—Texts change colour on white background
- **DR 722453**—PCB Interface: Wrong state of checkbox Use Custom Configuration after browsing to configuration file.
- **DR 722711**—DRC-109 issues bogus errors in 7.9.1 regarding nets not being ripped from bus. Regression from 7.9
- **DR 723475**—Using Automatically Propagate adds block name / label to underlying net when adding annotate symbol to that net
- **DR 724188**—"generic" as a selection of layout tools
- **DR 724587**—Port symbol deleting after pop / push
- **DR 725156**—Please rename option "Report extra internal or flat connection on ripped nets" for drc-121 check.
- **DR 725398**—Multi pass search seems to corrupt the database
- **DR 725904**—Running "PCLS_OK" from Dashboard toolbox fails.
- **DR 727283**—Templates require case sensitivity in the wdir path.
- **DR 727648**—"CLibPDF: Too many images: 32. Increase limits by cpdf_setDocumentLimits()." on exporting project with >31 embedded objects (OLEs) to PDF .
- **DR 728676**—EDIF Schematic Export fails with any design with named sheets
- **DR 728852**—Deleting a Block via the the Navigator window removes random Variant Unplace/Replace Modification data
- **DR 729914**—vnsd.exe remains in process list
- **DR 731022**—ODBC error, Invalid character value for cast specification on column number 1
- **DR 731203**—The "vp520.err" file is created on desktop in the machine.

- **DR 732759**—DxDesigner hangs at "Place from Schematic"
- **DR 733056**—DxD PDF does not recognize scaled Font
- **DR 733308**—Rotation of Properties is not kept after Replacing rotated part
- **DR 733556**—If the "Check for missing value" suboption of drc-401 is used, vdrc.exe will crash.
- **DR 734984**—drc-504: check that net connected to a tap has the expected Global Signal Name value
- **DR 736302**—DxDesigner should try to repair text binding to net segment on schematic open (Error 12001)
- **DR 737782**—DxDesigner hangs when a bus containing diff pairs is selected
- **DR 738427**—European Notation only correct for resistor Values
- **DR 741247**—Delete Local Symbol does not always work
- **DR 741391**—DxDesigner crashes if client A is removing port from block while client B is connecting net to the port.
- **DR 742123**—DxD going offline when updating block symbol in concurrent mode
- **DR 742205**—Case sensitivity issue in the VHDL configuration file
- **DR 742211**—Wrong bus mapping in VHDL configuration
- **DR 746307**—DxDesigner crash when using File Open Block Browse and then push on composite block within that design
- **DR 749260**—scaling translations using orcad.cnv increases the pin length
- **DR 749708**—DxDesigner behavior in graphical "line" object selection and moves
- **DR 751477**—When connecting two buses with the same name, DxDesigner crashes.
- **DR 751533**—Cross Reference if "Format Prefix" is empty and you click on "More Format Options" DxDesigner crashes
- **DR 752938**—Running DRC-121 crashes Verify
- **DR 753866**—DxDesigner Diagnostics prompt reuse block symbol update for design migrated from 2007.8 to 7.9.1
- **DR 754246**—Japanese menu problem in "Find and Replace Text" dialog.
- **DR 755372**—DxDatBook needs to support Oracle version 11
- **DR 756002**—Non understandable message in DxArchiver
- **DR 757291**—Running Packager with 'Verify' does not flag Pin Number errors but 'Package Symbols' does.
- **DR 759172**—CADStar translation shorts nets

- **DR 759542**—Bit numbers are moved so far away when increasing the space of each bus nets by using "Shift+Ctrl+Mouse Wheel".
- **DR 760262**—Unexpected connection occurs and DxDesigner crashes.
- **DR 764950**—DxDesigner crash on DxDiagnostics, runtime error , memory up to 2GB
- **DR 769769**—The PDF output, from an ICT project, fails with the message "PDF

Known Problems and Workarounds

- **DR 504235**—Preview window in Symbols addin does not display bitmaps in symbols.
Workaround: Place the symbol in the schematic to see the bitmap.
- **DR 505027**—Extract schematic - haven't got information when ports are not defined.
Workaround: Define hierarchical ports using Setup->Settings->Special Components tab before creating blocks.
- **DR 505660**—Design is translated to block while migration.
Workaround: Sometimes when a project contains multiple top-level designs after migration not all designs are created automatically. You can still do that manually in the Navigator by selecting a block (which in fact should be a design) and from the right mouse button menu select 'Create Design' option.
- **DR 508265**—vlib: Error: Unable to parse the integer token 'ffff00' from the "string. when exporting HPGL file from DxDesigner
Workaround: HPGL file can be generated on Windows platform.
- **DR 509882**—DxWebPack does not work in Windows Vista as a server.
Workaround: The path to dxdbweb.dll must be set in "ISAPI and CGI Restrictions" option on server level in IIS.

Next, DxDataBook server must be configured in DxDBConfig tool. There are two tabs: "DxDB Client Access" and "Browser Access".

"DxDB Client Access" - use this tab to choose ODBC Data Source Name and to add database aliases to chosen data source. Database aliases allow to define the set of data source names visible to DxDataBook client. After configuring this tab, it is possible to connect to DxDB Server and specified database from DxDataBook.

"Browser Access" - use this tab of DxDBConfig to specify the database configuration file that you want to use in the web extension to DxDataBook. After selecting DBC file, all tables configured in this file will be visible in explorer. It is needed to restart the web server in IIS after configuring the DxDBConfig. After restarting, It is possible to connect to DxDB web server from DxDataBook and from explorer.

- **DR 673417**—The "Substitute symbol(s)" option may not work properly if there is a "sym" folder in project folder.
Workaround: Delete or rename the sym folder if it is possible.

-
- **DR 685731**—DxD crashes on exit

Workaround: working script should be terminated prior to closing DxDesigner to avoid crash.

Problems Fixed

- **DR 560598**—HyperLynx Analog should accept variable parameter values
- **DR 728874**—Subckt name is incorrect in the Hspice netlist generated by Spicelink
- **DR 728880**—Model parameters missing in Hspice netlist generated by Spicelink
- **DR 728883**—Junk characters and comments are added at the beginning of some instance names in Hspice netlist generated by Spicelink
- **DR 641822**—Spice primitive resistor should not have TC3 property when HLASE simulator is set
- **DR 654604**—When I enter a PHASE value in the SpicePrimitive:v_sin source, the resultant sine wave in the simulation does not shift over in the transient simulation
- **DR 672762**—Document ADMS versions that are compatible with Hyperlynx Analog
- **DR 686494**—HLA should include the subcircuit referenced by another subcircuit
- **DR 692536**—HLA should accept variable parameter values
- **DR 728716**—AMS2010.2 support

Known Problems and Workarounds

- **DR 719006**—Generics not managed properly with block multi-instantiation
Workaround: Change design methodology. To create a block with a different name if there is a need to use different generics in one of the blocks.

Problems Fixed

- **DR 748869**—Crash for specific signal (during unravel)
- **DR 274676**—Error when the Xilinx pin file name is .PAD (instead of .pad)
- **DR 605410**—IOD 7.4 not allowing assignments from Quartus II 9.0, QSF file, for differential pairs.
- **DR 614855**—Net Name Delimiter setting is not used
- **DR 614950**—IOD 8.0 Does not recognize the "use ieee.std_logic_misc.all;" line in VHDL files
- **DR 692612**—Import/Export of Quartus 9.1 QFS constraints file into/out-of IOD is corrupting the constraints file
- **DR 721114**—Unable to generate schematic sheets with custom border.
- **DR 730724**—IOD crashes (iod_dx.exe), when attempting to import symbols
- **DR 731381**—Crash during updating .fpc using .pin file
- **DR 745410**—Customer needs to use devices not yet included into the tool library
- **DR 750587**—Bad allocation error when attempting to open FPC database in IOD.
- **DR 752733**—lpc is not supported in WG but message about license is displayed
- **DR 765282**—DIFFCLOCK type unavailable for specific pin/pins
- **DR 766126**—Customer requires FPGA device

Known Problems and Workarounds

- **dts0100472491**—Symbol pins are out of grid after schematic and symbols export to DxD in case of different grid settings.
Workaround: Please ensure the same grid settings between DxDesigner and I/O Designer before symbol's creation in I/O designer.
- **dts0100511732**—IOD fails to read in Quartus generated xChange file
Workaround: Change\use for all those IO standard names only upper case letters.
- **dts0100637000**—IOD no responding for 12 min after select all pins (cross probing on)
Workaround: Don't select large number of pins if cross probing is turned on.

- **dts0100644719**—Not valid error message is displayed and layout is not shown after saving scheme
Workaround: Reload database
- **dts0100670942**—[Symbols Generator] If symbols are created with Flat design type then there should be no warning about signals not placed on functional symbol.
Workaround: Please ignore the warnings
- **dts0100679922**—[Symbols Generator] Hierarchical connection broken after create/update symbols.
Workaround: It is highly recommended to re-create symbols with new Symbols Generator instead of using symbols created in older IOD versions in order to avoid such problems.
- **dts0100681038**—IOD does not use HDL signal name during resizing bus
Workaround: After resize do following steps:
 1. Start Signal "Rename" and change existing "HDL name" to any other name. Accept change
 2. Start Signal "Rename" again and change to required value. Accept change
- **dts0100683321**—[Symbols Generator] For databases with old symbols, duplicated pins can occur on symbols after SG is run to create symbols
Workaround: Recreation of all symbols with new SG does not give the effect and no duplicated pins are created.
- **dts0100684754**—Assignment is not restored after extending bus and undo
Workaround: Restore assignment manually
- **dts0100767099**—Borders are not placed when was not already used in DxD schematic
Workaround: Open DxD, insert border you want to be generated by IODesigner on any schematic and then remove placed border. Export schematic from IOD to DxD again. Now border is properly placed
- **dts0100769440**—Diff buses on functional symbol are wrongly updated after rerange
Workaround: Delete symbols and generate new set of symbols
- **dts0100634294**—IOD exports broken schematic. Functional block is empty.
Workaround: Functional symbols' names should be different than design name as it causes problems in IOD-DxD integration.
- **dts0100716494**—Update Power Signal doesn't delete power signal which are not needed
Workaround: Delete all power signals and run Update Power Signals again.
- **dts0100716742**—I cannot recreate symbols with the same settings until I remove all of my symbols before.
Workaround: Please remove all symbols before you create them.
- **dts0100718856**—Builtins are placed improperly from time to time - no connection on IOD generated schematic. Package failed in DxD.

Workaround: Export schematic once again from I/O Designer - after second and further exports builtins are connected properly.

- **dts0100720675**—It's possible to lock only one element of diff signal.

Workaround: To lock differential signal please select its parent.

- **dts0100722155**—During apply scenario there are assignment errors and it is caused by unravel with 'Use unused pins'.

Workaround: In FPGA database set swap group for all unassigned pins to empty

Chapter 5

PADS Logic and PADS Layout

Known Problems and Workarounds

- **Problem:** When importing an ECO file in PADS Layout 9.3.1, imported values are not recalculated according to the current design units. As a result, the import may end with wrong data and without warning. The issue exists when performing an ECO import in PADS Layout or using ECO to PCB in PADS Logic.

Workaround: Before importing an ECO file, make sure the design units are set the same in the ECO file as in the design. You can check the design units in the ECO file header.

Problems Fixed

- **DR 709338**—Incorrect default rules are passed from Logic to Layout
- **DR 736135**—RefDes are shown separately for components which are having same part types.
- **DR 743939**—bug in the Update From Library code - this feature has internal limit for updated part types count - 100, if a design has more Pads Logic crash
- **DR 744114**—Database corruption created with null ref des and blank pin numbers when part contains pins defined as 1-1, 1-2, etc
- **DR 746250**—Value attribute and free label placeholder identified as different between library and schematic
- **DR 747747**—Net \$\$\$3274 appears connected to +3.3V by virtue of tie dot, but remain two separate nets
- **DR 753785**—In Logic, Setup>Design Rules, Class Rules, V9.3 hides Available nets when Classes are created or v9.2 schematic is save within V9.3.

Problems Fixed

- **DR 754762**—DxDesigner Link doesn't highlight some hierarchical nets in PADS Layout
- **DR 750600**—ECO failure when ECO from PCB is performed (MAX_SEPARATION_DISTANCE)
- **DR 726564**—Silkscreen REFDES, Assembly REFDES, Part Number is not translating properly
- **DR 748514**—Remove IDF from the Import List when the user is not licensed for it
- **DR 726512**—PCB Decals translated from CADSTAR V8 have placement outline coming in on Assy Dwg Top - should be on Layer 20
- **DR 736996**—Bad suffix on number for Protel translation
- **DR 748891**—Samples folder is not created in PADS Project folder
- **DR 763175**—Incorrect Expedition layers generated from PADS
- **DR 774884**—Unable to create ODB++ file from design
- **DR 777509**—Fatal Error when exporting ODB output
- **DR 777803**—ODB++ file missing holes in oval pads
- **DR 742263**—On-the-fly Drill Drawing Data is not output in ODB++ output
- **DR 770309**—ODB++ export Fatal error generated
- **DR 754751**—ODB++ output from PADS 9.3 generates fatal error and fails
- **DR 746385**—Export ODB++ - *.odb format is not a general format, *.tgz is a common format
- **DR 719551**—Pads that have associated copper are not coming out round shapes on solder mask and paste mask layers when aperture macros are enabled, they are hexagon.
- **DR 723761**—File->Save As... does not save to the location from which the design was opened
- **DR 726149**—Fatal Runtime Error when exiting Layer Filter
- **DR 735102**—Display Color, net name visibility effects routing layer.
- **DR 735827**—Unable to open attached design into PADS Layout.

- **DR 735933**—Corrupt File - PADS Layout causes a fatal run-time error, and closes when an attempt is made to Via Stitch a plane.
- **DR 738778**—Terminal which is associated with copper will appear as default in ‘CAM Preview’ in 2007 version. Whereas it’s broken in later versions.
- **DR 740792**—RefDes of Jumper will resets its position when we run Tools > Verify > Verify Test points.
- **DR 744219**—Demo-Mode operation should be fully functional under a database limit. That has changed in 9.3 and some strange subsets now result.
- **DR 744755**—Absolute and relative moves in Macros are not functioning correctly
- **DR 746023**—Does not set a "Step and Repeat" on Japanese.
- **DR 746704**—Menu/Toolbar area background color appears in blue (always used to be grey).
- **DR 746776**—quick measure inaccuracy
- **DR 746812**—Crash occurs when using the Change Component command with Update Part Type from Library enabled for a decal with 40 characters in the library.
- **DR 748345**—Does not output Associate PAD.
- **DR 749098**—Process Status dialog in Compare/ECO Tool closes immediately after Run
- **DR 749867**—Regression: Negative pad offset values creates false errors about thermal line width being out of range when copying and pasting the part
- **DR 751319**—Does not work Design Rules in Japanese.
- **DR 753078**—Creating a new CAM Directory using the Browse forces users to select File not Directory to work.
- **DR 753238**—Flip Horizontal and Flip Vertical are reversed for a copied pin pair
- **DR 753810**—V9.3 DEMO Plane Connect does not function.
- **DR 754300**—Regression: Planes and Copper Pour can be selected using CTRL + A even though all the layers are not selected from the filter.
- **DR 754763**—Keepout shapes are not output in PDF when using Create PDF.
- **DR 755331**—fatal error when creating CQFP in wizard
- **DR 757408**—System Default Start-up File, Dimensioning Precision is set to Zero.
- **DR 758325**—Layout crashes while using ECO Change Component with "update from Library" checked with specific part Type name, 40 characters in length
- **DR 760854**—Create PDF - Cannot output circle with correct size.
- **DR 761658**—Some large setting widows of PADS Logic and PADS Layout, can not be fit in Windows 7.

- **DR 763312**—OK, Cancel and Help buttons are not visible in DXF Import menu of Decal Editor.
- **DR 765374**—CAM Preview incorrect w/ CAM plane when terminal uses Oval pad shape w/ custom thermal
- **DR 776038**—"Pads Layout switch to Router crashes 100% Design 12 Layer, 500mm x 450 mm Burn in Board with 17000 Parts, 35000 connections"

Known Problems and Workarounds

- **DR 781414**—Library dropdown is not refreshed in Layout/Logic after you synchronize library settings from the other application.
Workaround: After doing changes in Library List in Logic (or Layout) with "Synchronize with PADS Layout (or Logic)" option turned on, you need to open Manage Lib List window in Library Manager and click OK to have library list order correctly refreshed. Library lists are also correctly refreshed after restarting application.
- **Problem:** ODB++ export does not support designs with teardrops
Workaround: In the current release, exporting to ODB++ does not support designs with teardrops. Please, do not use ODB++ export for exporting designs that use teardrops or disable teardrops if you want to export to ODB++.
- **Problem** (DR 778986): Allegro to PADS translator fails to open when UAC is enabled on Windows 7
Workaround: Do not install PADS 9.3.1 to the Program Files location if you are using UAC, or turn UAC off

Problems Fixed

- **DR 567656**—When manually routing net \$\$\$19562 it stops at the border of the keepout. When I pass by the corner of the keepout it smooths the trace and places it right across the keepout.
- **DR 631678**—Router moves a protected pinpair/diffpair. This is a regression from PADS2007.
- **DR 639684**—Errors created when reloading BRE file of routed board: Copper of net <XXXX> does not have an adjacent edge
- **DR 684088**—"Integrity Test Error: Profile of net SDA4_01 has non-correct geometry"
- **DR 689700**—hangs at various stages of auto-routing, and finally crashes with a Fatal run-time error.
- **DR 695879**—PADS 9.2 RC2: Getting message 'Can't switch to joint mode' when I route differential pairs.
- **DR 697181**—Crash on placing a via with SHIFT+Mouseclick
- **DR 707361**—Tool will crash when I try to open attached design file.
- **DR 712970**—Autorun hangs at 85-90%
- **DR 717394**—Unable to get Diff Pair traces to join together in the location desired
- **DR 721666**—Heavy lag when attempting to interactively route Diff pair through BGA
- **DR 728592**—Fatal Runtime Error in Router when running AutoRouting
- **DR 730375**—Design crashes when entering Edit->Properties
- **DR 740769**—Router crashes with a layout file (click home on kb).
- **DR 741100**—Router re-routed straight Diff pair traces into ones with 90 degree angles after vias were added
- **DR 741258**—File hangs at 75% when loading it into Router
- **DR 741320**—Router does not display diff pair gap when routing separately. Router will not continue routing diff pairs.
- **DR 742173**—Traces route all over the place.
- **DR 743291**—Router Crashes loading BRE file

- **DR 747215**—Fatal Runtime error when moving component with Check Violations during Move enabled.
- **DR 750242**—PCB design crashes when loading into PADS Router if net names are enabled in Display Colors.
- **DR 755719**—PADS Router crashes repeatedly
- **DR 757131**—Tool crashes when I try to open attached design in PADS Router.
- **DR 774967**—Pads router is not respecting route keepout.

System Requirements

Microsoft .NET Framework Version 2.0

LP Wizard requires Microsoft .NET Framework Version 2.0 to function. You must install Microsoft .NET Framework 2.0 before or after installing the LP Wizard software. Later versions of Microsoft .NET Framework (v3.0, v4.0) are not compatible.

Problems Fixed

CAD Export

- **DR 708517**—LP Wizard's license checking routine spams server debug log with "Unsupported" messages.
- **DR 710547**—Export to CAD - Allegro in Inches creates incorrect files. does not build Land Pattern
- **DR 724292**—Incorrect rotation for Lands On Assembly for Allegro
- **DR 739221**—Expedition CAD Output/XCAM Still does not work for PacRim
- **DR 745878**—Thermal TAB for both SMT QFN's and SON's no longer build in Allegro - works in V10.1.1
- **DR 746490**—Allegro .pad file ERROR when using Rounded Corners (shape symbol script) to create a chip resistor land pattern.
- **DR 746588**—QFN Silkscreen in Land Patterns is generated wrong for Allegro 16.3 - all corners 90 degrees off.
- **DR 746757**—CAD Output for Allegro 16.3 EXTENTS issue has re-emerged
- **DR 748117**—CAD Output for Allegro broken for LP V10.3 and V10.2.1 - will not complete
- **DR 748197**—LP V10.3 Expedition CAD Output Error during *_Cell.hkp file Import
- **DR 749533**—Silkscreen and Assy outlines not correct in OrCAD from LP Wizard 10.3
- **DR 752081**—'Percentage of height' value is ignored
- **DR 752957**—Export of SOIC (maybe others) for P-CAD is bad
- **DR 756058**—Silkscreen cutout on radial LED incorrect.

- **DR 756064**—Circle on layer 20 for courtyard (placement area) is incorrectly filled
- **DR 757292**—Duplicate labels on exported footprints
- **DR 758029**—Remove Layer_25 in PADS Padstack
- **DR 766549**—SAMTEC connector output is not properly centering/spacing pins from origin resulting in unusable data
- **DR 769919**—JEDEC reference not correct for BGA Land Pattern BGA100C100P10X10_1100X1100X170
- **DR 771353**—Geometry height is exported to Allegro Script even though the attribute is disabled in Wizard properties
- **DR 773777**—Unable to open geometries generated by the LP Wizard for Allegro 15.7

Calculator

- **DR 743411**—LP Printable datasheet have mis-matched dimension references from Figures to Tables
- **DR 750191**—Connector calculator uses incorrect value for height value in name.
- **DR 750477**—Dimensions "d" and "T" are missing from the component column of the print sheet for the Connector - Header
- **DR 750873**—Axial Family, horizontal mount courtyard is mapping the nominal body
- **DR 751450**—The calculator does not create padstacks that match the IPC padstack tables on your website.
- **DR 752655**—Manually adding Fiducials in the BGA calculator does not override Global setting on-the-fly
- **DR 757006**—LP Calculator is producing an incorrect Mounting Hole Padstack Name
- **DR 757027**—Aluminum Electrolytic Capacitor component family silkscreen on 3.30 mm library parts are coming out incorrect

Changes and Enhancements

Calculator

- **DR 710274**—Request that the Complete Software Version be identified for LP Wizard output files
- **DR 710571**—Exit button doesn't ask if you want to save changes

Known Problems and Workarounds

- **Problem:** The LGA “preferences” for placement courtyard do not match the IPC-7351B standard for a 1.0 mm courtyard excess.

Workaround:

- a. Open the Preferences menu
- b. Select the SMT component family LGA
- c. Select the User option
- d. Change all 2.0 and 0.5 placement courtyards to 1.0
- e. Save and Close preferences

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