



CBM2091

Datasheet

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Contents

1	DESCRIPTION	1
2	FEATURES	1
3	BLOCK DIAGRAM	3
4	PIN ASSIGNMENT	4
4.1	TQFP48 (TOP SIDE)	4
4.2	LQFP64 (TOP SIDE)	5
5	PIN DESCRIPTION.....	6
6	ELECTRICAL CHARACTERISTICS	10
6.1	ABSOLUTE MAXIMUM RATINGS	10
6.2	RECOMMENDED OPERATING CONDITIONS	10
6.3	STATIC CHARACTERISTICS.....	10
6.4	DYNAMIC CHARACTERISTICS	11
7	TYPICAL APPLICATION.....	13
8	MECHANICAL DIMENSIONS.....	14
8.1	48-PIN CBM2091 PACKAGE OUTLINE DIMENSION	14
8.2	64-PIN CBM2091 MODE PACKAGE OUTLINE DIMENSION	15
9	COPYRIGHT NOTICE.....	16

1 Description

Fastest & Securest USB 2.0 Flash Disk Controller with dedicated 32-bit microprocessor

The CBM2091 is the USB 2.0 Flash Disk controller with the fastest transfer speed on the market. CBM2091 can reach theoretical flash access **speed limit of over 32MByte/s for read and 20MByte/s for write.**

The on-the-fly ECC engine is capable of correcting up to 4bytes (32bits), detect 5 or more bytes errors per 528bytes page . For data security, CBM2091 is designed with both hardware and software data protection technology to prevent data corruption even if it is powered off or unplugged during data transfer.

The CBM2091 supports all 8 bit and 16 bit NAND/MLC/AG-AND flash memory available in the market. New flash can be supported by software re-configuration. It also supports SPI NOR flash without extra components needed.

The CBM2091 has both a) 5V to 3.3V LDO and b) power on reset circuits integrated. Thus greatly reduced BOM cost and eased layout burden.

The CBM2091 runs smoothly with all available hosts and PC platforms. Complied with USB specification rev. 2.0, the CBM2091 can be supported without additional driver under Win XP, Win 2000, Windows Me, Mac OS and Linux OS. With device driver installed, it can support Win 98/98SE as well. Comprehensive applications, such as PC boot up, disk partitions, password check for security disk, are available as part of our standard mass production software package.

The CBM2091 is available in 48-pin TQFP and 64-pin LQFP package, which are thinnest and smallest on the market. The 48-pin CBM2091 supports up to 4 flash chips and the 64-pin CBM2091 supports up to 8 flash chips. Customers can choose different packages to meet their design requirement.

2 Features

■ **USB Interface**

High-speed USB 2.0 interface;

■ **Fastest data transfer rate on the market**

Dual-channel mode: 32MB/s for Read, 20MB/s for Write
Single-channel mode: 17MB/s for Read, 16MB/s for Write
Fastest file copy rate on the market.

■ **On-the-fly ECC built-in Hardware enhances reliability**

ECC for Binary NAND flash: 4-32 bit/page (1 page = 528 bytes)
ECC for MLC NAND flash: 8-32 bit/page
ECC for AG-AND flash: 8-32 bit/page

■ **Special wheel leveling algorithm to improve the flash life-time**

■ **Hardware & Software Data Protection Technology**

Prevent data corruption even if it is powered off or unplugged during data transfer.

■ **NAND, AG-AND & MLC Flash Interface**

Support 4k page flash parallel mode.
Support 8-bit and 16-bit Samsung SLC and MLC NAND flash.
Support 8-bit and 16-bit Toshiba SLC and MLC NAND flash.
Support 8-bit and 16-bit Hynix SLC and MLC NAND flash.
Support 8-bit and 16-bit ST Microelectronics SLC and MLC NAND flash.
Support 8-bit and 16-bit Micron/IM SLC and MLC NAND flash.
Support 8-bit and 16-bit Inferion SLC and MLC NAND flash.
Support 8-bit and 16-bit Sandisk SLC and MLC NAND flash.
Support Renesas AG-AND and AND flash memories
Support Actrans flash memories
Support SPI Nor flash without extra components needed
Software configuration to support various new flash memories
Supports up to 8 flash chips.

■ **Proprietary 32-bit CISC microprocessor feature**

Proprietary 32-bit CISC processor for USB protocol processing and flash access.
Single cycle instruction period

■ **Integrated 5v to 3.3v voltage regulator**

■ **Disk partitions and password check for security disk available**

■ **PC boot up as USB Zip Disk, USB Hard Disk or CDROM**

■ **Auto run function**

■ **Low power dissipation**

Operating current 50mA (Bus power compatible)

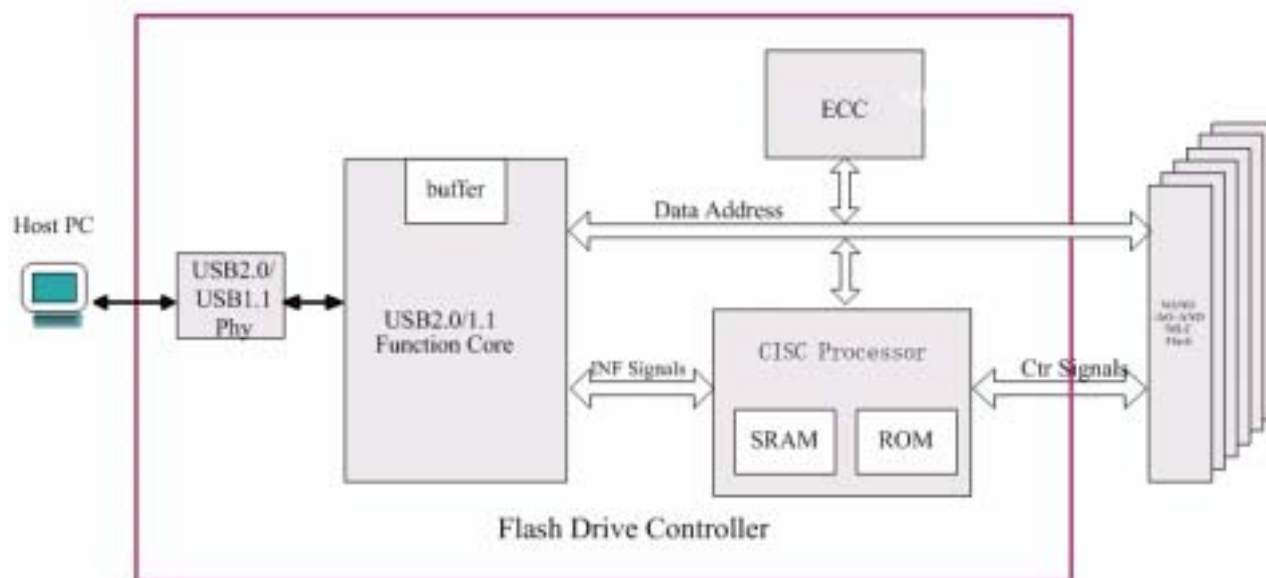
■ **Leading 0.18um CMOS technology**

■ **48-pin TQFP /64-pin LQFP package**

48-pin CBM2091 supports up to 4 Flash Chips
64-pin CBM2091 supports up to 8 Flash Chips

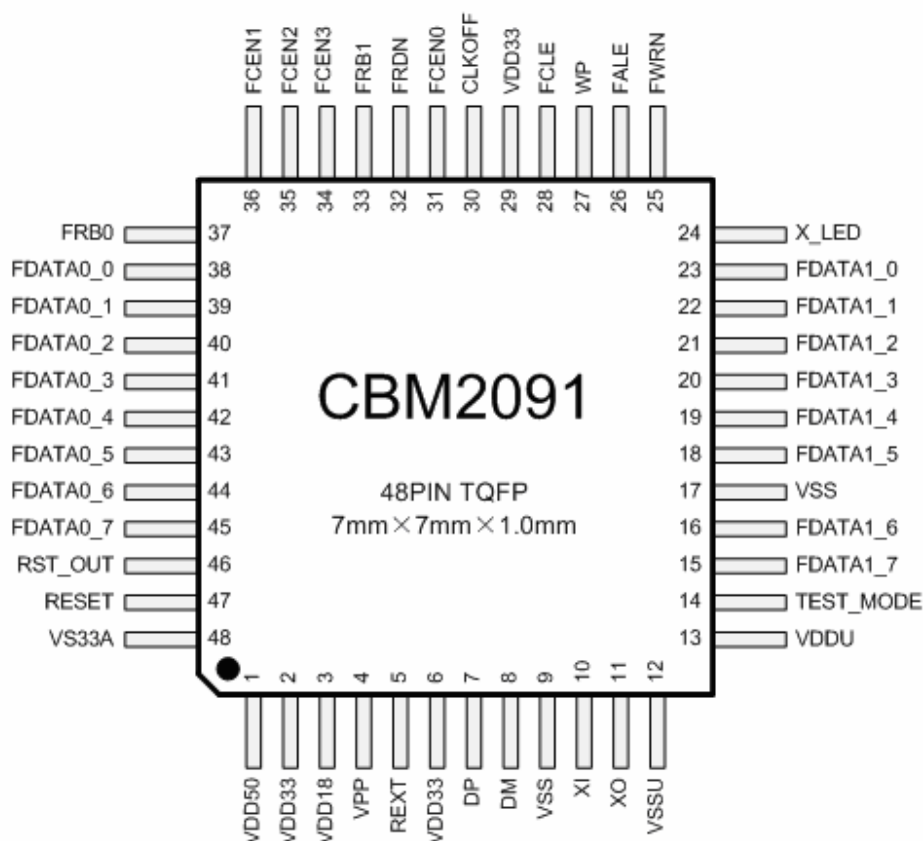
■ **Windows, Mac and Linux compatible**

3 Block Diagram

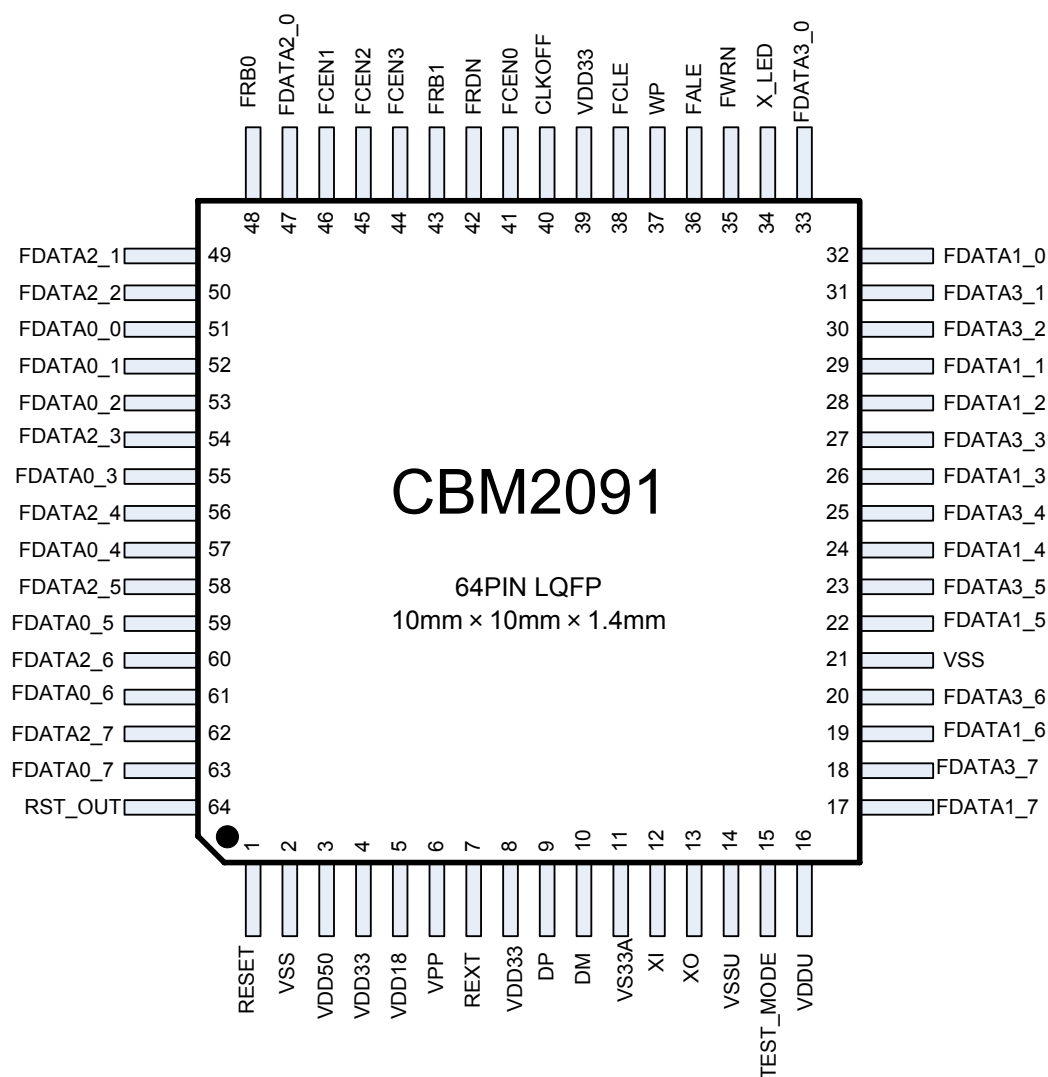


4 Pin Assignment

4.1 TQFP48 (Top Side)



4.2 LQFP64 (Top Side)



5 Pin Description

Brief CBM2091 pin functions are shown in the following tables.

I : Input signal
O : Output signal
I/O : Bi-direction signal
PWR : Power signal
GND: Ground signal
PU: pull up
PD: pull down

CBM2091 LQFP64 / TQFP48 Pin Description

LQFP64 Pin No.	TQFP48 Pin No.	Pin Name	Type	Description
3	1	VDD50	PWR	Regulator 5V Power Input
4	2	VDD33	PWR	Regulator 3.3V Power OUT
5	3	VDD18	PWR	Regulator 1.8V Out
6	4	VPP	I	Inner Programme
7	5	REXT	I	Connect External Resister for current reference
8	6	VD33	PWR	Padding 3.3V Power
9	7	DP	I/O	USB Data D+
10	8	DM	I/O	USB Data D-
2	9	VSS	GND	Padding 3.3V / Logic 1.8V Ground
12	10	XI	I	Crystal Input (12 MHz)
13	11	XO	O	Crystal Output
14	12	VSSU	GND	Analog 1.8V Ground
15	13	VDDU	PWR	Analog 1.8V Power
16	14	TEST_MODE	I PD	Test Mode Enable Pin When high , test mode When low , normal mode
17	15	FDATA1_7 GPIO15	I/O PU	Group 1 Flash Data Bus - bit 7 General I/O port 15 When select spi mode ,as spi chip select .

				(configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select master mode , configure output , otherwise, configure as input.).
19	16	FDATA1_6 GPIO14	I/O PU	Group 1 Flash Data Bus - bit 6 General I/O port 14 When select spi mode, as clock out support ligh-tun sensor (configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select ligh-tun mode , configure output).
21	17	VSS	GND	Padring 3.3V / Logic 1.8V Ground
22	18	FDATA1_5 GPIO13	I/O PU	Group 1 Flash Data Bus - bit 5 General I/O port 13
24	19	FDATA1_4 GPIO12	I/O PU	Group 1 Flash Data Bus - bit 4 General I/O port 12
26	20	FDATA1_3 GPIO11	I/O PU	Group 1 Flash Data Bus - bit 3 General I/O port 11
28	21	FDATA1_2 GPIO10	I/O PU	Group 1 Flash Data Bus - bit 2 General I/O port 10
29	22	FDATA1_1 GPIO9	I/O PU	Group 1 Flash Data Bus - bit 1 General I/O port 9
32	23	FDATA1_0 GPIO8	I/O PU	Group 1 Flash Data Bus - bit 0 General I/O port 8
34	24	X_LED	I/O	When TEST_MODE =1, as scan clock input. When TEST_MODE =0, as LED Indication
35	25	FWRN	O	Group Flash Write Enable (active low)
36	26	FALE	O	Group Flash Address Latch Enable
37	27	WP	I	Write Protect Switch Input
38	28	FCLE	O	Group Flash Command Latch Enable
39	29	VDD33	PWR	Padring 3.3V Power
40	30	CLKOFF	I PD	Clock input switch. CLK_OFF=1, select external test clock.
41	31	FCEN0	O	Flash Chip Enable - Chip 0 (active low)
42	32	FRDN	O	Group Flash Read Enable (active low)
43	33	FRB1 /SYNC_F /INTR	I	Group Flash Ready_Busy 1, when select spi mode ,as light-tun frame sync signal. 2, when select flash_rb1 mode, as Group Flash Ready_Busy1 signal input(detail in soft_flag [30]). 3, when select intr mode, as external interrupt input signal(detail in soft_flag [30]).
44	34	/SCK(I2c) /MOSO FCEN3	O	1, When select test-mode, as scan-chain output 2, When select i2c , as sck

				3, When select spi_en, as master/slave output data 4, When select chip select2/3 mode, as CE3 output
45	35	FCEN2 /MIS1	I/O PU	1, When select test_mode, As scan-chain input 2, when select chip select2/3 mode, as CE2 output .(active when disable test_mode) 3, When deselect test_mod and chip-select2/3 mode , as spi master/slave data input .at same time, need set spi_en bit
46	36	X_CLK_OUT /FCEN1 /MCLK_OUT /SCLK	I/O PU	1, When select clock input mode (X_CLK_OFF =1 or select spi slave mode), (1), X_CLK_OFF=1, as external input test clock. (2), select spi slave mode , as spi slave SCLK input 2, When select chip select1 mode or spi master mode, as output. (only active when X_CLK_OFF =0 or de-select spi slave mode) (1), select spi master mode, as spi master clock output (2), select chip select1 mode (detail in soft_flag [30]), as CE1 output (3), otherwise, as normal clock_out ,which defined at config_r[20].
48	37	FRB0	I	Group Flash Ready_Busy0
51	38	FDATA0_0 GPIO0	I/O PU	Group 0 Flash Data Bus - bit 0 General I/O port 0
52	39	FDATA0_1 GPIO1	I/O PU	Group 0 Flash Data Bus - bit 1 General I/O port 1
53	40	FDATA0_2 GPIO2	I/O PU	Group 0 Flash Data Bus - bit 2 General I/O port 2
55	41	FDATA0_3 GPIO3	I/O PU	Group 0 Flash Data Bus - bit 3 General I/O port 3
57	42	FDATA0_4 GPIO4	I/O PU	Group 0 Flash Data Bus - bit 4 General I/O port 4
59	43	FDATA0_5 GPIO5	I/O PU	Group 0 Flash Data Bus - bit 5 General I/O port 5
61	44	FDATA0_6 GPIO6	I/O PU	Group 0 Flash Data Bus - bit 6 General I/O port 6
63	45	FDATA0_7 GPIO7	I/O PU	Group 0 Flash Data Bus - bit 7 General I/O port 7
64	46	RST_OUT	O	Chip reset output/ External device reset signal Low active pulse output Should connect with RESET pad
1	47	RESET	I	Reset Sign (active low)
8	48	VS33A	GND	Analog 3.3V Ground
47		FDATA2_0	I/O PU	Group 2 Flash Data Bus - bit 0 General I/O port

49		FDATA2_1	I/O PU	Group2 Flash Data Bus - bit 1 General I/O port
50		FDATA2_2	I/O PU	Group 2 Flash Data Bus - bit 2 General I/O port
54		FDATA2_3	I/O PU	Group 2 Flash Data Bus - bit 3 General I/O port
56		FDATA2_4	I/O PU	Group 2 Flash Data Bus - bit 4 General I/O port
58		FDATA2_5	I/O PU	Group2 Flash Data Bus - bit 5 General I/O port
60		FDATA2_6	I/O PU	Group 2 Flash Data Bus - bit 6 General I/O port
62		FDATA2_7	I/O PU	Group 2 Flash Data Bus - bit 7 General I/O port
33		FDATA3_0	I/O PU	Group 3 Flash Data Bus - bit 0 General I/O port
31		FDATA3_1	I/O PU	Group 3 Flash Data Bus - bit 1 General I/O port
30		FDATA3_2	I/O PU	Group 3 Flash Data Bus - bit 2 General I/O port
27		FDATA3_3	I/O PU	Group 3 Flash Data Bus - bit 3 General I/O port
25		FDATA3_4	I/O PU	Group 3 Flash Data Bus - bit 4 General I/O port
23		FDATA3_5	I/O PU	Group 3 Flash Data Bus - bit 5 General I/O port
20		FDATA3_6	I/O PU	Group3 Flash Data Bus - bit 6 General I/O port When select spi mode, as clock out support ligh-tun sensor (configure as GPIO and set pin_64(detail in spi_ctl[13] .when select ligh-tun mode , configure output).
18		FDATA3_7	I/O PU	Group 3 Flash Data Bus - bit 7 General I/O port When select spi mode ,as spi chip select . (configure as GPIO and set pin_64(detail in spi_ctl[13] .when select master mode , configure output , otherwise, configure as input.).

6 Electrical Characteristics

6.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions	min	max	unit
VCCA	analog supply voltage		-0.5	5.5	v
VCCD	digital supply voltage		-0.5	4.5	v
VI	input voltage		-0.5	5.5	v
Vesd	electrostatic discharge voltage[1]	ILI < 1 A			v
		DP, DM and GND pins	-4000	+4000	
		other pins	-2000	+2000	
Tstg	storage temperature		-40	+125	

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k Ω resistor (Human Body Model).

6.2 Recommended operating conditions

symbol	Parameter	conditions	min	Typ	max	Unit
VCCA	analog supply voltage		3.0	3.3	3.6	V
VCCD	digital supply voltage		3.0	3.3	3.6	V
VI	input voltage		0	-	VCCD	V
VI(AI/O)	input voltage on analog I/O pins DP DM	Low/Full speed	0	3.3	3.6	V
		High speed	0	400	-	mV
Tamb	ambient temperature		0	-	+70	

6.3 Static characteristics

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V; Tamb = 40 to 85 $^{\circ}$ C;

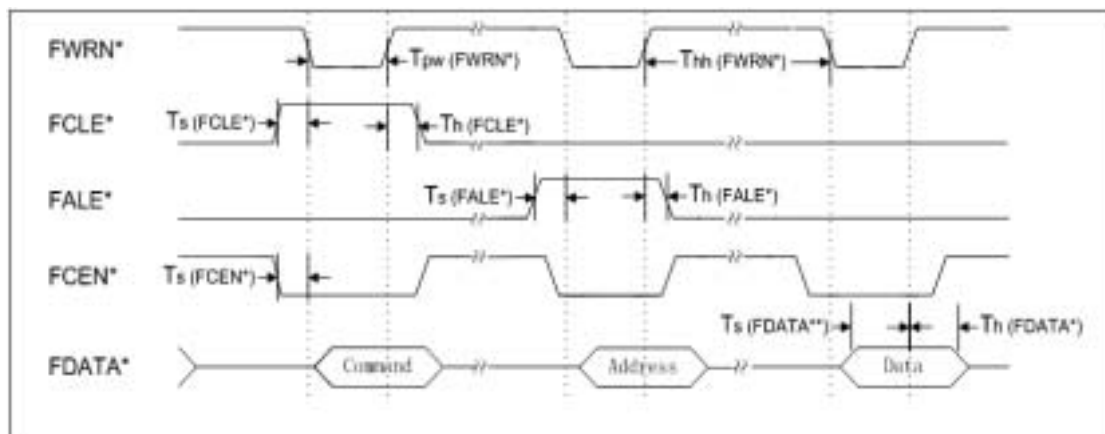
symbol	Parameter	Conditions	min	Typ	max	Unit
ICC	operating supply current	Full-speed transmitting and receiving;	-	29.5	-	mA
		high-speed transmitting and receiving	-	50		
ICC(susp)	suspend supply current	in suspend mode	-	500		μ A

6.4 Dynamic characteristics

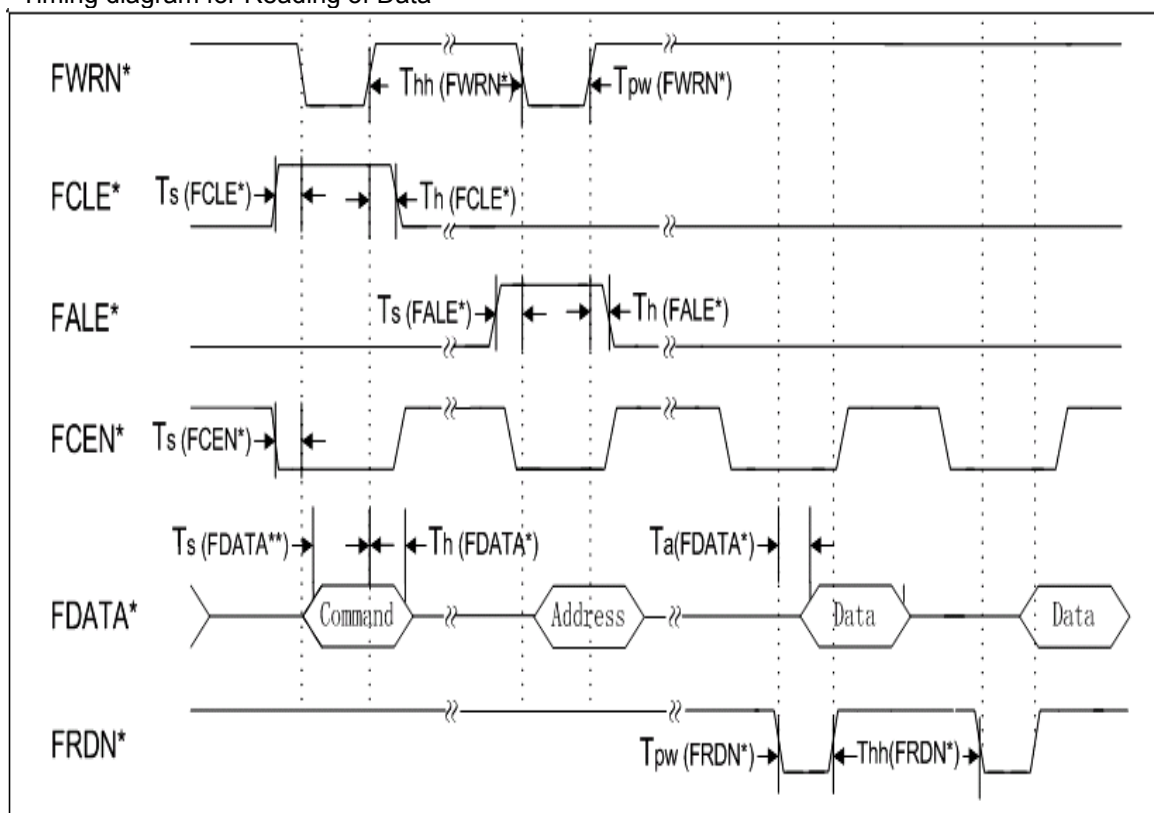
All parameters are measured at $V_{CCA} = V_{CCD} = 3.0$ to 3.6 V; $V_{AGND} = V_{DGND} = 0$ V; $T_{amb} = 40$ to 85 °C;

symbol	Parameter	conditions	min	Typ	max	Unit
$T_s(FDATA^*)$	FDATA* setup time relative to rising FWRN* edge		-	33	-	ns
$T_h(FDATA^*)$	FDATA* hold time relative to falling FWRN* edge		-	33	-	ns
$T_s(FCLE^*)$	FCLE* setup time relative to falling FWRN* edge		-	33	-	ns
$T_h(FCLE^*)$	FCLE* hold time relative to rising FWRN* edge		-	33	-	ns
$T_s(FALE^*)$	FALE* setup time relative to falling FWRN* edge		-	33	-	ns
$T_h(FALE^*)$	FALE* hold time relative to rising FWRN* edge		-	33	-	ns
$T_s(FCEN^*)$	FCEN* setup time relative to falling FWRN* edge		-	99	-	ns
$T_{pw}(FWRN^*)$	FWRN* Pulse Width		-	33	-	ns
$T_{hh}(FWRN^*)$	FWRN* high hold time		-	33	-	ns
$T_a(FDATA^*)$	FDATA* access time relative to falling FRDN* edge		-	-	40	ns
$T_{pw}(FRDN^*)$	FWRN* Pulse Width		-	33	-	ns
$T_{hh}(FRDN^*)$	FWRN* high hold time		-	33	-	ns

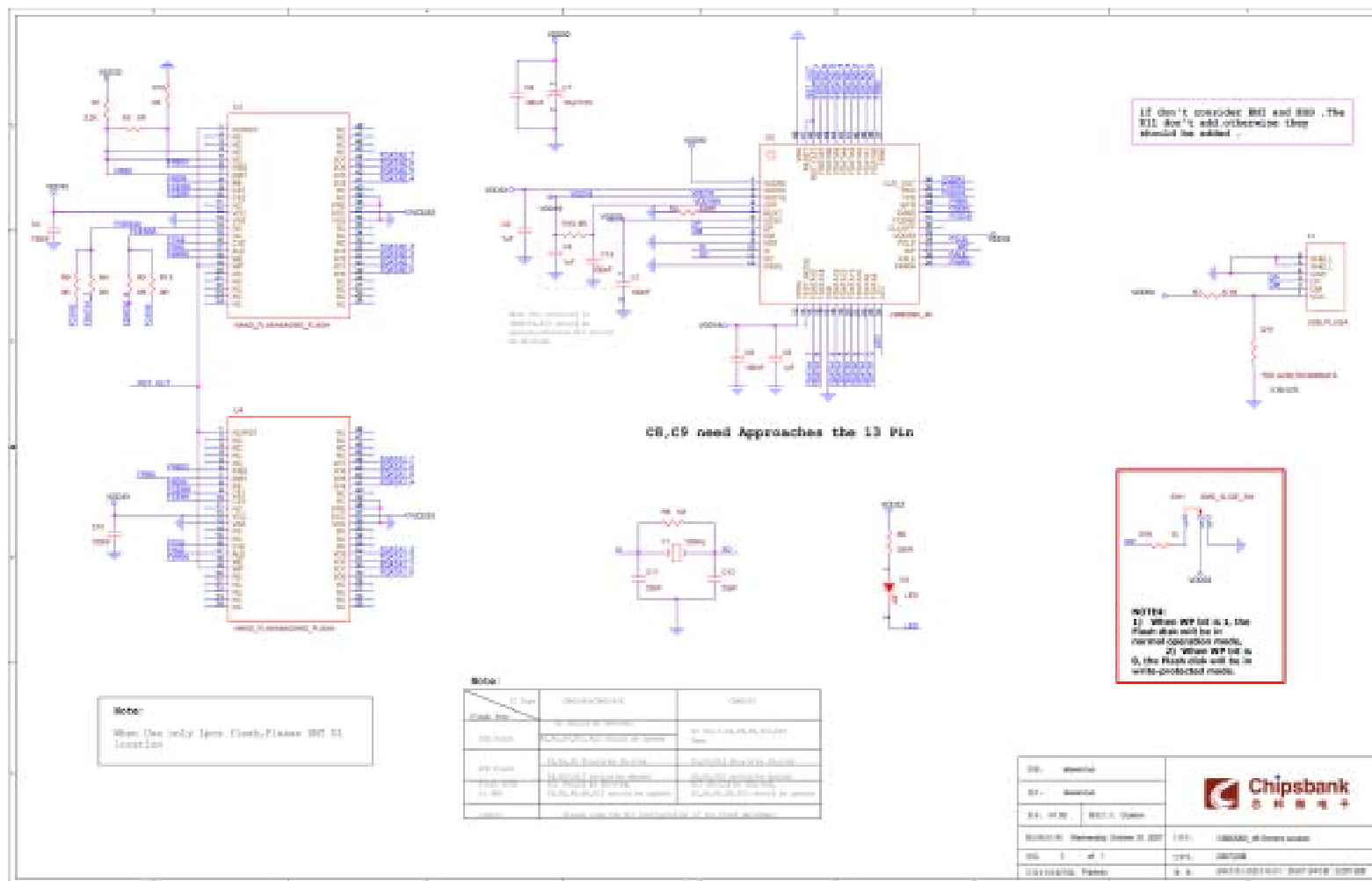
Timing diagram for Writing of Data



Timing diagram for Reading of Data

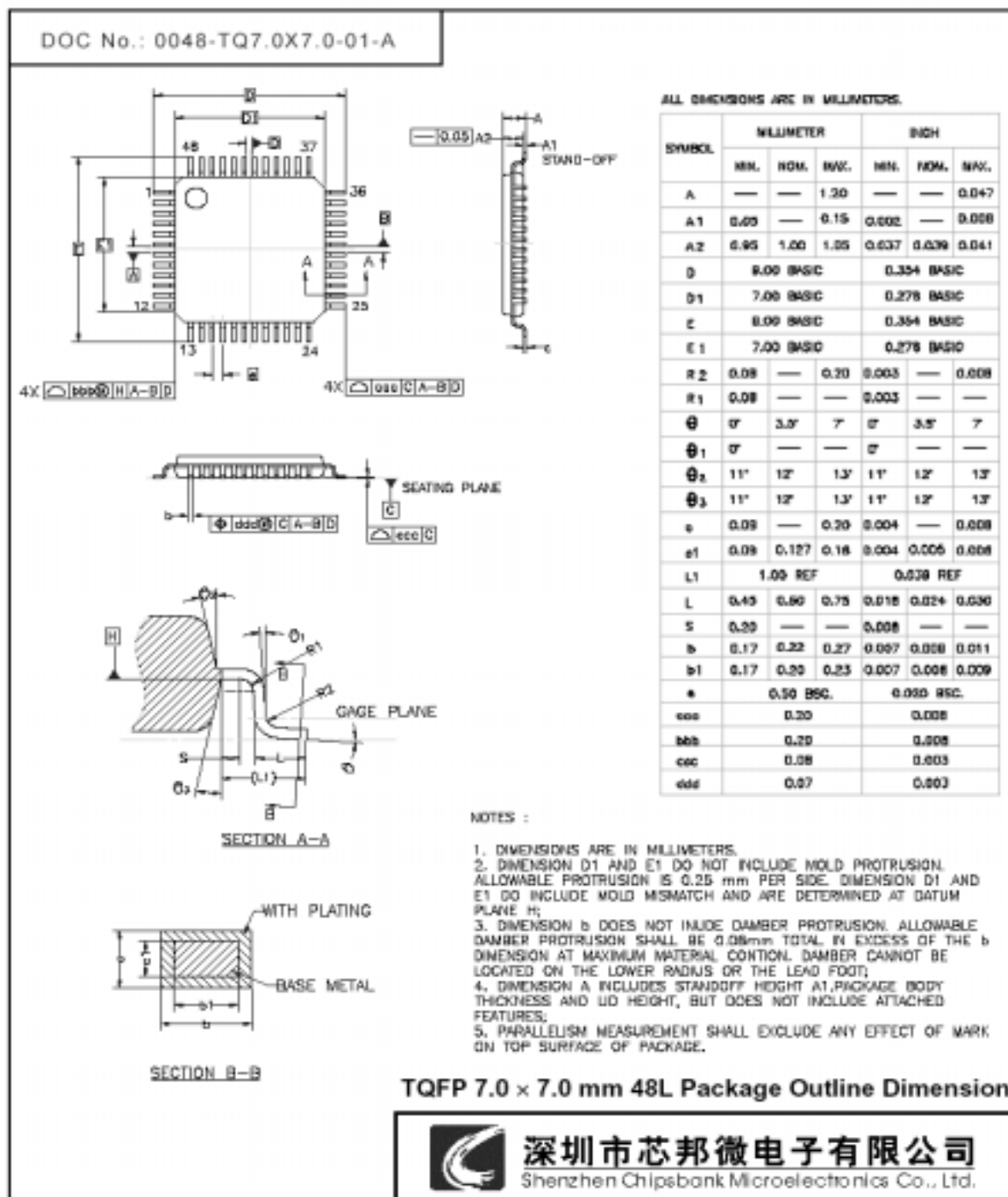


7 Typical Application

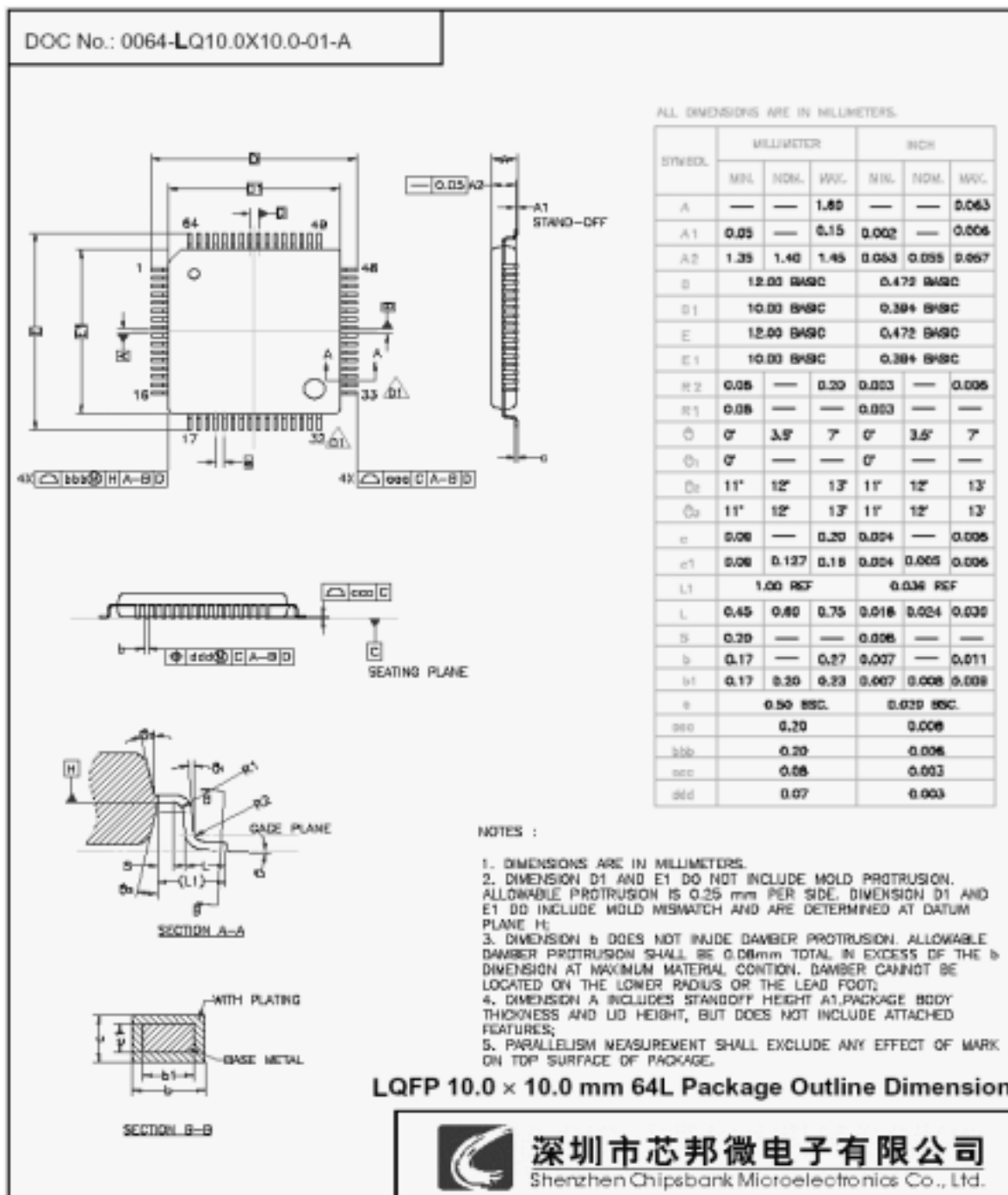


8 Mechanical Dimensions

8.1 48-Pin CBM2091 Package Outline Dimension



8.2 64-Pin CBM2091 Mode Package Outline Dimension



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