Investigating Via and Discrete Capacitor Effects Using Power Integrity Design Tools and Measurement Results

Kun Zhang, Huawei Technologies Co.
Zhen Mu, Cadence Design Systems, Inc
Heiko Dudek, Cadence Design Systems, Inc

Power delivery system design affects the performance of high-speed printed circuit board (PCBs). Good design strategy in a high-speed system not only provides clean and stable power supplies to the components, but also helps reduce design cycles and manufacturing costs. As the signal spectrum reaches the multiple megahertz to gigahertz range, power delivery design problems can no longer be ignored. It is evident that the results of power delivery and EMI research will soon lead the technology trend in the fields of high-speed analysis and simulation.

In recent years, methods of plane modeling in power delivery design for high-speed PCBs have been proposed. With these modeling and analysis methodologies, EDA tools have been developed to aid in power delivery design and analysis. However, there are still a number of problems in power plane modeling and analysis that must be addressed. One particular concern is how to accurately model and analyze via effects, especially in cases where there are many dense via areas on a board.

This paper investigates and discusses the effects of via density on power delivery systems designed for high-speed PCBs, the decoupling effect of discrete capacitors, and the precision of simulations conducted with the Allegro PCB PI option 610 (SPECCTRAQuest SQPI) power plane module (determined by correlating simulation results with measurements). For the purpose of this experiment, evaluation boards were specially designed and manufactured. Results of frequency responses between VNA measurements and Allegro PCB PI simulations were then compared. It was confirmed that vias shift a plane's resonance frequency

and that via effects on a board change the capacitance and inductance of plane pairs. In addition, via placement density has an impact on board decoupling designs. It was determined that when there are enough decoupling capacitors, the effects of densely placed vias can be ignored in the frequency range below 400MHz (where most discrete decoupling capacitors are at a high-impedance state before the first plane resonance occurs).The agreement between VNA measurements and Allegro PCB PI waveforms verified the modeling and simulation accuracy of the software, which can be used to guide power delivery designs for high-speed PCBs. The decoupling effect of discrete capacitors was also analyzed, and design guidelines are given in placing these capacitors.

INVESTIGATING VIA EFFECTS

Research has already revealed that via effects change a plane's capacitance and inductance and cause a shift of resonance frequency points on a plane pair. However, there was insufficient study on other via effects, especially when many areas on a board have high via density. An evaluation board was designed for the purpose of this investigation. To eliminate manufacturing variations, the board was segmented into four identical areas, as shown in Figure 1. Each area was assigned a different configuration of vias and via pads. Area (1) was a solid power plane with no via, noted as Novia; area (2) was a solid power plane with only anti-pads, noted as Antipad; area (3) was a solid power plane with both anti-pads and signal vias, noted as Signalvia; and, area (4) was a solid power plane with vias connecting to the power plane, noted as Powervia. The four sections had identical stackup parameters. The numbers, sizes, and positions of vias and pads in areas (2) through (4) were also identical. To investigate decoupling capacitor effects on vias, four types of capacitors were used: 0.01µF (X7R), 0.1µF (X7R), 1000pF (X7R), and 560pF (NPO). Five testing boards of this design were manufactured. No capacitor was placed on the first board. Placed on each of the four boards were 50 decoupling capacitors of each type.

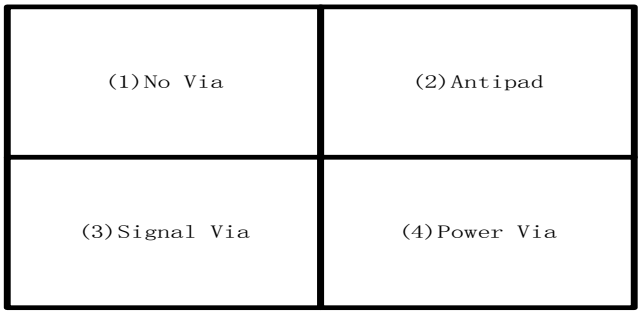


Figure 1: *Evaluation board design*

The measurements were taken using network analyzer E5071B with a full 2-port calibration. Simulations on power integrity using Allegro PCB PI were also performed. A 16 x 16 cell mesh of transmission line method [1] was used for plane modeling.

Figure 2 presents the frequency spectrum of the testing board 1.

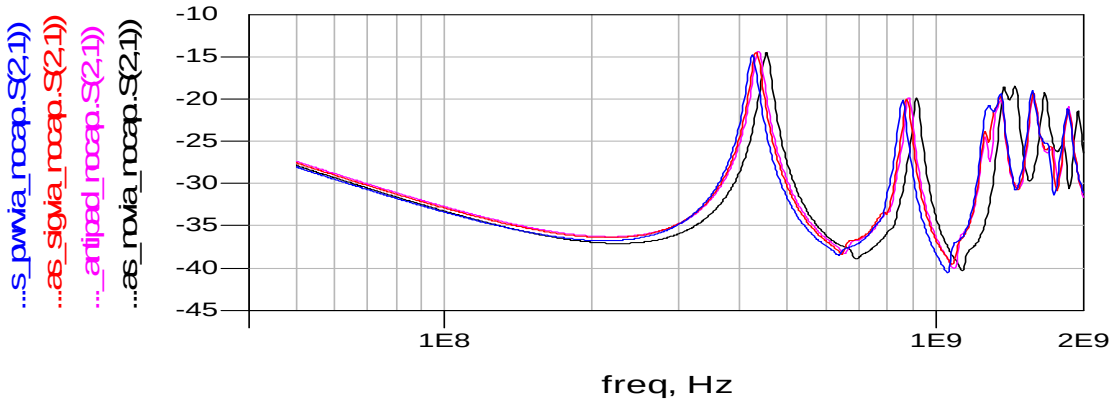


Figure 2 (a): Measurement results of testing board 1 (bare board) at 50MHz – 2GHz

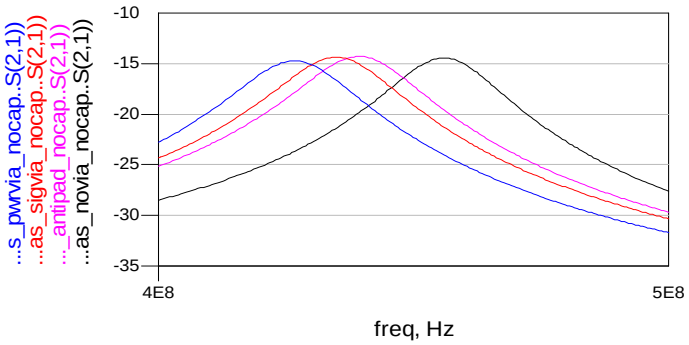


Figure 2 (b): Detailed measurements of testing board 1

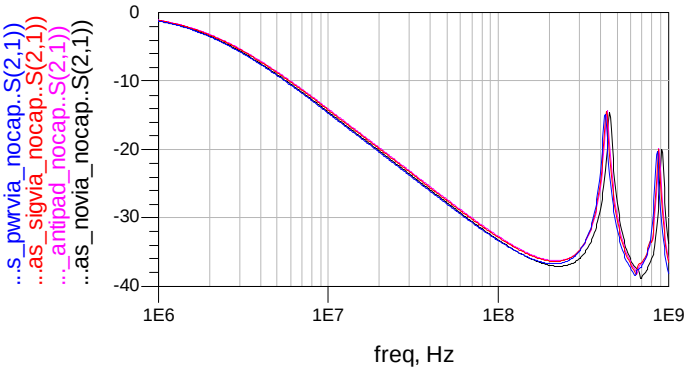


Figure 2 (c): Detailed measurements of testing board 1 up to 1GHz

Figure 3 displays the measured and simulated frequency responses of testing board 2 with 50 0.1µF (X7R) decoupling capacitors.

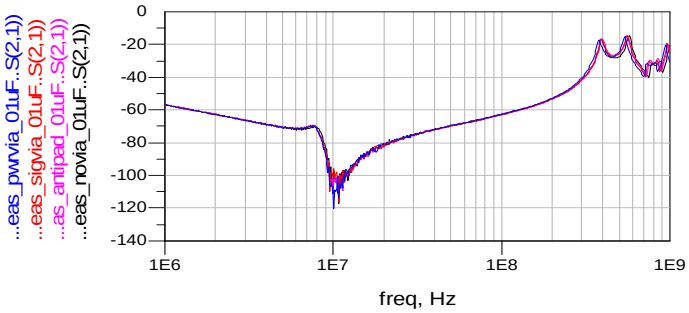


Figure 3 (a): Measurements of testing board 2 with 50 0.1µF (X7R) decoupling capacitors

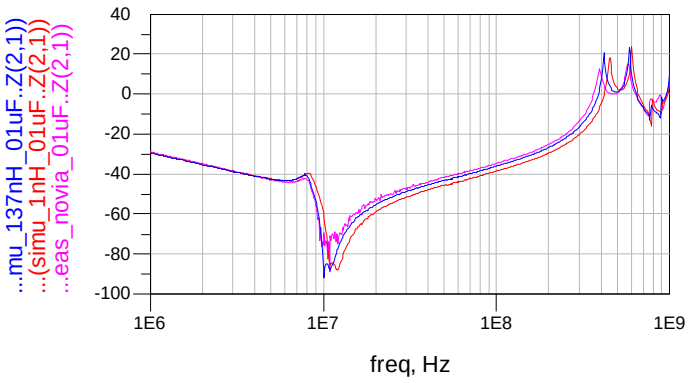


Figure 3 (b): Comparison of SQPI simulation results to the measurements of testing board 2 with 50 0.1µF (X7R) decoupling capacitors

Figure 4 shows the measured and simulated frequency responses of testing board 3 with 50 0.01µF (X7R) decoupling capacitors.

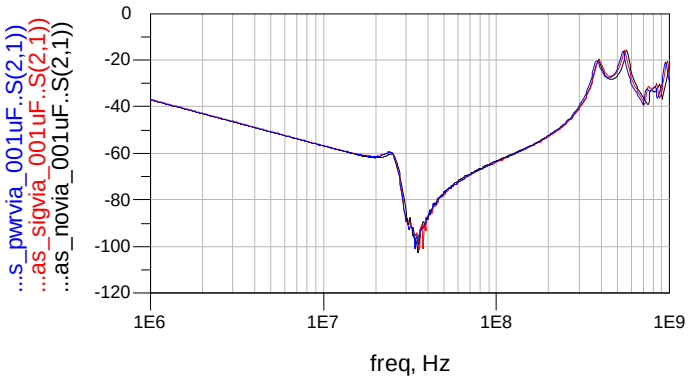


Figure 4 (a): Measurements of testing board 3 with 50 0.01µF (X7R) decoupling capacitors

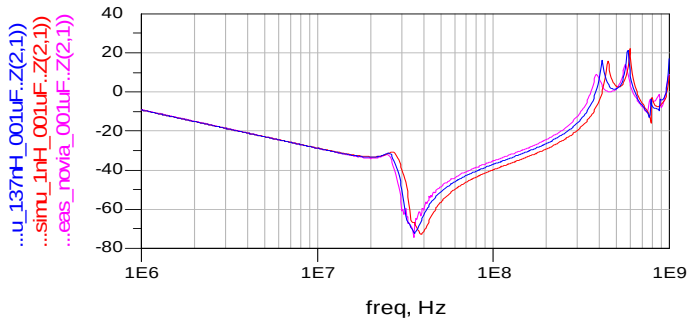


Figure 4 (b): Comparison of SQPI simulation results to the measurements of testing board 3 with 50 0.01µF (X7R) decoupling capacitors

Figure 5 presents the measured frequency responses of testing board 4 with 50 1000pF (X7R) decoupling capacitors.

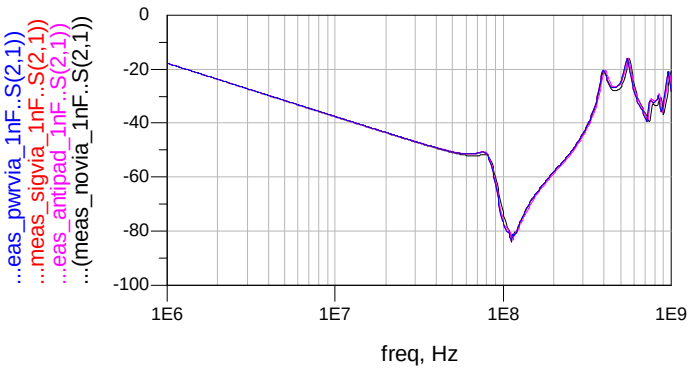


Figure 5 (a): Measurements of testing board 4 with 50 1000pF (X7R) decoupling capacitors

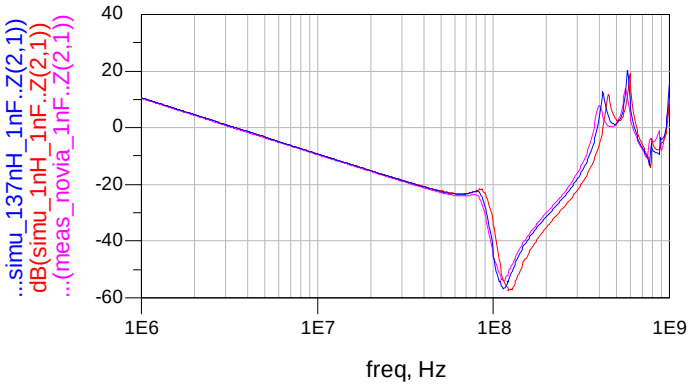


Figure 5 (b): Comparison of SQPI simulation results to the measurement of testing board 4 with 50 1000pF (X7R) decoupling capacitors

Figure 6 displays the measured and simulated frequency responses of testing board 5 with 50 560pF (NPO) decoupling capacitors.

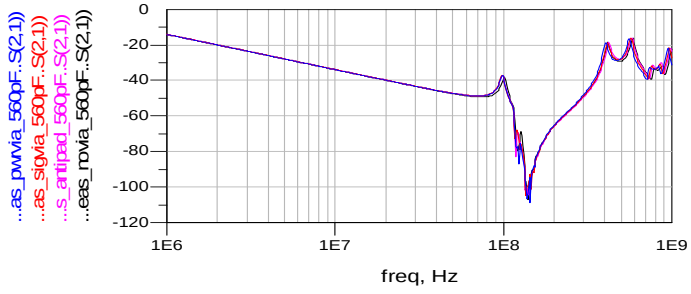


Figure 6 (a): Measurements of testing board 5 with 50 560pF (NPO) decoupling capacitors

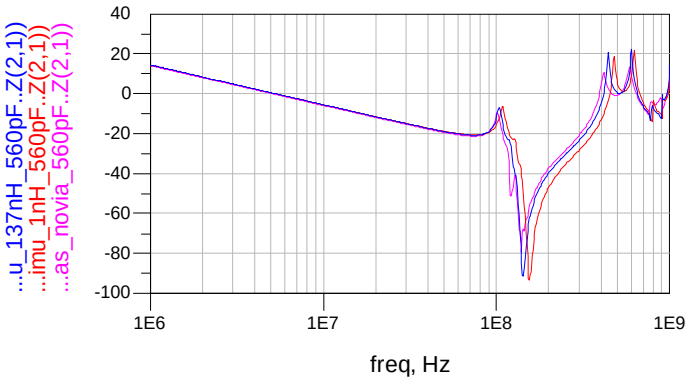


Figure 6 (b): Comparison of SQPI simulation results to the measurements of testing board 5 with 50 560pF (NPO) decoupling capacitors

Note: In all the curves of measurement and simulation, the red curves represent an inductance of 1.0nH, while the blue curves correspond to an inductance of 1.37nH.

Based upon our analysis of the measurement results from the five testing boards, we determined that, in the frequency range lower than 400MHz, there is no significant difference in plane behavior between the bare board and the boards with sufficient decoupling capacitors. Therefore, the planes with dense vias can be treated as solid planes when sufficient decoupling capacitors are in place. Equipped with correct capacitor models, Allegro PCB PI simulation results demonstrate the same conclusion with the measurements in agreement.

In larger planes, the first resonance frequency point moves lower and the via effect on resonance shifting becomes even more invisible due decoupling capacitors. At approximately 400MHz, the plane begins to resonate, and via effects are observable since decoupling capacitors behave as higher impedance.

CONTROLLING CAPACITORS' LEADING WIRES

Our investigation on via density also shows that the inductance caused by the capacitor leading wire has significant effect on the plane impedance. Therefore, limiting the length and width of leading wires plays a significant role in the success of power delivery system designs. It is difficult, based on simulation results, to identify the inductance problems caused by decoupling capacitors' leading wires. The best design practice here is to set up design rules in advance and apply the corresponding checking during placement and routing. Allegro PCB SI (SPECCTRAQuest) provides the functionality, EMControl, to automatically check problems which cause the EMI test failure. One of its rules is to control leading wire parameters of decoupling capacitors. It checks and limits the trace width and length of the following types of capacitors: bulk capacitors, tantalum capacitors, and ceramic capacitors, as Figure 7 indicates. By employing this rule in our designs, we are able to minimize the inductance effects on plane impedance and to best utilize all decoupling capacitors for power supplies.

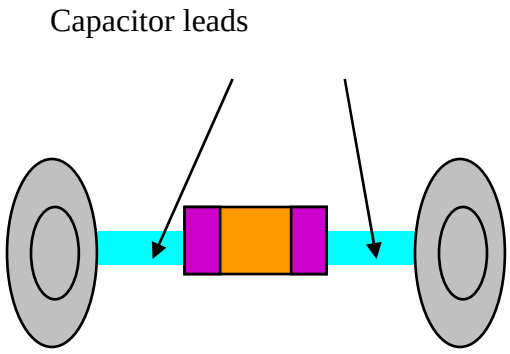


Figure 7: Using EMControl rule to control the leading wire parameters of decoupling capacitors

STUDYING DECOUPLING CAPACITORS

In this section, we examine the decoupling scheme of power and ground planes at high frequency range. We can compare the decoupling effect according to our measurements conducted in the previous section. Figure 8 presents the frequency spectrums of the boards with no capacitors and with 50 different capacitors, respectively. The measurement results indicate that:

a. as ESR goes up and capacitance goes down, the X7R capacitors do not have a good decoupling effect at higher frequencies, and

b. for the capacitors with equal capacitance values, the NPO capacitors give smaller ESR, which results in a better decoupling effect at higher frequencies.

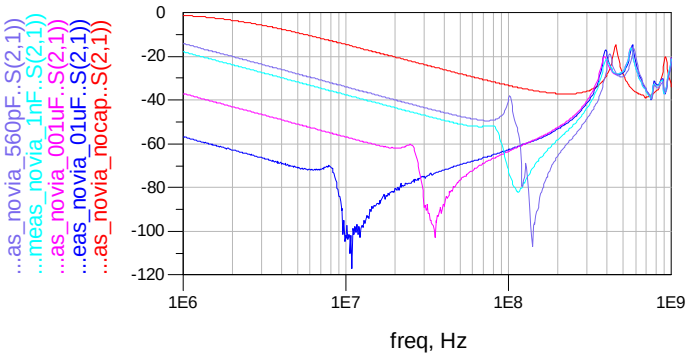


Figure 8: *Comparison of decoupling effect of different capacitors*

Our test results also show that the frequency range where planes are well decoupled can be extended up to 400MHz by means of correctly selected capacitors. When decoupling capacitors at high frequencies are used, anti-resonance can occur due to the variation

in spectrum between capacitors and power plane pairs. All of these require a solid understanding of plane capacitances. In the following section, we measure the plane capacitance of the four plane pairs from Figure 1.

At low frequency, the dimension of the plane pair is less than the wavelength. Therefore, the plane pair can be treated as one capacitor, as Figure 9 illustrates.

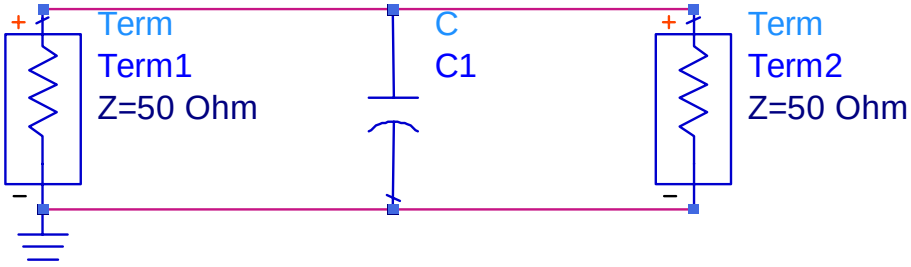


Figure 9: S-parameter representation of a capacitor

The two-port network consists of one capacitor. The following equations represent the relationship between S-parameters and capacitance impedance:

$$S_{21} = \frac{Z_x}{Z_x + 25} \quad Z_x = \frac{1}{j\omega C_1} \quad (1)$$

From the above equations, it is obvious that when Z_x is small, Z_x can be well represented by S_{21}. When Z_x is too large, S_{21} is close to 1. The change of Z_x cannot be derived from S_{21}. In addition, Z_x becomes larger when the frequency is lower. In order to measure the capacitance of a plane pair, we need to choose a suitable frequency point that satisfies the following conditions:

a. The frequency must be low enough that the plane pair can be treated as one capacitor, but

b. The frequency cannot be too low because then the plane's capacitive impedance is too large.

Here, we set the frequency to 50MHz for our measurements. Figure 10 presents the S_{21} measurement results of four plane pairs at the symmetrical positions: S(1,2) for the no via area; S(3,4) for the antipad area; S(5,6) for the signal via area; and, S(7,8) for the power via area.

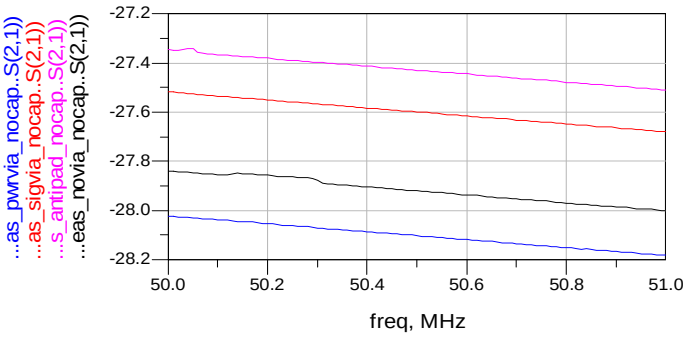


Figure 10: *S_{21} measurements in four areas*

Table 1 provides the S-parameters and corresponding Z and C values.

Table 1

	S21(db)	S21	Z	C (nF)
Novia	-27.84	-0.0406	-1.015	3.14
Antipad	-27.35	-0.0429	-1.073	2.97
Sigvia	-27.52	-0.0421	-1.053	3.02
PwrVia	-28.02	-0.0397	-0.993	3.21

The capacitances obtained here reflect the resonance frequency of the plane pairs, which can be extracted from the measurements provided in Figure 2. The corresponding resonance frequencies are: 465.6MHz in the novia area, 449.8MHz in the antipad area, 445.7MHz in the signalvia area, and 436.6MHz in the powervia area.

CONCLUSIONS

This paper investigated an important aspect in power delivery system design: the effect of vias. The measurements and correlated simulation results provide the design guideline that such effect can be ignored in the frequency range where decoupling capacitors are effective, under the condition that enough decoupling capacitors are correctly selected and placed. The paper also suggests to designers that applying design rules to restrict the geometry of decoupling capacitors is a better practice to improve the quality of a power delivery design.

REFERENCES

[1] Larry D. Smith, Raymond E. Anderson, Douglas W. Forehand, Thomas J. Pelc, and Tanmoy Roy; Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology, IEEE TRANS. Advanced Packaging, Vol. 22, No. 3, August 1999.

[2] Technical report on plane analysis and measurement, Huawei Technologies CO., 2003.

射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

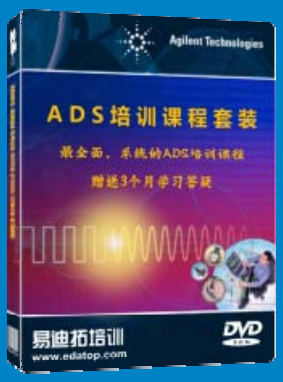
易迪拓培训课程列表：http://www.edatop.com/peixun/rfe/129.html

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

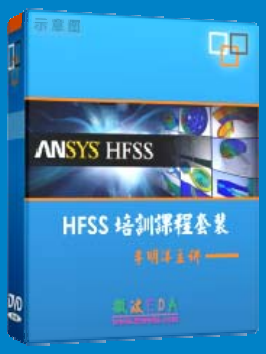
课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装



该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html



HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com