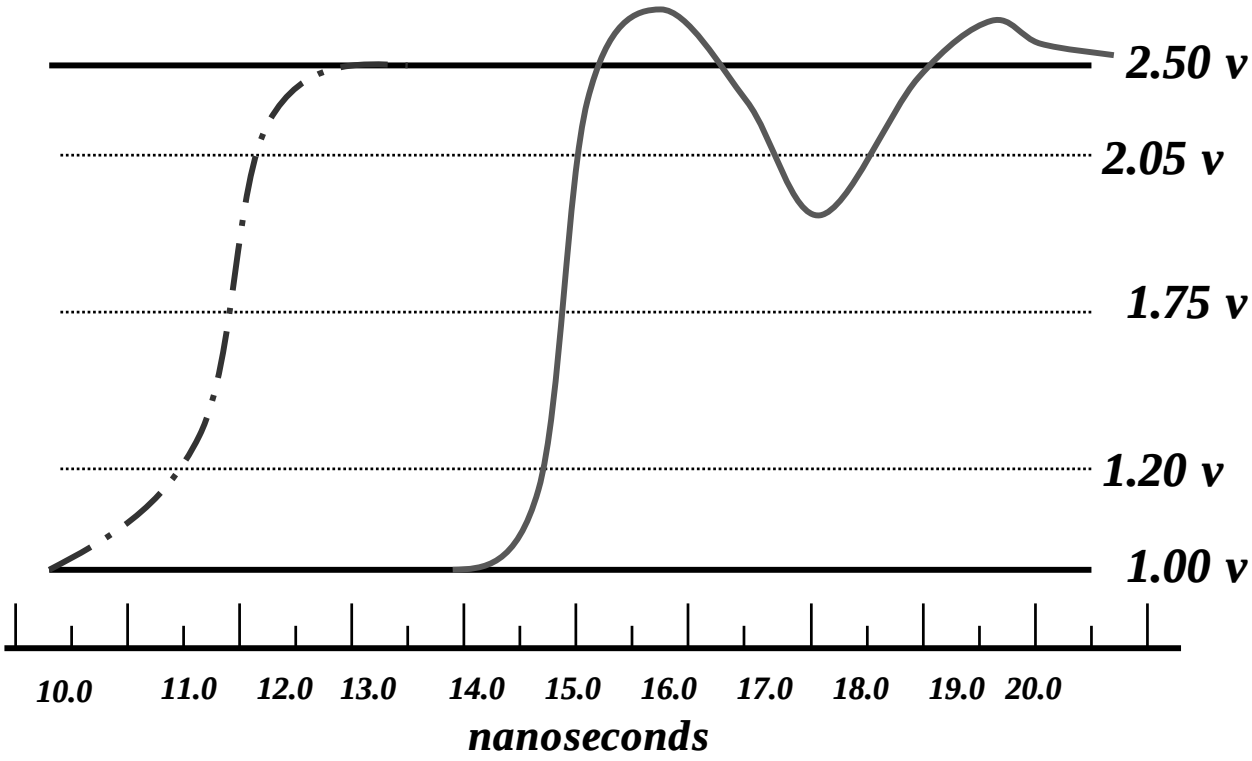
# ECE 744 - Homework # 1

## Spring 2001

## Due: Thursday February 8, 2001 11:20 AM. (On-Campus Only!)

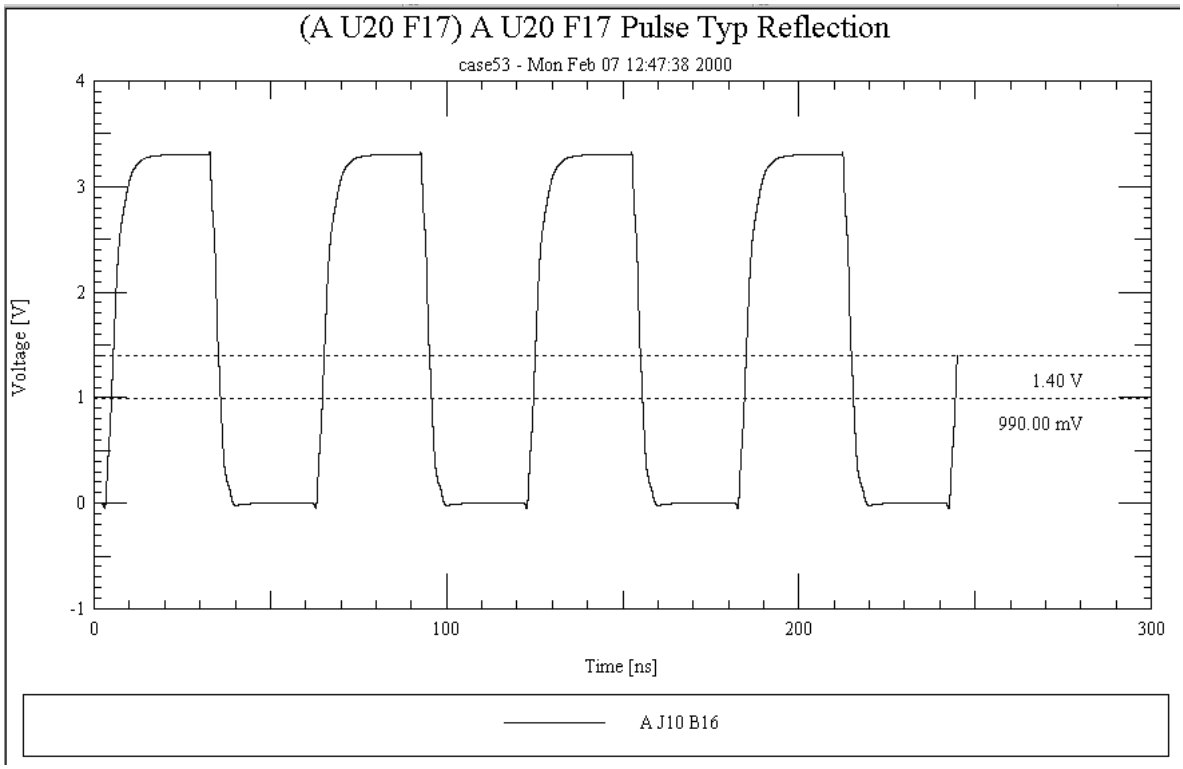
You may turn in paper copy or e-mail your homework. It may be hand-written or in electronic format.
**I highly encourage** you to work in groups, but each person must turn in their own homework, expressed in their own words, own calculations, etc. There will be no blatant copying allowed. State All Assumptions! Show All Work for Partial Credit !!!

(1) For the following 2 Plots of a Signal, Identify the Various SI parameters… fill in the tables for each. Assume the thresholds are marked by the appropriate lines…. **[5 pnts. Each]**




$V_{il\text{-}max}$ = 1.20V, $V_{ih\text{-}min}$ = 2.05V, $V_{ref\text{-}Driver}$ = 1.75 V, $V_{steady\text{-}state\text{-}high}$ = 2.50 V, $V_{steady\text{-}state\text{-}low}$ =1.0V

| Parameter | Measurement | Parameter | Measurement | Parameter | Measurement |
|---|---|---|---|---|---|
| Period T | | Noise Margin High | | Ringback (Rising) | |
| Duty Cycle | | Noise Margin Low | | Ringback (Falling) | |
| High Time | | Overshoot (Rising) | | Output Buffer Delay | |
| Low Time | | Overshoot (Falling) | | | |
| Frequency | | Monotonic Y/N ?? | | | |




$V_{il\text{-}max}$ = 0.7V, $V_{ih\text{-}min}$ = 2.55V, $V_{ref\text{-}Driver}$ = 1.75 V, $V_{steady\text{-}state\text{-}high}$ = 3.30 V, $V_{steady\text{-}state\text{-}low}$ =0.0V

| Parameter | Measurement | Parameter | Measurement | Parameter | Measurement |
|---|---|---|---|---|---|
| Period T | | Noise Margin High | | Ringback (Rising) | |
| Duty Cycle | | Noise Margin Low | | Ringback (Falling) | |
| High Time | | Overshoot (Rising) | | | |
| Low Time | | Overshoot (Falling) | | | |
| Frequency | | Monotonic Y/N ?? | | | |

(2) For the following Rise / Fall Times, what are the highest frequencies of interest for our analyses? Assume the 3X Rule applies. What is the wavelength $\lambda$ at this frequency? Assume $\varepsilon_r = 4.3$. **[6 pnts.]**

900 psecs Rise Time

2.0 nsecs Rise Time

250 psecs Rise Time

(3) For the following set of DC and AC Noise items, calculate the total noise based on each of the three formulas discussed in the lectures. Rank the calculated totals in order of magnitude. **[4 pnts.]**
The values listed are in millivolts.

| | |
|---|---|
| DC Noises | |
| Ohmic Drop | 5 |
| Voltage Differential | 11 |
| Temperature Differential | 7 |
| AC Noises | |
| Ohmic Drop | 20 |
| Reflection | 200 |
| Crosstalk | 139 |
| SSN | 277 |
| Power Supply Ripple | 15 |
| EMI (Incoming) | 5 |
| Gate I/O Level | 50 |

(4) (a) Given the following set of timings and interconnect lengths, determine the minimum cycle time.
Assume $\varepsilon_r = 4.0$ Assume Actual Line Load = Standard Load Specification. Assume Common Clock Architecture. **[4 pnts.]**

| | |
|---|---|
| Setup Time | = 1000 psecs |
| Hold Time | = 1 nsec |
| TCO - | = 1 nsec |
| Interconnect Length | = 35 inches |
| Settling Time | = 1.4 nsecs |
| Clock Skew | = 475 psecs |
| Clock Jitter | = 75 psecs |

(4b) Given the following set of timings and operational frequency, determine the minimum and maximum interconnect lengths for the system. Assume Common Clock Architecture. Assume Actual load = Standard Load Specification. Assume $\varepsilon_r = 4.5$ **[4 pnts.]** Do we satisfy hold time requirements?

Operation Frequency = 70MHz
Setup Time = 1.1nsecs
Hold Time = 1.1nsecs
Tco = 1.2 nsecs
Settling Time = 0 nsecs
Clock Skew = 500 psecs
Clock Jitter = 500 psecs

(5) (a) On a PCB design, a CPU requires that a 1.5 volt trace is routed across the board from the regulator. This CPU draws 40 Amps from the regulator. This trace length is 4 inches, and the device can tolerate a maximum DC drop of 1.5% for the regulated voltage. For a 2 oz. Copper trace, how wide must the trace be to meet these specifications? How much energy is dissipated in the trace? **[3 pnts.]**

(6) Calculate the size of a round wire, 100 feet long, which will connect to an ideal 8 ohm pure resistive load. This wire must carry a 40 volt signal and the voltage at the end must be within 5% of the source. How much energy is dissipated in this wire? **[4 pnts.]**

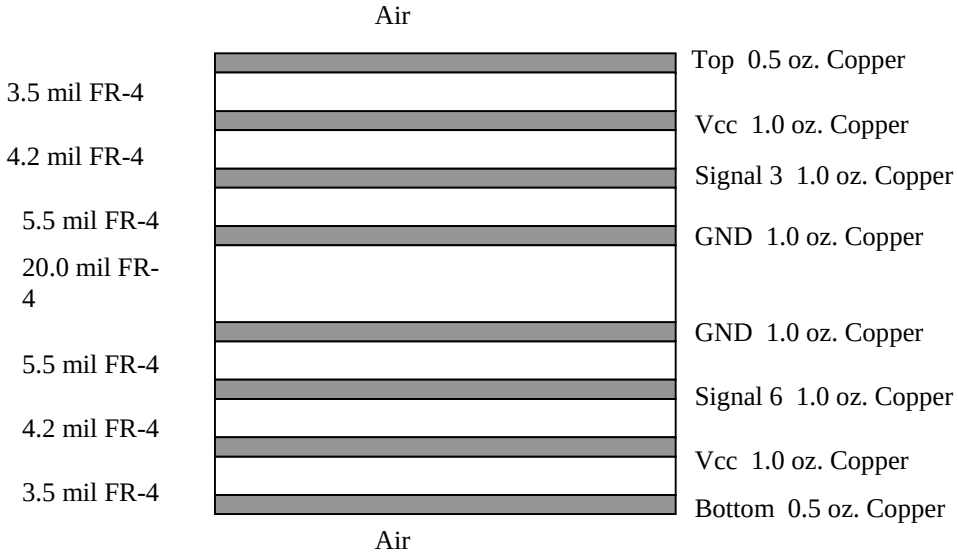
(7) (a) A PCB is 10 inches by 11 inches square. The Vcc and GND planes are 2.5 mils apart, with FR-4 material as the dielectric. Calculate the total capacitance provided by these two planes. State your assumptions. **[4 pnts.]**

(7b) How close would the same planes need to be to produce a capacitance of 1 uF ?? What dielectric would be needed to produce this type of board ? State your assumptions and reasoning. **[4 pnts.]**

(8) Fill in the blanks for the following parameters. Show all work. Use the equations from the class notes, show which equation you chose to use for each application. **[ 16 pnts. ]**

Assume straight, lossless lines w/o distributed loadings, Assume $\varepsilon_r = 4.3$

This PCB is a 4s4p (4 Signal, 4 Power) stackup, as shown.




| **Item** | **Layer** | **Width** | **Length** | **$C_o$ pf/inch** | **$R_o$ mohms/inch** | **$L_o$ nH/inch** | **$Z_o$ ohms** | **$C_{total}$ pF** | **$R_{total}$ ohms** |
|---|---|---|---|---|---|---|---|---|---|
| Wire | Top | 4 mils | 12 " | | | **N/A** | | | |
| Wire | Top | 12 mils | N/A | | | **N/A** | | | |
| Wire | S3 | 5 mils | N/A | | | | | | |
| Wire | S3 | 14 mils | N/A | | | | | | |
| Wire | S6 | 10 mils | 6" | | | | | | |
| Wire | Bottom | 5 mils | 16" | | | **N/A** | | | |

**What is the total board thickness ?**

(9) Repeat Example 5.3.2 from the textbook (Poon), but make the wave a **FALLING EDGE**. Use your choice of SPICE simulator, producing a plot similar to that of Figure 5.7. Discuss **briefly** why the number of segments used in the simulation effect the shape and accuracy of the waveform. Please submit your circuit and stimulus files as well as the plots of the results. **[ 17 pnts.]**

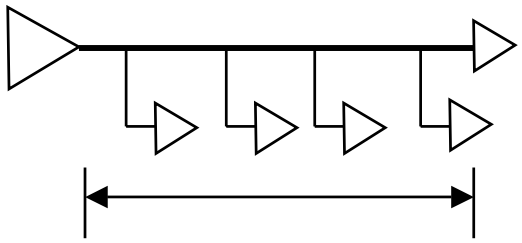
(10) What is the skin effect depth and $R_{skin}$ of the following wires at the specified rise times (frequency of interest): **[ 8 pnts.]**

| **Wire #** | **Material** | **$T_r$** | **Skin Depth cm** | **Trace Width cm** | **$R_{skin}$ Ohms/cm** |
|---|---|---|---|---|---|
| 1 | Copper | 2 usec | | $1.28 \times 10^{-2}$ | |
| 2 | Copper | 300 psec | | $2.00 \times 10^{-2}$ | |
| 3 | Tungsten | 3 usec | | $0.75 \times 10^{-2}$ | |
| 4 | Tungsten | 300 nsec | | $1.00 \times 10^{-2}$ | |
| 5 | Aluminum | 3 nsec | | $0.75 \times 10^{-2}$ | |
| 6 | Aluminum | 600 psec | | $0.75 \times 10^{-2}$ | |
| 7 | Gold | 1 nsec | | $1.28 \times 10^{-2}$ | |
| 8 | Gold | 500 psec | | $1.28 \times 10^{-2}$ | |

(11) (a) For the 4s2p stackup shown in problem number (8), determine the wire size and spacing required to produce a differential pair with an individual impedance of 70 ohms, and a differential impedance of 120 ohms. Assume that the wires are routed only on the TOP layer. **[ 6 pnts. ] State all other assumptions.**

(12) The specifications for the USB (Universal Serial Bus) differential pair wiring require an individual impedance of 50 ohms, with a differential impedance of 100 ohms. How can this be? Is this possible? What are they really trying to tell us here? What is the wire size and spacing required to meet this specification on the same PCB as in problem (8)? Assume the routing is on the BOTTOM layer only. State all assumptions required to solve this problem. **[4 pnts.]**

(13) For the following Driver / Receiver circuit, calculate the effects of adding 7 additional (total of 8) loads, equally spaced, with a capacitive load of 6 pF each. Assume that the chip inputs are on the transmission line (no stubs). Calculate BOTH the new $Z_o$ and $T_o$ values for this circuit**. Length = 10 inches! [6 pnts.]**



$C_o$ = 1.0 pf/inch, $Z_o$ = 65 ohms, $T_o$ = 175 ps/inch.

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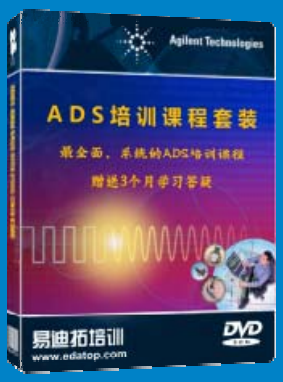


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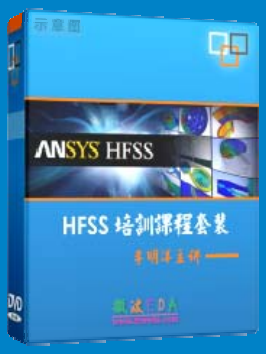


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