BGA (Ball Grid Array)

National Semiconductor
Application Note 1126
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Printed Circuit Board (PCB) Layout Guidelines

SOLDER BALL AND PBGA BALL PAD SIZES

As-received PBGA solder ball diameters are listed in *Table 1*. Recommended solder ball diameters as described in JEDEC Standard 95-1 Section 14 are listed in *Table 2*. The diameter is the maximum diameter of the ball measured parallel to the substrate surface. The ball sizes are for "low melt" solder, which is defined in the JEDEC Standard as a solder metallurgy that will go into the liquidus state when subjected to standard industry mount reflow temperatures of 220° C. Typical PBGA pad opening sizes as a function of pitch are listed in *Table 3*.

TABLE 1. As-Received Pbga Solder Ball Diameters

Pitch (mm)	Ball Diameter (mm)
1.27 (Note 1)	0.76
1.0 (Note 1)	0.5

TABLE 2. PBGA Solder Ball Diameters (Attached To Substrate)

Pitch (mm)	Ball Diameter (mm)		
	Min	Nom	Max
1.27 (Note 1)	0.60	0.75	0.90
1.0 (Note 1)	0.50	0.60	0.70
0.8 (Note 2)		0.45 - 0.5	

TABLE 3. PBGA Pad Opening Size

Pitch mm (mils)	Pad Opening Size mm (mils)
1.27 (50)	0.63 (25)
1.0 (40)	0.45 (18)
0.8 (31)	0.35-0.45 (14-18)

Note 1: JEDEC Specification

Note 2: Available

PRINTED CIRCUIT BOARD PAD DEFINITION

Two types of land patterns are used for surface mount packages: (1) Solder mask defined (SMD) pads that have the solder mask opening smaller than metal pad and (2) Non-solder mask defined (NSMD) pads that have the metal pad smaller than the solder mask opening. *Figure 1* illustrates the two types of pad geometry.

SMD defined pads have an advantage in that the photoprocessing of the soldermask results in better definition compared to the copper pad. Control of the isotropic etch of the copper is the limiting factor in defining the metal pad. Copper adhesion to the laminate is increased because of the overlying solder mask.

NSMD defined pads enhance vision registration of copper fiducials compared to the SMD defined pad. For SMD defined pads, any misregistration of the solder mask will contribute to further Moreover, SMD pad definition can introduce stress concentration points near the solder mask on the PCB side that may result in solder joint cracking under extreme fatigue conditions.

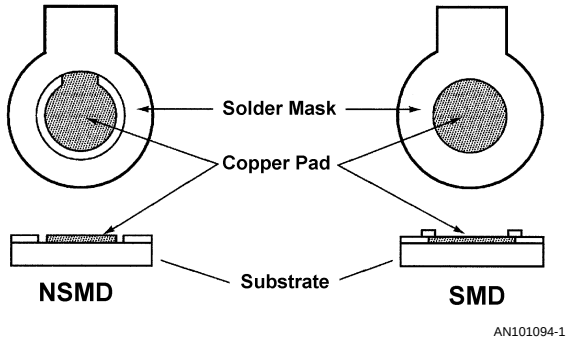

FIGURE 1. NSMD and SMD Pad Designs

A 1:1 ratio between the package pad and PCB pad is desirable to balance the stress during temperature cycling, though a slightly smaller ratio (0.8) can be used for the PBGA to facilitate routing between pads in the area array package. For NSMD pads it is necessary to have a clearance around the copper pad and the solder mask to account for mask registration tolerances (typically ±0.075 mm or 3 mils) and to void any overlap between solder joint and the solder mask. *Table 4* list recommended guidelines for PCB pad designs as a function of PBGA ball pitch.

TABLE 4. Guidelines For Pad Designs

	NSMD mm(mils)	SMD mm(mils)
PBGA Ball Pitch = 1.27 mm		
Ball Size	0.75 (30)	0.75 (30)
PCB Pad Diameter	0.63 (25)	0.71 (28)
Solder Mask Opening Diameter	0.78 (31)	0.63 (25)
PBGA Ball Pitch = 1.00 mm		
Ball Size	0.60 (24)	0.60 (24)
PCB Pad Diameter	0.45 (18)	0.55 (22)
Solder Mask Opening Diameter	0.60 (24)	0.45 (18)
PBGA Ball Pitch = 0.8 mm		
Ball Size	0.5 (20)	0.5 (20)
PCB Pad Diameter	0.35 (14)	0.48 (19)
Solder Mask Opening Diameter	0.5 (20)	0.38 (15)

ROUTING GUIDELINES

A typical PBGA substrate has four or five rows of solder balls around the periphery of the package that provides interconnection to the PCB. The number of lines routed (N) between the pads on the PCB is defined by the pad size and the line width and spacing capabilities. The following relationship is used to define N:

$$N = \frac{P - D - S}{L + S}$$

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P = Pad Pitch
D = Pad Diameter
L = Line Width
S = Line Space

For NSMD pads exposure of underlying copper traces is forbidden, so the diameter and tolerance of the solder mask opening define D.

The number of routing lines as a function of pad pitch for various PCB line space/width geometries are shown in *Table 5*. Routing assumes a four layer board (2 signal and 2 ground) with NSMD pads on the PCB. The package pad to PCB pad diameter ratio is 1:0.8.

TABLE 5. Number of Routing Lines

	Pad Pitch		
	1.27 mm (Note 3)	**1.0 mm** (Note 4)	**0.8 mm** (Note 5)
L/S = 0.15 mm (6 mil)	1	1	X
L/S = 0.125 mm (5 mil)	2	1	X
L/S = 0.1 mm (4 mil)	2	2	1
L/S = 0.075 mm (3 mil)	3	3	2

Note 3: Solder mask opening diameter = 0.60 mm (24 mil)

Note 4: Assume NSMD, pad diameter = 0.45 mm (18 mil)

Note 5: Assume NSMD, pad diameter = 0.45 mm (18 mil)

Either a 1.0 or 1.27 mm pitch PBGA with four rows of solder balls can be routed to a four layer PCB (*Figure 2*) using a 0.15 mm (6 mil) line/space. The first two ball rows can be routed to one signal layer while the third and fourth ball rows can be routed to a second signal layer.

Routing possibilities become more complicated for a four-layer board if there are five rows of solder balls. For a 1.27 mm ball pitch PBGA, a 0.125 mm (5 mil) PCB line/space design will be necessary for routing (*Figure 3*). A 1.0 mm PBGA will require a 0.10 mm (4 mil) line/space to successfully route 5 rows of solder balls to a four-layer PCB (*Figure 4*). For both packages, the first three ball rows are routed to one signal layer while the fourth and fifth ball rows are routed to a second signal layer.

Six rows of solder balls would require a reduction to a 0.075 mm (3 mil) line/space design for routing a four-layer PCB for both the 1.0 and 1.27 mm PBGA. These geometries will require advanced micro-via structures to achieve the desired via and line densities (*Figure 5*).

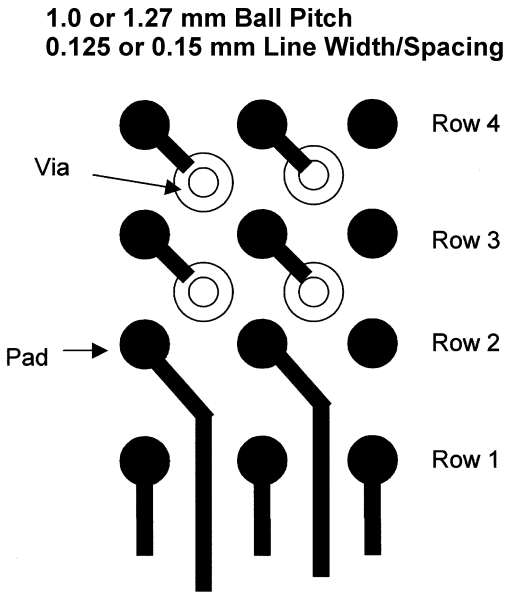

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FIGURE 2. Routing for Four Rows of Solder Balls

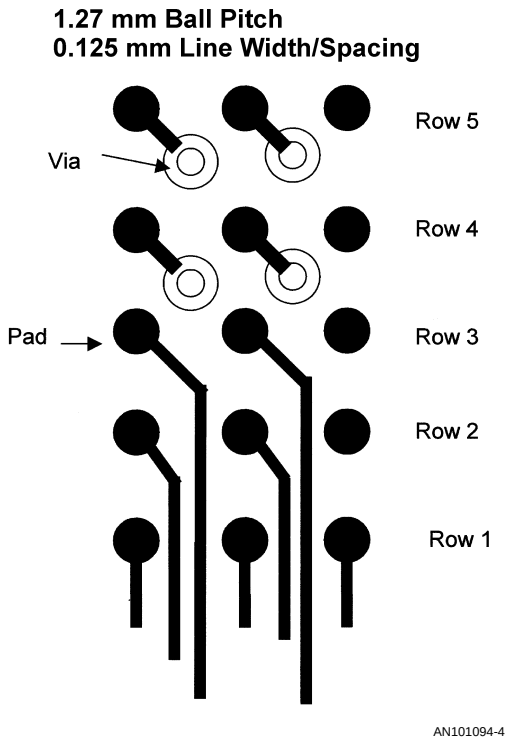


FIGURE 3. Routing for Five Rows of Solder Balls for a 1.27 mm Pitch PBGA

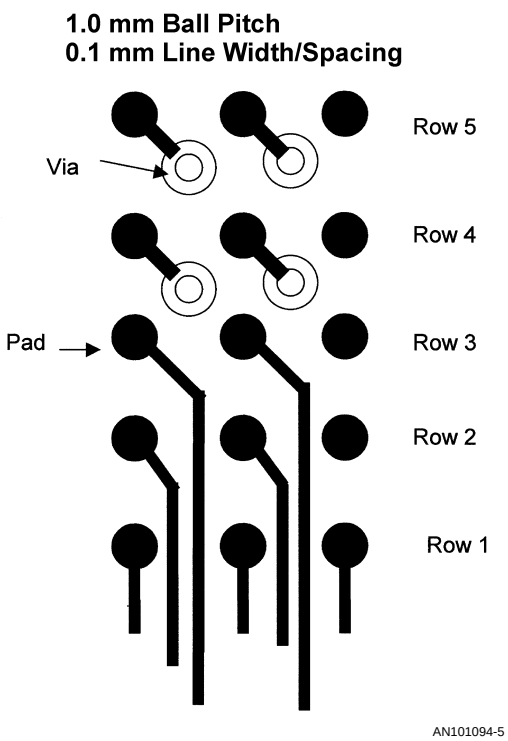


FIGURE 4. Routing for Five Rows of Solder Balls for a 1.0 mm Pitch PBGA

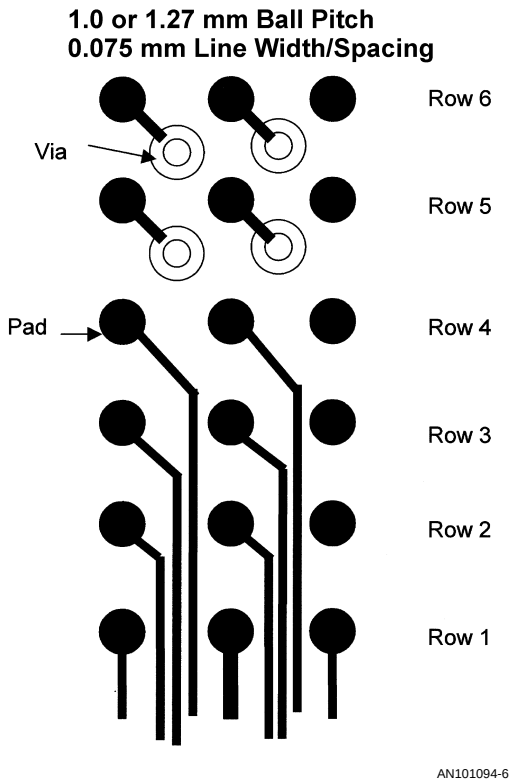


FIGURE 5. Routing for Six Rows of Solder Balls

VIA DENSITY

Via density has a significant impact on the routability of PBGA especially as the solder ball pitch decreases to 0.8 mm. *Figure 6* shows the routability of a 0.8 mm ball pitch PBGA using 0.1 mm line space and width.

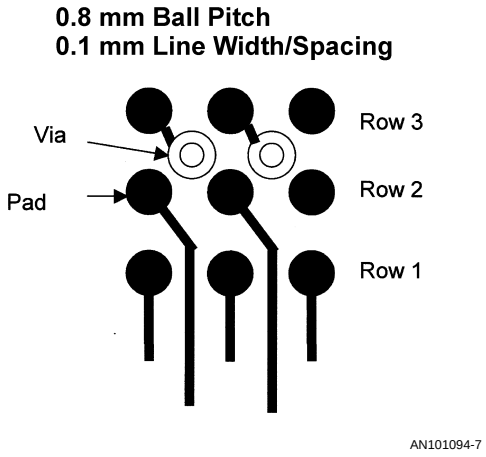


FIGURE 6. Routing for Six Rows of Solder Balls

Mechanically drilled holes below 0.30 mm (12 mil) in diameter, begin to add substantial cost to the PCB, with 0.20 mm (8 mil) being the minimum diameter that can be typically drilled in high-volume PCB manufacturing.

As traditional PCB material and processes have been pushed to the limit and are unsatisfactory in meeting the wiring densities, new PCB manufacturing technologies have emerged. *Table 6* list trends for PCB used in portable computers.

TABLE 6. Feature Trends for Portable Computer PCB

	Portable Computers		
	1997	**2000**	**2002**
Number of Layer	5-8	7-9	7-10
Inner Layer Thickness (mm)	0.1	0.7	0.5
Via Diameter (mm)	0.28	0.125	0.1
Land Diameter (mm)	0.48	0.25	0.25
Line Space/Width (mm)	0.1	0.75	0.5

To increase wiring density and improve electrical performance, thin layers are fabricated onto a PCB core with small micro-vias. These micro-via technologies which are referred to as build-up board (BUB) technologies are cost-effective alternatives to PCB processes for manufacturing board substrates.

There are many variations of BUB boards, though a generic structure consists two-layers of unreinforced epoxy dielectric coated on to a rigid (core). Micro-vias are typically formed using either laser or photolithography processes. The fabrication of BUB boards requires new processes and materials compared to standard PCB technologies. *Table 7* shows some micro-via geometries available to facilitate the routing of PBGA packages.

The cost trade-offs for deciding on a micro-via PCB design compared to a standard PCB design is a function of the via forming process, materials used, and the number of vias. Consult your PCB manufacturer for a detail cost analysis.

TABLE 7. Availble Micro-Via Geometries

Line Width	0.075-0.1mm (3-4 mil)
Line Spacing	0.075-0.1mm (3-4 mil)
Microvia Hole Size	0.075-0.1mm (3-4 mil)
Microvia Pad	0.2-3 mm (8- 12 mil)
Drilled Through Hole (Core)	250 µm (10 mil)
Drilled Through Hole Pad (Core)	500 µm (20 mil)
Buried Via Hole	200 µm (8 mil)
Buried Via Capture Pad	450 µm (18 mil)

Package To Board Assembly

PACKAGE HANDLING

Handling during board level assembly requires the typical precautions associated with BGA packages (Reference J-STD-013) with the PBGA compatible with high-volume au-

Package To Board Assembly

(Continued)

tomated pick & place systems used in board assembly. Manual handling of the packages using a vacuum wand or a non-metallic tweezers requires the appropriate ESD protection. The BGA is available in JEDEC trays and will be available in tape & reel for high volume production. Trays are recycable.

MOISTURE PRECONDITIONING

Both the encapsulant and substrate materials used for PBGA absorb moisture. Handling precautions as defined by JEDEC specification J-STD-020 must be carefully followed to prevent cracking and delamination associated with the ″popcorn″ effect during solder reflow. PBGA are tested and classified for moisture level performance following the specification that defines temperature, humidty, and time conditions for moisture. (Chapter 5 contains more details on moisture sensitivity characterization).

A typical PBGA is classified at a Level 3 or 4 moisture sensitivity. Components are baked prior to vacuum sealing in a dry bag that includes a dessicant pack and a humidity indicator card. If the specified out of bag time has elapsed, components must be baked and resealed in a vacuum bag. Storage in either a nitrogen cabinet or a dry box is another option available to prevent moisture uptake. Failure to comply with the times specified for each moisture level, risk component failure during solder reflow. Since moisture uptake occurs during the life of the component mounted on the board, baking procedures are required prior to any rework process.

SURFACE MOUNT CONSIDERATIONS

PBGA surface mount assembly operations include screen printing solder paste on the PCB, package placement using standard surface mount (SMT) placement equipment, reflow and cleaning (depending on flux type). Standard tape and reel or tray shipping media facilitates package handling during assembly.

STENCIL PRINTING SOLDER PASTE

The solder paste is stencil printed onto the board, which involves transferring the solder paste through pre-defined apertures by the application of pressure. Stencil parameters such as aperture area ratio and fabrication process have significant impact on volume of paste deposited onto the pad. The aperture area ratio is defined as the ratio of stencil aperture cross-section to the aperture wall area. To obtain the desired solder paste transfer an area ratio of ≥ 0.66 is recommended. Inspection of the stencil prior to placement of the packages is highly recommended as part of a quality program to improve board assembly yields.

Three typical stencil fabrication methods include chem-etch, laser cut and metal additive processes. Nickel plated, electropolished chem-etch stencils or laser cut stencils with tapered aperture walls (5o taper is recommended) to facilitate paste release are recommended. For PBGAs the recommended aperture size is 0.1 mm larger than the pad size to allow 0.05 mm overprinting on each side. Stencil thickness of 0.125 mm to 0.150 mm are recommended to PBGAs. General guidelines for aperture openings for 0.75 mm and 0.6 mm ball sizes are 0.70 mm and 0.55 mm, respectively.

Table 8 list Solder Paste Classifications and Mesh Sizes. To avoid drying out the paste follow the handling guidelines recommended by the paste supplier.

TABLE 8. Solder Paste Classification

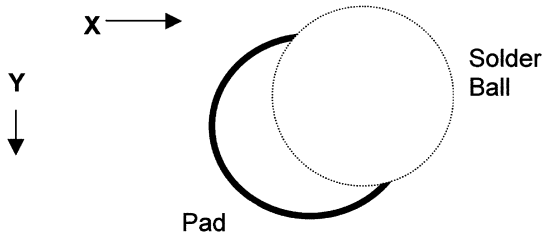
Class	Mesh Size
Type 1 -100/+200	100 (150 µm/6.0 mil)
Type 2 -100/+200	200 (75 µm/3.0 mil)
Type 3 -100/+200	325 (45 µm/1.8 mil)
Type 4 -100/+200	400 (38 µm/1.5 mil)
Type 5 -100/+200	500 (25 µm/1.0 mil)
	635 (20 µm/8.0 mil)

PART PLACEMENT

PBGA packages are placed using standard pick & place equipment with ±0.050mm (± 2 mil) placement accuracy. Package pick & place systems comprise of a vision system to recognize and position the component and a mechanical system to physically perform the pick and place operation. Two commonly used types of vision systems for area array packages are (1) a vision system that locates package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. The latter type often renders more accurate placement but tends to be more expensive and time consuming. Both pick & place methods are acceptable as misaligned packages will self-align during reflow.

PBGA has excellent self-alignment during solder reflow if a minimum 50% of the ball is aligned with the pad. The 50% accuracy is in both the X and Y direction as determined by the following relation,

$$\frac{D}{2} = (X^2 + Y^2)^{1/2}$$



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where D is the pad diameter. 50% misalignment for a 0.63 mm and 0.35 mm diameter pads are ±0.22 mm and ±0.12mm, respectively. As stated above, standard pick & place equipment can accurately place components within this degree of accuracy.

SOLDER PASTE REFLOW AND CLEANING

The PBGA are assembled using standard SMT reflow processes without any special considerations. Both packages are qualified up to three reflow operations (J-STD-020). Recommended peak reflow temperature is 220° C for the PBGA.

DOUBLE-SIDED PROCESS

The double-sided process follows the same procedure as the single-sided process: mount and reflow the packages on one side, turnover the board and repeat the process.

COMPONENT REWORK

Rework is the removal and replacement of a defective component from the PCB. Removing the PBGA from PCB has unique challenges as direct contact between rework tools and the solder ball joints can not be achieved. Heating of the solder joints is achieved by using a special fixture for directing and confining heat to the ball joints and the PCB directly underneath the package.

Rework involves heating solder joints above liquidus temperature of eutectic solder using a vacuum gas nozzle. Nozzle designs optimize the hot gas flow around the BGA while eliminating the hot gas back pressure and the corner and edge effect associated with package proximity to the nozzle. A 1.25 mm (50 mil) keep out zone for adjacent components, including discretes, is recommended for standard rework processing. If adjacent components are closer, custom tools or heat shields will be required for package rework and removal.

Ramp rates and thermal profiles must be controlled to minimize damage to the surrounding components. A ±5 ˚C gradient across the heating zone is recommended. Preheating the PCB to a predetermined temperature (a uniform and reliable board temperature of 100 ˚C is suggested) before heating the PBGA will insure a controlled process. Once the liquidus temperature is surpassed, the nozzle vacuum is automatically activated and the component is picked up.

After removing the PBGA, the pads may be heated using the same vacuum gas nozzle to reflow any residual solder, which is then removed using a Teflon tipped vacuum wand. Clean solder pads with alcohol and a brush then dry and inspect. For component replacement, no-clean flux is applied to the reworked site, and the component is placed, reflowed, inspected, and electrically tested. Temperature monitoring of the PCB is recommended to minimize board warpage.

Suggest rework equipment and tooling vendors.

Air-Vac Engineering (203)888-9900	OK International (914)969-6800	Zephyrtronics (909)865-2595

INSPECTION

Traditional line-of-sight techniques for the inspection (AOI and human visual Inspection) of solder joints are impossible with PBGA since the balls are hidden from open view. Transmission X-ray inspections are employed following surface mount assembly to identify defects such as missing contacts, bridging, misregistrations, opens, and voids.

Missing Contacts:	Missing or misplaced solder balls
Bridging:	Caused by excessive solder on the contact
Misregistration:	Misalignment of BGA balls to the PCB pads
Opens:	Caused when no contact is achieved between the solder ball and the PCB pad
Voids:	Caused by the entrapment of volatiles and other compounds in the solder ball during reflow

SOLDER JOINT RELIABILITY

Board level reliability has been demonstrated with the PBGA under various conditions. A 361-Lead PBGA with 1.27 mm pitch passes 6000 temperature cycles from -40 to 100 ˚C (10 ˚C/minute ramp and 16 minute dwell) . *Table 9* lists the number of cycles to the first failure and 50% failures with various package and board designs. The use of NSMD on both the package and the board clearly has an advantage for promoting board reliability.

TABLE 9. Board Reliability Results for 361L PBGA, -40 to 100 ˚C temperature cycle.

	Package		Board		Cycles to falure	
	Pad	Size (mm)	Pad	Size (mm)	First	50% (Note 6)
1	NSMD	0.51	NSMD	0.51	5500	6000
2	SMD	0.56	SMD	0.56	2500	2900
3	SMD	0.56	NSMD	0.56	2100	2800
4	NSMD	0.51	SMD	0.51	3200	4000

Note 6: 50% of packages have one failure

Board reliability for -40 to 125 ˚C (8-10 ˚C/minute ramp, 25 minute dwell 125 ˚C and 15 minute dwell at -40 ˚C) also proves the integrity of the PBGA package .

Board Reliability Results for 256L PBGA, -40 to 125 ˚C temperature cycle.

Cycles to failure	
First	50%
1451	4359

Although, a majority of board level characterization is performed using a PCB with organic solderability preservative coating (OSP) finish, no significant impact of PCB pad finish is observed with the assembly and reliability of the PBGA. A uniform coating thickness is key for high assembly yield. For an electroplated nickel-immersion gold finish, the gold thickness shall be a minimum of 0.5µm to avoid solder joint embrittlement.

1. R. Rorgren, P.E. Tegehall, and P. Carlsson, Journal of Surface Mount Technology, V11(2) p.35, 1998

2. P. Viswanadham, K. Ewer, R. Aguirre, and T. Carper, Journal of Surface Mount Technology , V12(1) p.1, 1999

Tray, Tape & Reel and Test Socket Info

JEDEC trays and tape & reel available from KOSTAT and Peaks Plastic. Test and burn in sockets are tooled with Loranger. The test contacts are tooled up with Johnstech.

KOSTAT Santa Clara, CA (888)390-0885	Loranger International Corp. Warren, PA (814)723-2250
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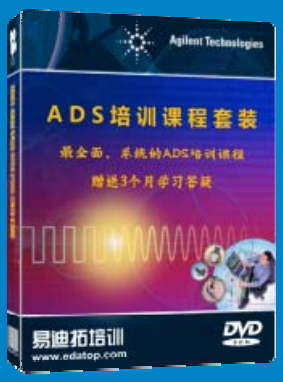

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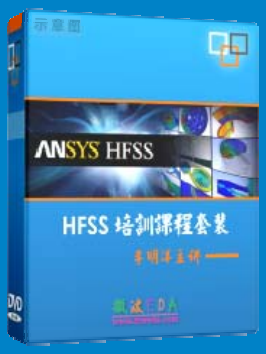

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课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

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