GROUNDING IN HIGH SPEED SYSTEMS

Walt Kester, James Bryant

The importance of maintaining a low impedance large area ground plane is critical to practically all analog circuits today, especially at high speeds. The ground plane not only acts as a low impedance return path for high frequency currents but also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuits susceptibility to external EMI/RFI is also reduced.

All IC ground pins should be soldered directly to the ground plane to minimize series inductance. Power supply pins should be decoupled to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1mm. Ferrite beads may be also required.

The ground plane allows the impedance of PCB traces to be controlled, and high frequency signals can be terminated in the characteristic impedance of the trace to minimize reflections when necessary.

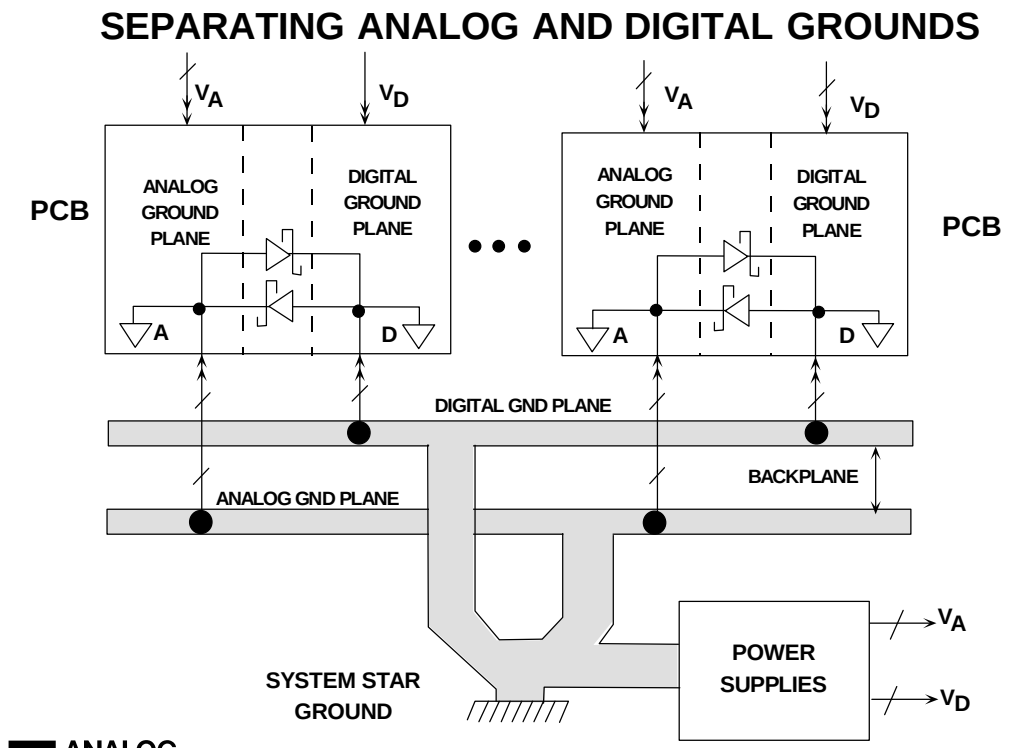
Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers and vias. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands." IC ground pins located in a ground "island" have no current return path to the ground plane.

The best way of minimizing ground impedance in a multicard system is to use another PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the mother card. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities: (1) The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. (2) The ground plane can be connected to a single system "star ground" point (generally at the power supply).

The first approach is often used at very high frequencies and where the return currents are relatively constant. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. It is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

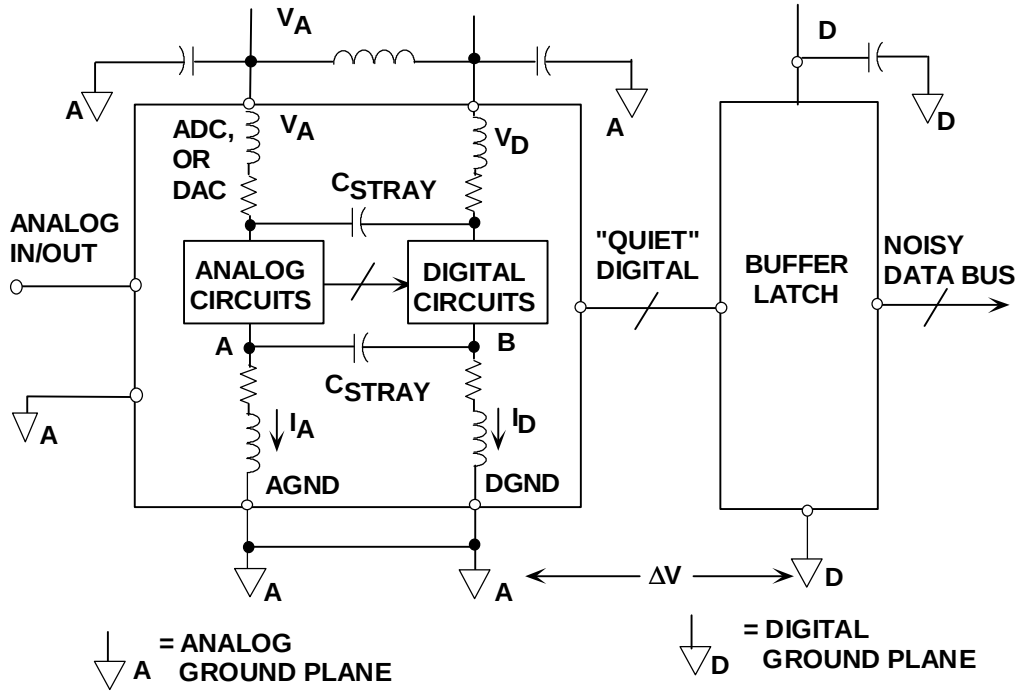
In other systems, especially high speed ones with large amounts of digital circuitry, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually desirable to use separate ground planes for the analog and the digital circuitry. On PCBs which have both analog and digital

circuits, there are two separate ground planes. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The arrangement shown in Figure 7.26 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper brads for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged.



Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. *The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog components and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 7.27 will help to explain this seeming dilemma.

PROPER GROUNDING OF ADCs, DACs, AND OTHER MIXED-SIGNAL ICs



ANALOG DEVICES

7.27

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 7.27 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

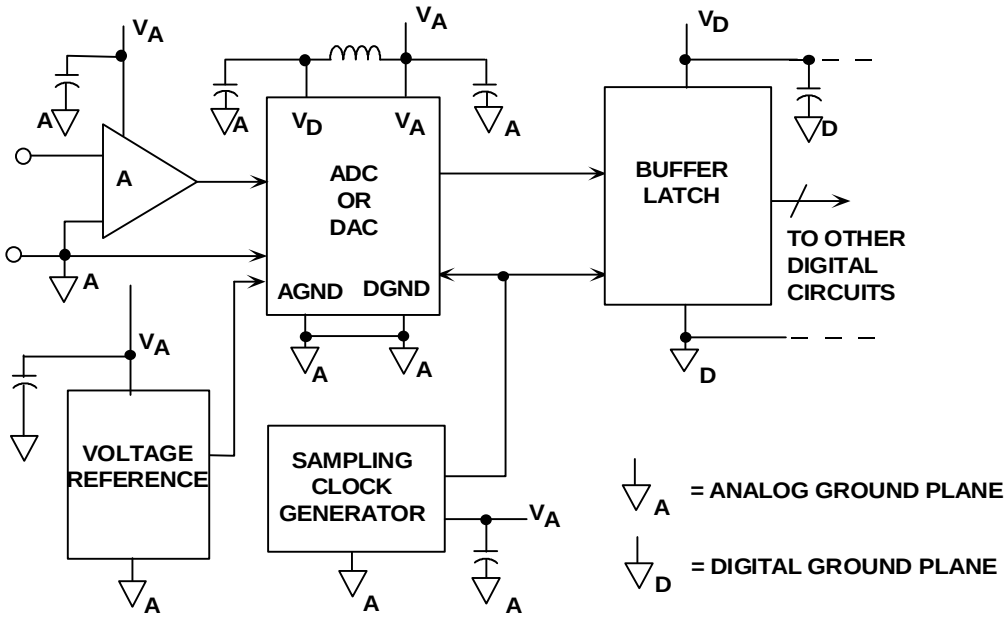
The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout (they normally can't by design). Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic

supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 7.27. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 7.27) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS



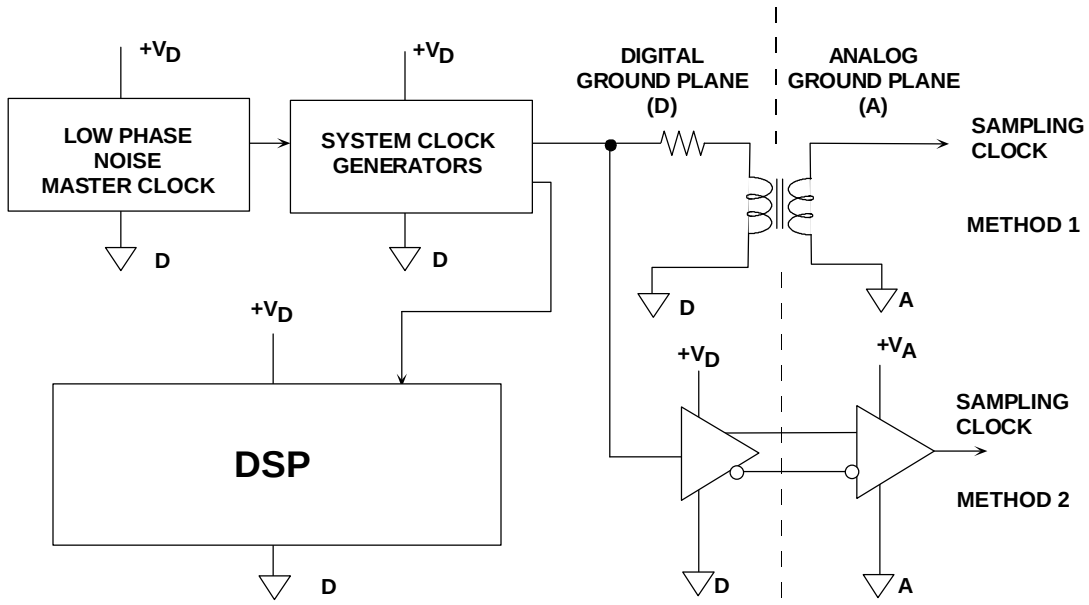
Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious. The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces degradation in system SNR.

A low phase-noise crystal oscillator should be used to generate the ADC sampling clock, because sampling clock jitter modulates the input signal and raises the noise

and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

Ideally, the sampling clock generator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. If it is passed between its origin on the digital ground plane to the ADC on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling clock signal as a differential one using either a small RF transformer or a high speed differential driver and receiver as shown in Figure 7.29. The driver and receiver should be ECL to minimize phase jitter. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

SAMPLING CLOCK DISTRIBUTION FROM DIGITAL TO ANALOG GROUND PLANES



ANALOG DEVICES

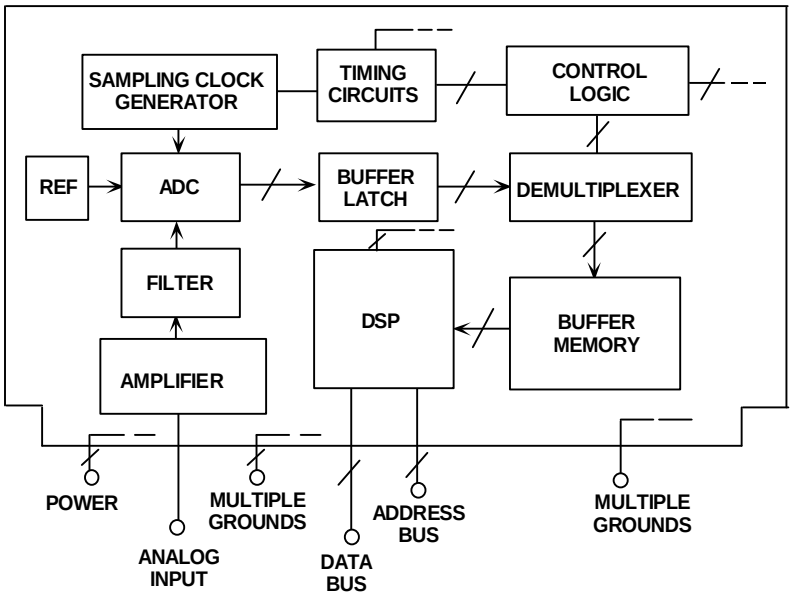
7.29

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 7.30 shows a good layout for a data acquisition board

where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING



There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

POWER SUPPLY NOISE REDUCTION AND FILTERING

Walt Jung and John McDonald

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, with the output loading of your system.

The following section discusses filter techniques for rendering a noisy switcher output *analog ready*, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes various DC-DC converters as well as popular 5V (PC type) supplies.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a *source*, a *path*, and a *receptor* [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. This section focuses on reducing switching power supply noise with external post filters.

Tools useful for combating high frequency switcher noise are shown by Figure 7.31. They differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small sized.

NOISE REDUCTION TOOLS

- **Capacitors**
- **Inductors**

- **Ferrites**
- **Resistors**
- **Linear Post Regulation**
- **PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS !!**

ANALOG DEVICES

7.31

Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of effective practical supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These can in turn can be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 7.32.

CAPACITOR SELECTION

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 µF (1)	120 µF (1)	100 µF (1)	1 µF	0.1 µF
Rated Voltage	25 V	25 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (2)	≅ 100 kHz	≅ 500 kHz	≅ 1 MHz	≅ 10 MHz	≅ 1 GHz

(1) Types shown in Figure 7.33 data
(2) Upper frequency limit is strongly size and package dependent

ANALOG DEVICES

7.32

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it

can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of μA, and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of 500μF or less[Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 5]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10μF/50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of

dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 4, 5, 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several µF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of 0.1µF or less, with 0.01µF representing a more practical upper limit.

Multilayer ceramic “chip caps” are very popular for bypassing/ filtering at 10MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

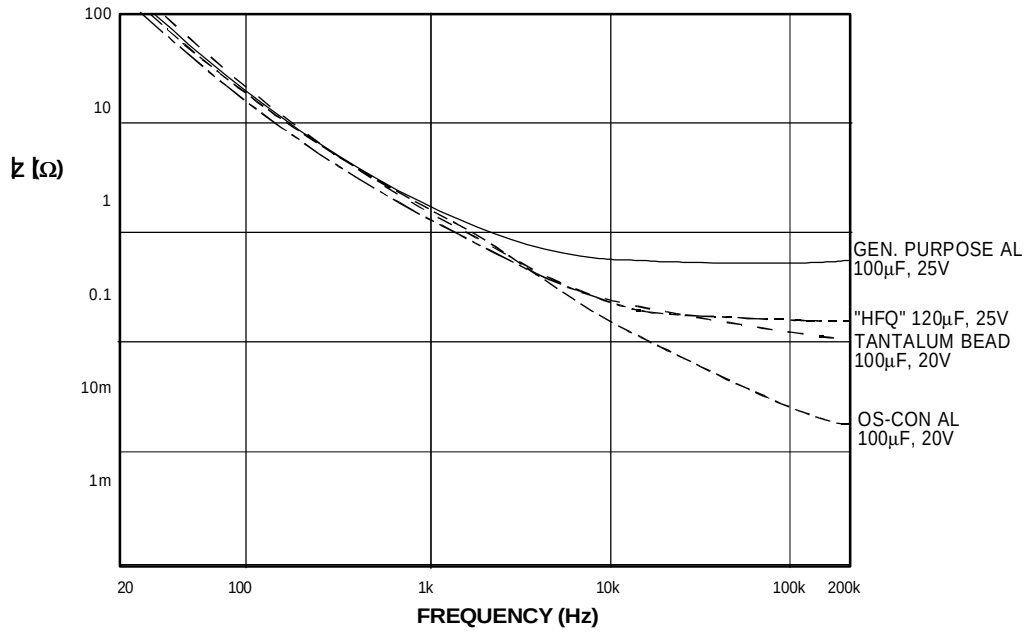
All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying “free” damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance vs. frequency plot. This occurs where |Z| falls to a minimum level, nominally equal to the capacitor’s ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the very high Q sharp resonances of film and ceramic caps, the low Q behavior of electrolytics can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at –55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100kHz is no more than 2× that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

Figure 7.33 illustrates the high frequency impedance characteristics of a number of electrolytic capacitor types, using nominal 100µF/20V samples. In these plots, the impedance, |Z|, vs. frequency over the 20Hz-200kHz range is displayed using a high resolution 4-terminal setup [Reference 8]. Shown in this display are performance samples for a 100µF/25V general purpose aluminum unit (top curve @ right), a 120µF/25V HFQ unit (next curve down @ right), a 100µF/20V tantalum bead type (next curve down @ right), and a 100µF/20V OS-CON unit (lowest curve @ right). While the HFQ and tantalum samples are close in 100kHz impedance, the

general purpose unit is about 4 times worse. The OS-CON unit is nearly an order of magnitude lower in 100kHz impedance than the tantalum and switching electrolytic types.

IMPEDANCE Z(Ω) VS. FREQUENCY FOR 100μF ELECTROLYTIC CAPACITORS (AC CURRENT = 50mA RMS)



ANALOG DEVICES

7.33

As noted, all real capacitors have parasitic elements which limit their performance. The equivalent electrical network representing a real capacitor models both ESR and ESL as well as the basic capacitance, plus some shunt resistance. In such a practical capacitor, at low frequencies the net impedance is almost purely capacitive (noted in Figure 7.33 by the 100Hz impedance). At intermediate frequencies, the net impedance is determined by ESR, for example about 0.12Ω to 0.4Ω at 125kHz, for several types. Above about 1MHz these capacitor types become inductive, with impedance dominated by the effect of ESL (not shown). All electrolytics will display impedance curves similar in general shape. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style).

Regarding inductors, *Ferrites* (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful in power supply filters [Reference 9]. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 7.34 summarize a number ferrite characteristics.

CHARACTERISTICS OF FERRITES

- **Good for frequencies above 25kHz**

- **Many sizes and shapes available including leaded "resistor style"**
- **Ferrite impedance at high frequencies is primarily resistive -- Ideal for HF filtering**
- **Low DC loss: Resistance of wire passing through ferrite is very low**
- **High saturation current**
- **Low cost**

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 11). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available.

PSpice ferrite models for Fair-Rite materials are available, and allow ferrite impedance to be estimated [see Reference 12]. These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should lead to a proper ferrite selection.

CHOOSING THE RIGHT FERRITE DEPENDS ON

- **Source of Interference**
- **Interference Frequency Range**
- **Impedance Required at Interference Frequency**
- **Environmental Conditions:**

  Temperature, AC and DC Field Strength,

Size / Space Available

■ **Don't fail to Test the Design -------**

EXPERIMENT! EXPERIMENT!

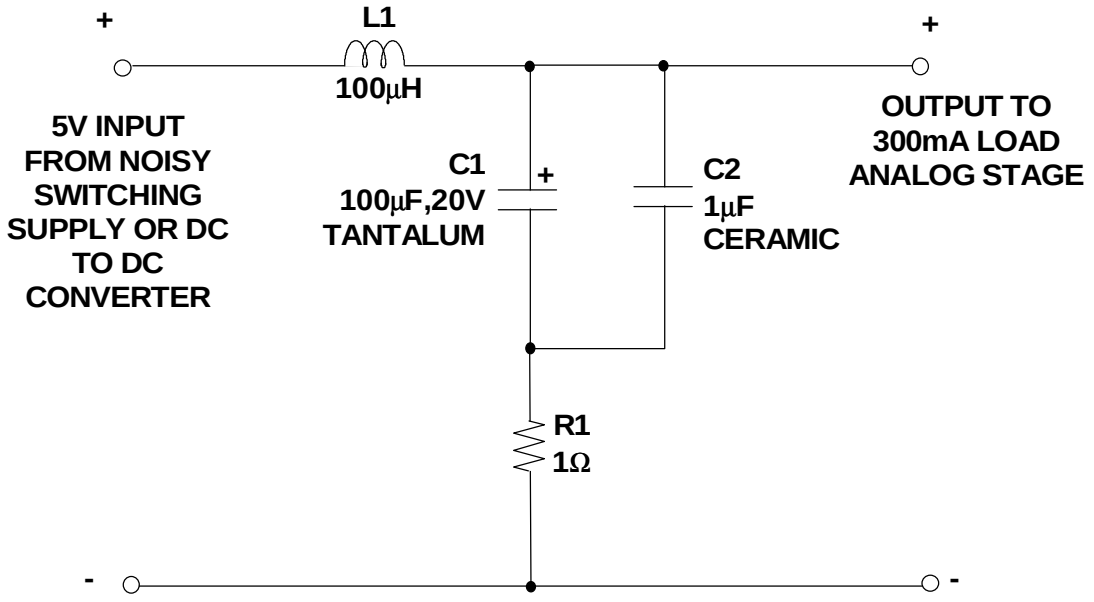
ANALOG DEVICES

7.35

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switcher's DC output so as to produce an *analog ready* 5V supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies. A basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to a 1-10MHz range. This larger filter is used as a *card entry filter* providing broadband filtering for all power entering a PC card. Smaller, more simple local filter stages are also used to provide higher frequency decoupling right at the power pins of individual stages.

Figure 7.36 illustrates a card entry filter suitable for use with switching supplies. With a low rolloff point of 1.5kHz and mV level DC errors, it is effective for a wide variety of filter applications just as shown. This filter is a single stage LC low-pass filter covering the 1kHz to 1MHz range, using carefully chosen parts. Because of component losses, it begins to lose effectiveness above a few MHz, but is still able to achieve an attenuation approaching 60dB at 1MHz.

"CARD-ENTRY" SWITCHING SUPPLY FILTER



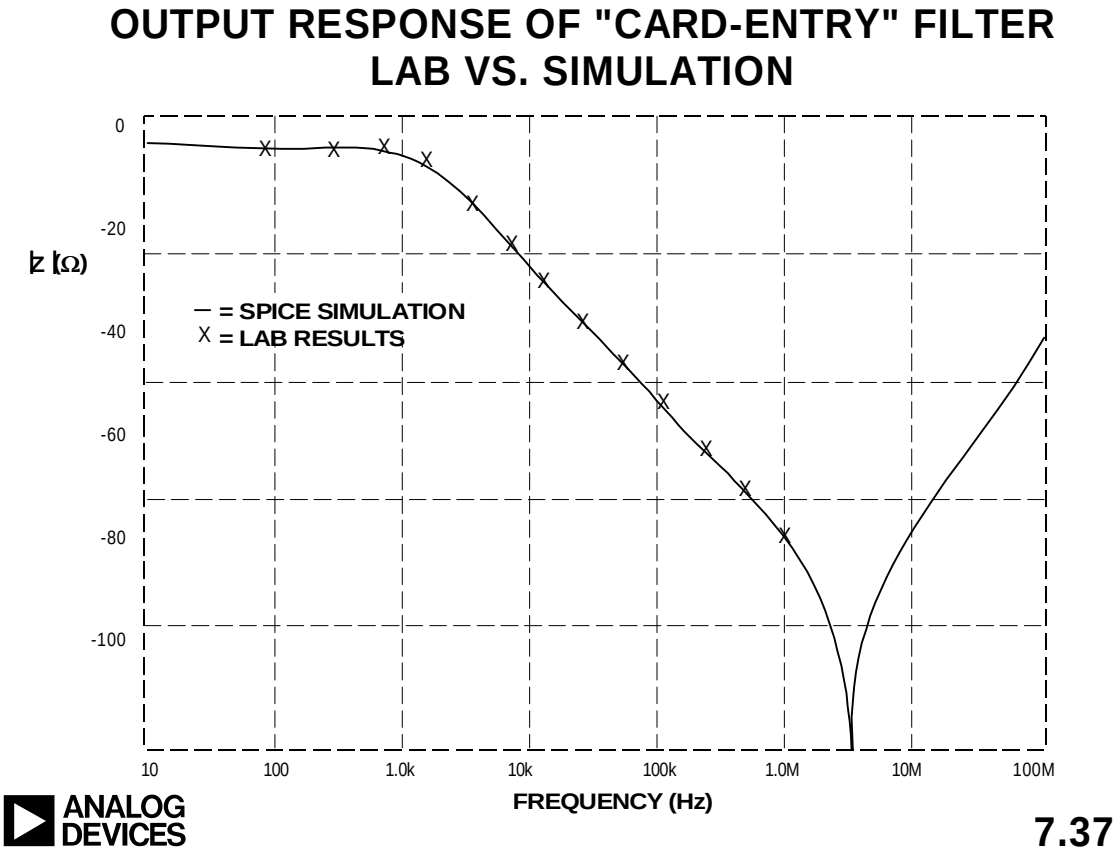
ANALOG DEVICES

7.36

The key to low DC losses is the use of input choke, L1, a ferrite-core unit selected for a low DC resistance (DCR) of <0.25Ω at the 100µH inductance (either an axial lead

type 5250 or a radial style 6000-101K choke should give comparable results) [Reference 13]. These chokes have low inductance shift with a 300mA load current, and the low DCR allows the 300mA to be passed with no more than 75mV of DC error. Alternately, resistive filtering might be used in place of L1, but a basic tradeoff here is that load current capacity will be compromised for comparable DC errors. C1, a 100µF/20V tantalum type, provides the bulk of the capacitive filtering, shunted by a 1µF multilayer ceramic.

Figure 7.37 shows the frequency response of this filter in terms of SPICE simulation and lab measurements, with good agreement between the simulation and the measurements below 1MHz.

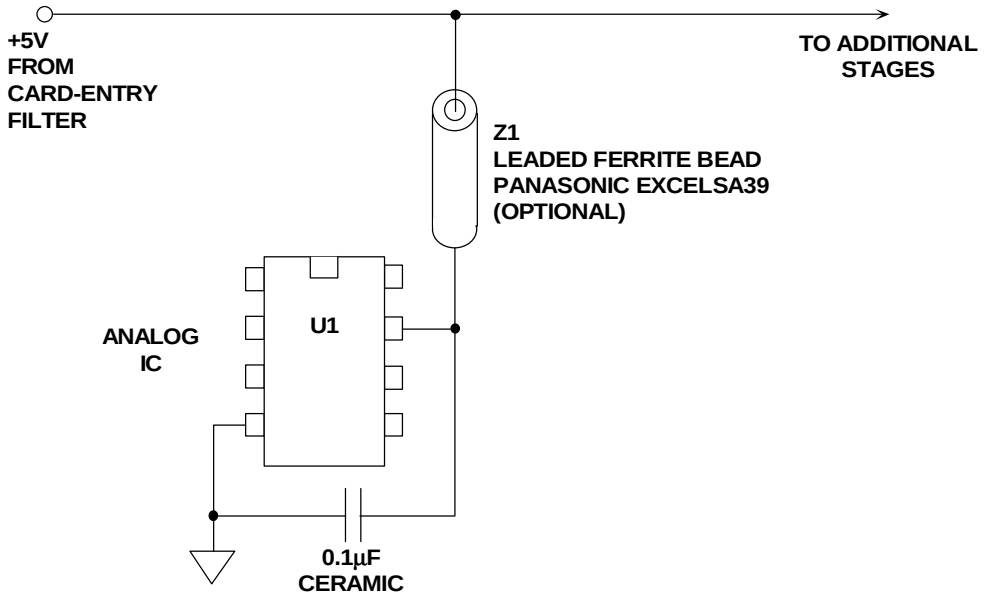


This type of filter does have some potential pitfalls, and one of them is the control of resonances. If the LCR circuit formed does not have sufficiently high resistance at the resonant frequency, amplitude peaking will result. This peaking can be minimized with resistance at two locations: in series with L1, or in series with C1+C2. Obviously, limited resistance is usable in series with L1, as this increases the DC errors.

In the filter, R1 is a damping resistor, used to control resonant peaks, and it should not be eliminated. A 1Ω value provides a slightly underdamped response, with peaking on the order of 1dB. Alternately, 1.5Ω can be used for less peaking, with a tradeoff of less attenuation below 1MHz. Note that for wide temperature range applications, all temperature sensitive filter components will need consideration.

A local high frequency filter useful with the card entry filter is shown in Figure 7.38. This simple filter can be considered an option, one which is exercised dependent upon the high frequency characteristics of the associated IC and the relative attenuation desired. It uses Z1, a leaded ferrite bead such as the Panasonic EXCELSA39, providing a resistance of more than 80Ω at 10MHz, increasing to over 100Ω at 100MHz. The ferrite bead is best used with a local high frequency decoupling cap right at the IC power pins, such as a 0.1µF ceramic unit shown.

HIGH FREQUENCY LOCALIZED DECOUPLING



ANALOG DEVICES

7.38

Both the card entry filter and the local high frequency decoupling filters are designed to filter differential-mode noise only, and use common, off the shelf components [Reference 14].

The following list summarizes the switching power supply filter layout/construction guidelines which will help ensure that the filter does the best possible job:

(1) *Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low* DL *at the rated DC current, as well as low DCR.*

(2) *Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.*

(3) *Use short leads or better yet,* leadless *components, to minimize lead inductance. This minimizes the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred.*

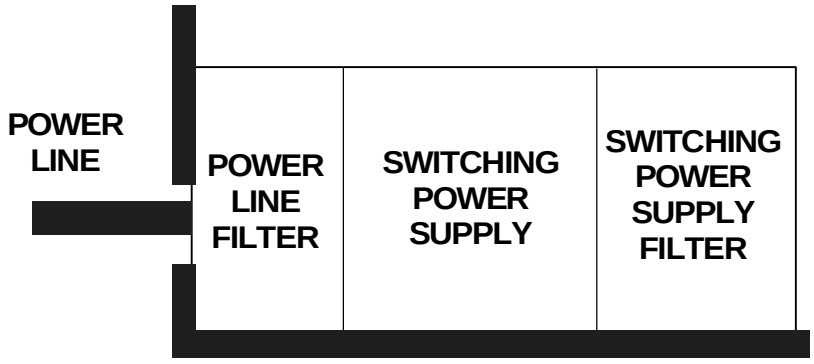
(4) *Use a large-area ground plane for minimum impedance.*

(5) *Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not* absolutely *necessary, it does instill confidence in a design when correlation is achieved*(see Reference 15).

The discussion above assumes that the incoming AC power is relatively clean, an assumption not always valid. The AC power line can also be an EMI entry/exit path! To remove this noise path and reduce emissions caused by the switching power supply or other circuits, a *power line filter* is required.

It is important to remember that AC line power can potentially be lethal! Do not experiment without proper equipment and training! All components used in power line filters should be UL approved, and the best way to provide this is to specify a packaged UL approved filter. It should be installed in such a manner that it is the first thing the AC line sees upon entering the equipment (see Figure 7.39). Standard three wire IEC style line cords are designed to mate with three terminal male connectors integral to many line filters. This is the best way to achieve this function, as it automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.

POWER LINE FILTERING IS ALSO IMPORTANT



Power Line Filter Blocks EMI from Entering or Exiting Box Via Power Lines

Commercial power line filters can be quite effective in reducing AC power-line noise. This noise generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections

(black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines. By design, most commercially available filters address both noise modes (see Reference 16).

REFERENCES: NOISE REDUCTION AND FILTERING

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6. Ian Clelland, *Metalized Polyester Film Capacitor Fills High Frequency Switcher Needs*, **PCIM**, June 1992.

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POWER SUPPLY REGULATION/CONDITIONING
Walt Jung

Many analog circuits require stable regulated voltages relatively close in potential to an unregulated source. An example would be a linear post regulator for a switching power supply, where voltage loss (dropout) is critical. This *low dropout* type of regulator is readily implemented with a rail-rail output op amp. The wide output swing and low saturation voltage enables outputs to come within a fraction of a volt of the source for medium current (<30mA) loads, such as reference applications. For higher output currents, the rail-rail voltage swing feature allows direct drive to low saturation voltage pass devices, such as power PNPs or P-channel MOSFETs. Op amps working from 3V up with the rail-rail features are most suitable here, providing power economy and maximum flexibility.

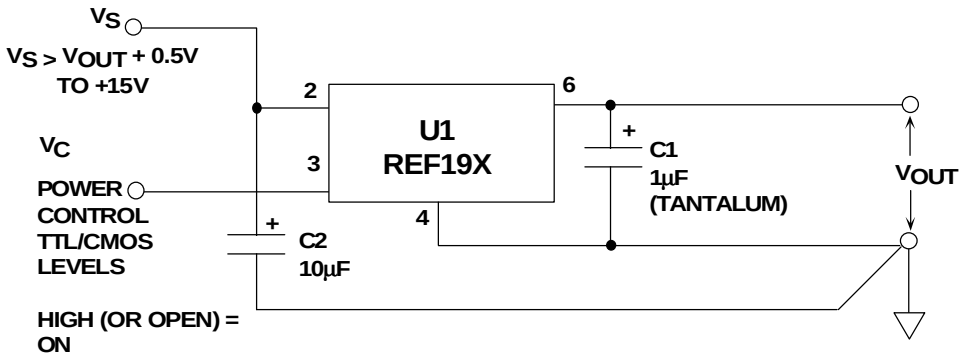
LOW DROPOUT REFERENCES

Basic references

Among the many problems in making stable DC voltage references work from 5V and lower supplies are quiescent power consumption, overall efficiency, the ability to operate down to 3V, low input/output (dropout) capability, and minimum noise output. Because low voltage supplies can't support zeners of ≅6V, low voltage references must necessarily be bandgap based-- a basic ≅1.2V potential. With low voltage systems, power conservation can be a critical issue with references, as can output DC precision.

For many applications, simple one-package fixed (or variable) voltage references with minimal external circuitry and high accuracy are attractive. Two unique features of the three terminal REF19X bandgap reference family are low power, and shutdown capability. The series allows fixed outputs from 2.048-5V to be controlled between ON and OFF, via a TTL/CMOS power control input. It provides precision reference quality for those popular voltages shown in Figure 7.40.

30mA REFERENCE FAMILY WITH OPTIONAL SHUTDOWN



U1	VOUT (V)
REF191	2.048
REF192	2.5
REF193	3.0
REF196	3.3
REF198	4.096
REF194	4.5
REF195	5.0

ANALOG DEVICES

7.40

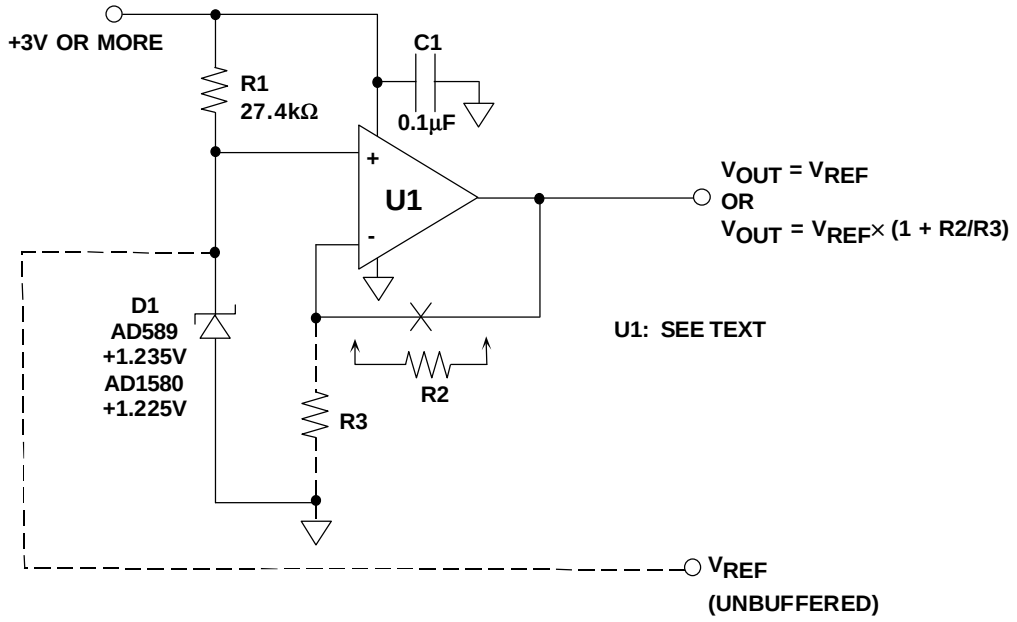
The REF19X family can be used as a simple three terminal fixed reference as per the table by tying pins 2 and 3 together, or as an ON/OFF controlled device, by programming pin 3 as noted. In addition to the shutdown capacity, the distinguishing functional features are a low dropout of 0.5V at 10mA, and a low current drain for both quiescent and shutdown states, 45 and 15µA (max.), respectively. For example, working from inputs in the range of 6.3 to 15V, a REF195 used as shown drives 5V loads at up to 30mA, with grade dependent tolerances of ±2 to ±5mV, and max TCs of 5 to 25ppm/°C. Other devices in the series provide comparable accuracy specifications, and all have low dropout features.

To maximize DC accuracy in this circuit, the output of U1 should be connected directly to the load with short heavy traces, to minimize IR drops. The common terminal (pin 4) is less critical due to lower current in this leg.

Scaled References

Another approach, one with the advantage of voltage flexibility, is to buffer/scale a low voltage reference diode. With this approach, one difficulty is getting an amplifier to work well at 3V. A workhorse solution is the low power reference and scaling buffer shown in Figure 7.41. Here a low current 1.2V, two-terminal reference diode is used for D1, either the 1.235V AD589 or the 1.225V AD1580. Resistor R1 sets the diode current, chosen for 50µA at a minimum supply of 2.7V. Obviously, loading on the unbuffered diode must be minimized at the V_{REF} node.

RAIL-TO-RAIL OUTPUT OP AMPS ALLOW GREATEST FLEXIBILITY IN LOW DROPOUT REGULATORS



ANALOG DEVICES

7.41

Amplifier U1 both buffers and optionally scales up the nominal 1.2V reference, allowing much higher source/sink currents. A higher op amp quiescent current is expended in doing this, but this is a basic tradeoff of the approach. Quiescent current is amplifier dependent, ranging from 45µA/channel with the OP196/296/496 series to 1000-2000µA/channel with the OP284 and OP279. The former series is most useful for very light loads (<2mA), while the latter series provide device dependent outputs up to 50mA. Various devices can be used in the circuit as shown, and their key specs are summarized in Figure 7.42.

OP AMPS USEFUL IN LOW VOLTAGE RAIL-RAIL REFERENCES AND REGULATORS

Device*	Iq/channel mA	Vsat(+), V(min @ mA)	Vsat(-), V (max @ mA)	Isc, mA (min)
OP193/293/493	0.017	4.20 @ 1	0.280 @ 1 (typ)	± 8
OP196/296/496	0.045	4.30 @ 1	0.430 @ 1	± 4
OP295/495	0.150 (max)	4.50 @ 1	0.110 @ 1	± 11
OP191/291/491	0.300	4.80 @ 2.5	0.075 @ 2.5	± 8.75
AD820/822/824	0.620	4.89 @ 2	0.055 @ 2	± 15
OP184/284/484	1.250 (max)	4.85 @ 2.5	0.125 @ 2.5	± 7.5

OP279	**2.000**	**4.80 @ 10**	**0.075 @ 10**	**± 45**

***Typical device specifications @ Vs = +5V, T_A = 25°C, unless otherwise noted.**

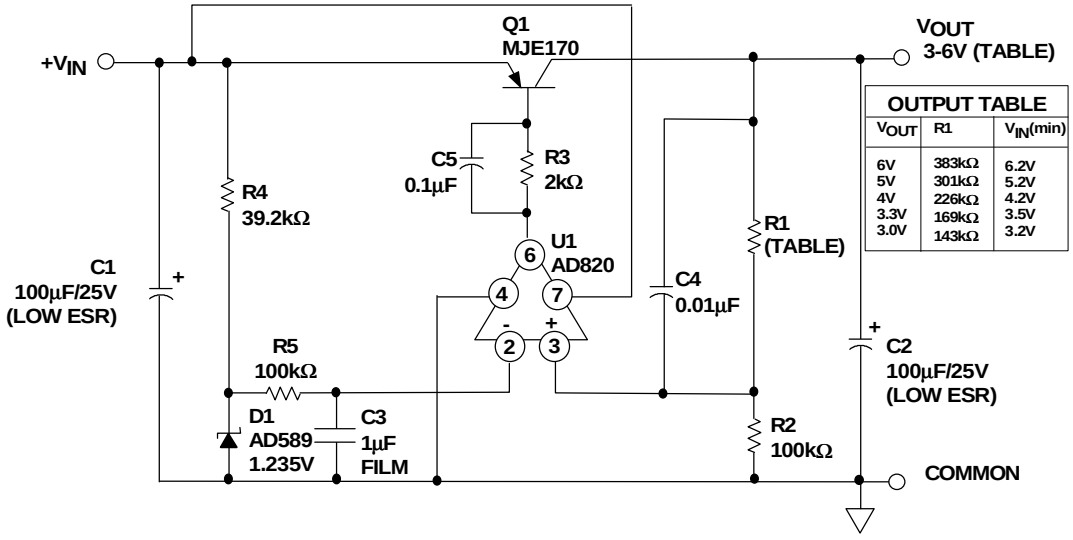
In Figure 7.41, without gain scaling resistors R2-R3, V_{OUT} is simply equal to V_{REF}. With the scaling resistors, V_{OUT} can be set anywhere between V_{REF} and the positive rail, due to the op amp's rail-rail output swing. Also, this buffered reference is inherently low dropout, allowing a +4.5V reference output on a +5V supply, for example. The general expression for V_{OUT} is shown in the figure, where V_{REF} is the reference voltage.

Amplifier standby current can be further reduced below 20µA, if an amplifier from the OP193/293/493 series is used. This will be at the expense of current drive and positive rail saturation, but does provide the lowest possible quiescent current if necessary. All devices in Figure 7.42 operate from voltages down to 3V (except the OP279, which operates at 5V).

Low Dropout Regulators

By adding a boost transistor to the basic rail-rail output low dropout reference of Figure 7.41, output currents of 100mA or more are possible, still retaining features of low standby current and low dropout voltage. Figure 7.43 shows a low dropout regulator with 800µA standby current, suitable for a variety of outputs at current levels of 100mA.

100mA LOW NOISE, LOW DROPOUT REGULATOR



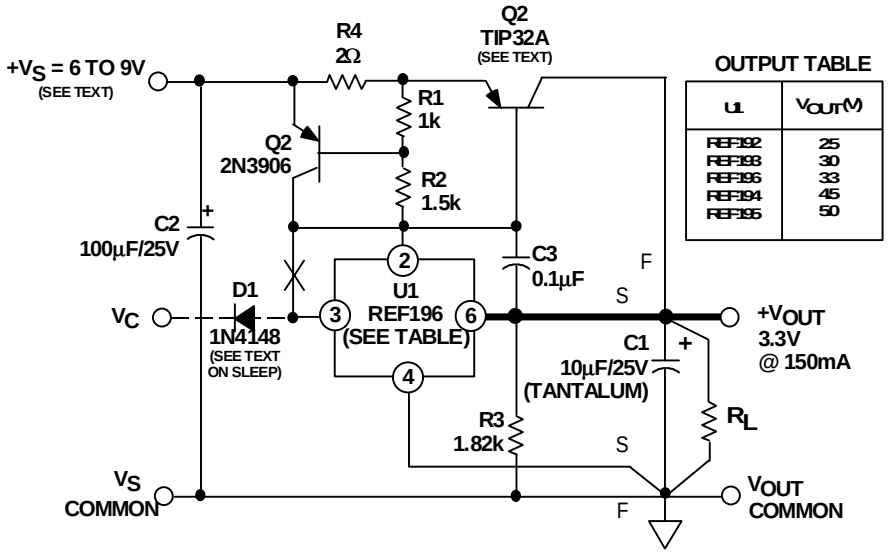
The 100mA output is achieved with a controlled gain bipolar power transistor for pass device Q1, an MJE170. Maximum output current control is provided by limiting base drive to Q1 via series resistor R3. This limits the base current to about 2mA, so the max H_{FE} of Q1 then allows no more than 500mA. This limits Q1's short circuit power dissipation to safe levels.

Overall, the circuit operates as a follower with gain, as was true in the case of Figure 7.41, so V_{OUT} has a similar output expression. The circuit is adapted for different voltages simply by programming R1 via the table. Dropout with a 100mA load is about 200mV, thus a 5V output is maintained for inputs above 5.2V (see table), and V_{OUT} levels down to 3V are possible. Step load response of this circuit is quite good, and transient error is only a few mVp-p for a 30-100mA load change. This is achieved with low ESR switching type capacitors at C1-C2, but the circuit also works with conventional electrolytics (with higher transient errors).

If desired, lowest output noise with the AD820 is reached by including the optional reference noise filter, R5-C3. Lower current op amps can also be used for lower standby current, but with larger transient errors due to reduced bandwidth.

While the 30mA rated output current of the REF19X series is higher than most reference ICs, it can be boosted to much higher levels if desired, with the addition of a PNP transistor, as shown in Figure 7.44. This circuit uses full time current limiting for protection of pass transistor shorts.

150 mA BOOSTED OUTPUT REGULATOR/REFERENCE WITH CURRENT LIMITING



In this circuit the supply current of reference U1 flows in R1-R2, developing a base drive for pass device Q1, whose collector provides the bulk of the output current. With a typical gain of 100 in Q1 for 100-200mA loads, U1 is never required to furnish more than a few mA, and this factor minimizes temperature related drift.

Short circuit protection is provided by Q2, which clamps drive to Q1 at about 300mA of load current. With separation of control/power functions, DC stability is optimum, allowing best advantage of premium grade REF19X devices for U1. Of course, load management should still be exercised. A short, heavy, low resistance conductor should be used from U1-6 to the V_{OUT} sense point “S”, where the collector of Q1 connects to the load.

Because of the current limiting, dropout voltage is raised about 1.1V over that of the REF19X devices. However, overall dropout typically is still low enough to allow operation of a 5 to 3.3V regulator/reference using the 3.3V REF-196 for U1, with a Vs of 4.5V and a load current of 150mA.

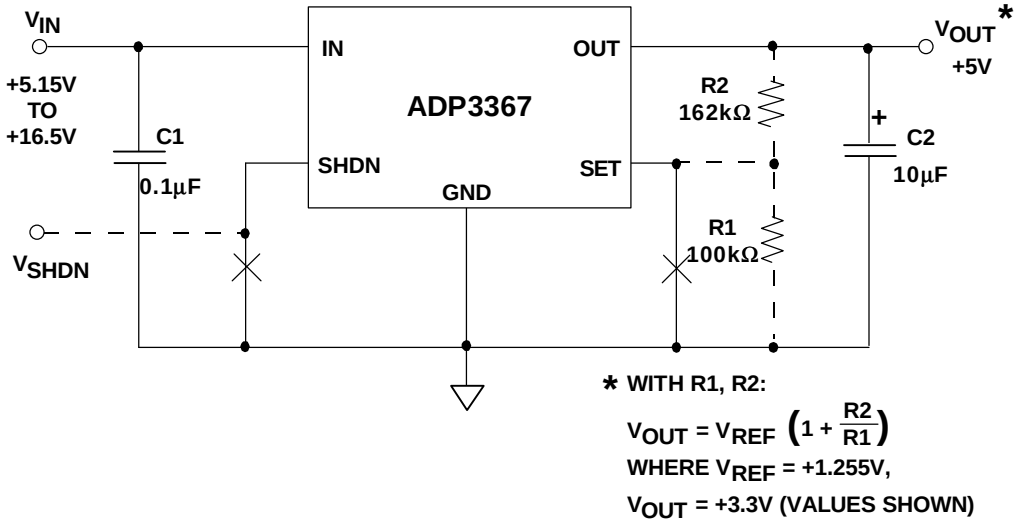
The heat sink requirements of Q1 depend upon the maximum power. With Vs = 5V and a 300mA current limit, the worst case dissipation of Q1 is 1.5W, less than the TO-220 package 2W limit. If TO-39 or TO-5 packaged devices such as the 2N4033 are used, the current limit should be reduced to keep maximum dissipation below the package rating, by raising R4. A tantalum output capacitor is used at C1 for its low ESR, and the higher value is required for stability. Capacitor C2 provides input bypassing, and can be an ordinary electrolytic.

Shutdown control of the booster stage is shown as an option, and when used, some cautions are in order. To enable shutdown control, the connection to U1-2 and U1-3 is broken at “X”, and diode D1 allows a CMOS control source to drive U1-3 for ON/OFF control. Startup from shutdown is not as clean under heavy load as it is with the basic REF19X series stand-alone, and can require several milliseconds under load. Nevertheless, it is still effective, and can fully control 150mA loads. When shutdown control is used, heavy capacitive loads should be minimized.

Dedicated low dropout linear IC regulators offer all the virtues of the discrete approaches, but in a easier-to-use compact format. The ADP3367 is such a device, providing either a fixed output of 5V ±2%, or adjustable outputs over a range of 1.3 to 16.5V, with current outputs up to 300mA. Using a CMOS architecture with a PNP pass transistor, it has a quiescent current of 25μA (max., unloaded), and a dropout voltage of 175mV (max.) with a 100mA output.

Figure 7.45 shows the basic hookup for the ADP3367, which uses the "thermal coastline" 8 pin SOIC package, which is designed for power dissipation up to 960mW. For fixed 5V outputs, R1 and R2 aren’t used, and the SET pin is grounded as shown. With the SHDN pin also grounded, this simple hookup provides a constant 5V at V_{OUT}, with the low dropout features mentioned.

300mA LOW DROPOUT FIXED/VARIABLE REGULATOR WITH OPTIONAL SHUTDOWN

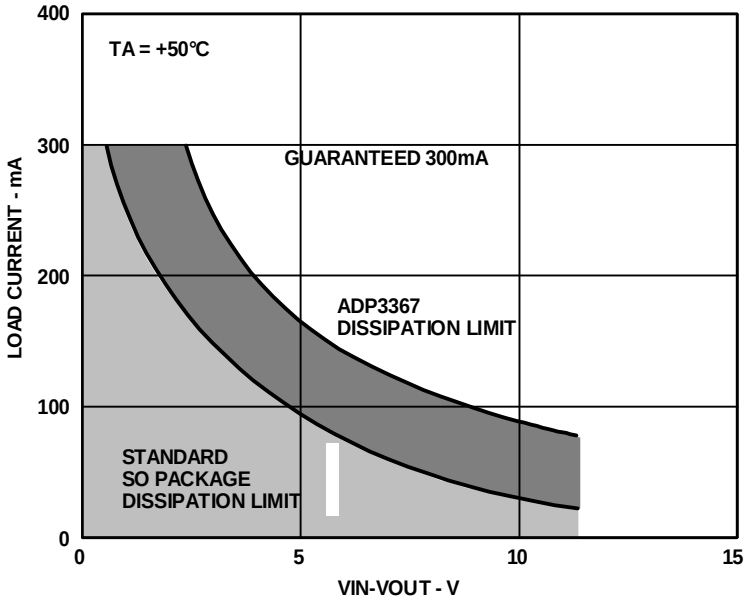


ANALOG DEVICES

7.45

The ADP3367's useful output current capacity will be dependent upon the V_{IN}-V_{OUT} differential, such that the resulting power it dissipates is contained to 960 mW or less. For example, at low input-output differences of 2.5V, up to 300mA is available. For higher input-output differences, the allowable current is reduced according to the curves shown in Figure 7.46. The upper shaded curve corresponds to the output current which is consistent with the ADP3367's package limitations. Note that the allowable output current is appreciably higher than that of a standard SO package, shown in the lower shaded curve.

ADP3367 LOAD CURRENT VS. INPUT - OUTPUT VOLTAGE



ANALOG DEVICES

7.46

The ADP3367 can be placed in a shutdown mode, which reduces the output voltage to zero and drops the standby current to less than 1μA. When implemented, shutdown is accomplished by applying a control voltage of more than 1.5V to V_{SHDN}. Otherwise, this pin should be tied to ground as shown. The SET pin has a dual function, and can be used either to select an internal divider (which provides the fixed 5V output), or it can be used with an external divider, R1-R2. When the SET pin is grounded, the internal divider is active, and the 5 V output results. When the SET pin is used with the external divider, V_{OUT} is programmed as:

$$V_{OUT} = V_{REF} * \left(1 + \frac{R2}{R1}\right)$$

where V_{REF} is 1.255V, the internal reference voltage of the ADP3367. The divider's absolute resistance values are not critical, since the input current at the SET pin is low, typically 10pA. This allows resistances of 100k - 1meg, consistent with the overall low standby power objectives. The example 1% values shown provide a 3.3V output. They can be further increased, if it is desired to lower standby current consumption below the ≅12μA resulting with the values shown.

C2, the output capacitor, is a 10μF type, and is required for regulator stability. Larger sizes are permissible, and will help improve transient response. An input bypass is also recommended, C1.

To achieve the full power capability inherent to the design, the ADP3367 should be mounted on a PCB in such as way that internally-generated heat can flow outward easily from the die to the PCB. Large area PCB copper traces should be used beneath and around the IC, and mounting should be such that the part is exposed to unrestricted air flow [see Reference 5].

REFERENCES: POWER SUPPLY REGULATION/CONDITIONING

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2. Walt Jung, *Getting the Most from IC Voltage References*, **Analog Dialogue 28-1**, 1994.

3. Walt Jung, *The Ins and Outs of 'Green' Regulators/References* , **Electronic Design Analog Applications Issue**, June 27, 1994.

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THERMAL MANAGEMENT
Walt Jung

For reliability reasons, modern semiconductor based systems are increasingly called upon to observe some form of *thermal management*. All semiconductors have some specified safe upper limit to junction temperature (T_J), usually on the order of 150°C (but sometimes 175°). Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn't be exceeded. In conservative designs, it won't be approached by less than an ample safety margin. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. The cooler semiconductors can be kept during operation, the more closely they will approach maximum useful life.

Thermal basics

The general symbol θ is used for *thermal resistance*, that is:

θ = thermal resistance, in units of °C/watt (or, °C/W).

θ_{JA} and θ_{JC} are two more specific terms used in dealing with semiconductor thermal issues, which are further explained below.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1W, as measured between two reference points. Note that this is a linear relation, so a 500mW dissipation in the same part will produce a 50°C differential, and so forth. For any power P (in watts), calculate the effective temperature differential (ΔT) in °C as:

$\Delta T = P \times \theta$

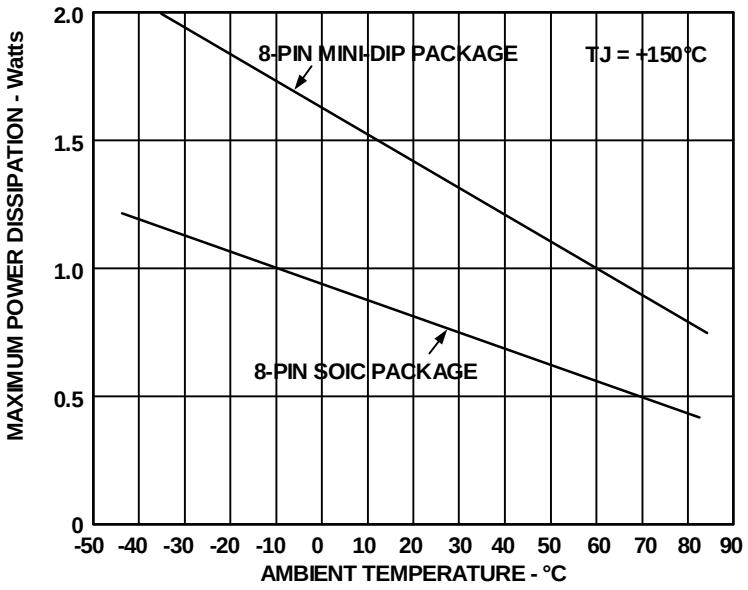
where θ is the total applicable thermal resistance. Figure 7.47 summarizes these thermal relationships.

THERMAL BASICS

- **θ = Thermal Resistance (°C/W)**
- **$\Delta T = P \times \theta$**
- **θ_{JA} = Junction - to - Ambient Thermal Resistance**
- **θ_{JC} = Junction - to - Case Thermal Resistance**
- **θ_{CA} = Case - to - Ambient Thermal Resistance**
- **$\theta_{JA} = \theta_{JC} + \theta_{CA}$**
- **$T_J = T_A + (P \times \theta_{JA})$, P = Total Device Power Dissipation**
- **$T_{J(Max)}$ = 150°C (Sometimes 175°C)**

A real example illustrating this relationship is shown by Figure 7.48. These curves indicate the maximum power dissipation vs. temperature characteristic for a device using 8 pin DIP and SOIC packaging. For a $T_{J(max)}$ of 150°C, the upper curve shows the allowable power in a DIP package. This corresponds to a θ which can be calculated by dividing the ΔT by P at any point. For example, 1W of power is allowed at a T_A of 60°C, so the ΔT is 150°C – 60°C = 90°C. Dividing by 1W gives this DIP package's θ of 90°C/W. Similarly, the SOIC package yields 160°C/W. These figures are in fact the θ_{JA} for the AD823 op amp, but they also happen to be quite similar to other 8 pin devices. Given such data as these curves, the θ_{JA} for a given device can be readily determined, as above.

MAXIMUM POWER DISSIPATION VS. TEMPERATURE FOR 8-PIN MINI-DIP AND 8-PIN SOIC PACKAGES



7.48

As the relationship signifies, to maintain a low T_J, either θ or the power dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to low maximum junction temperatures.

In semiconductors, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either the case of the device, or the *ambient temperature*, T_A, that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, θ_{JA} and θ_{JC}.

Taking the more simple case first, θ_{JA} is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs which do not dissipate serious amounts of power, that is 1W or less. θ_{JA} figures typical of op amps and other small devices are on the order of 90-100°C/W for a plastic 8 pin DIP package. It must be understood that thermal resistances are highly package dependent, as different materials have differing degrees of thermal conductivity. As a general rule of thumb, thermal resistance for the conductors within packaging materials is closely analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance (lowest θ).

A summary of the thermal resistances of various IC packages is shown in Figures 7.49 and 7.50. In general, most of these packages do not lend themselves to easy heat sink attachment (with notable exceptions, such as the older round metal can types). Devices which *are* amenable to heat sink attachment will often be noted by a θ_{JC} dramatically lower than the θ_{JA}. See for example the 15 pin SIP package (used by the AD815).

STANDARD PACKAGE THERMAL RESISTANCES - 1

Package	ADI designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment
8 pin plastic DIP	N-8	90		AD823
8 pin ceramic DIP	D-8	110	22	AD712
8 pin SOIC	R-8	160	60	
8 pin SOIC	R-8	90	60	ADP3367 Thermal Coastline
8 pin metal can	H-08A (TO-99)	150	45	OP07
10 pin metal can	H-10A (TO-100)	150	25	AD582
12 pin metal can	H-12A (TO-8)	100	30	AD841
14 pin plastic DIP	N-14	150		AD713
14 pin ceramic DIP	D-14	110	30	AD585
14 pin SOIC	R-14	120		AD813
15 pin SIP	Y-15	41	2	AD815 Through-Hole
16 pin plastic DIP	N-16	120	40	
16 pin ceramic DIP	D-16	95	22	AD524
16 pin SOIC	R-16	85		AD811

STANDARD PACKAGE THERMAL RESISTANCES - 2

Package	ADI designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment

18 pin ceramic DIP	**D-18**	**120**	**35**	**AD7575**
20 pin plastic DIP	**N-20**	**102**	**31**	
20 pin ceramic DIP	**D-20**	**70**	**10**	
20 pin SOIC	**R-20**	**74**	**24**	
24 pin plastic DIP	**N-24**	**105**	**35**	
24 pin ceramic DIP	**D-24**	**120**	**35**	**AD7547**
28 pin plastic DIP	**N-28**	**74**	**24**	
28 pin ceramic DIP	**D-28**	**51**	**8**	
28 pin SOIC	**R-28**	**71**	**23**	

θ_{JC} is the thermal resistance of a given device as measured between its *junction* and the device *case*. This form is most often used with larger power semiconductors which do dissipate significant amounts of power, that is typically more than 1W. The reason for this is that a *heat sink* generally must be used with such devices, to maintain a sufficiently low internal junction temperature. A heat sink is simply an additional low thermal resistance device attached externally to a semiconductor part to aid in heat removal. It will have some additional thermal resistance of its own, also rated in °C/W.

Rather than just a single number, θ in this case will be composed of more than one component, i.e., θ_1, θ_2, etc. Like series resistors, thermal impedances add, making a net calculation relatively simple. For example, to compute a net θ_{JA} given a relevant θ_{JC}, the thermal resistance of the heat sink, θ_{CA}, or *case* to *ambient* is added to the θ_{JC} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

and the result is the θ_{JA} for that specific circumstance.

A second form of the general overall relationship between T_J, T_A, P and θ is:

$$T_J = T_A + (P \times \theta)$$

To take a real world example, the AD815AVR power-tab packaged op amp has a θ_{JA} of 41°C/W with no additional heat sinking (the device simply operating in still air). Using it just as this would allow a power of:

$$P = (T_J - T_A)/ \theta_{JA}$$

or, (150°C – 70°C)/41°C /W, which results in an allowable power of about 2W.

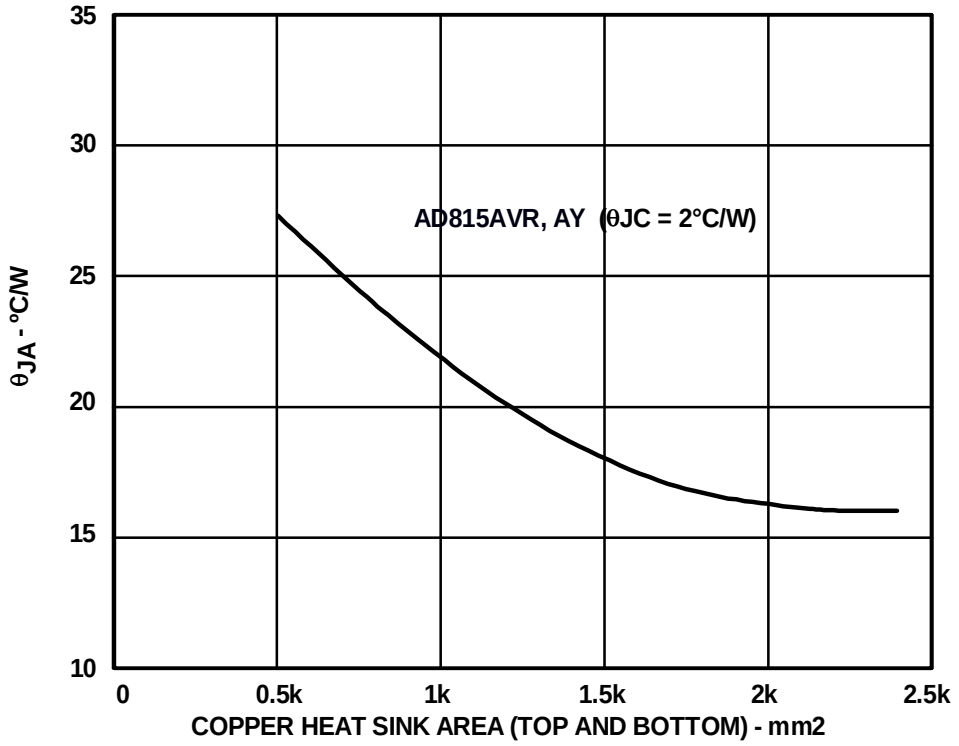
However, such a mode of operation falls short of the device's full power handling capacity. The AD815AVR's θ_{JC} is quite low at about 2°C/W, and if a heat sink of significantly less than 38°C/W is used with it, then it can dissipate much more power for a given junction temperature. A 20°C/W heat sink will allow almost twice the power to be dissipated by the same device, simply because of the lower net θ_{JA} only 22°C/W. This can be accomplished by a double-sided PCB copper plane area of 1k mm^2 [see Reference 1].

To illustrate, the general relationship of the AD815AVR and PCB heat sink net θ_{JA} is shown by Figure 7.51. In the first example cited above, full advantage of PCB heat sink area was not taken, and as the graph shows, the net θ_{JA} can be reduced to as low as ≅17°C/W by increasing the heat sink area further. The tradeoff is simply one of board area, and with a 2k mm^2 heat sink area, nearly 5W of power can be handled by the same device, assuming the same ΔT and max T_J. Of course, for the AD815 (and other devices) even more conservative operation is optionally possible by holding to a lower maximum T_J.

Note that for the data of Figure 7.51, these data assume that the AD815AVR is soldered directly to one of the dual copper PCB planes.

The power tab style package used with the AD815AVR can also be used with conventional PC mounted heat sinks, with θ_{JC} of 20°C/W and less. See Reference 2.

AD815AVR AND PCB HEAT SINK θ_{JA} VS. PCB HEAT SINK AREA



7.51

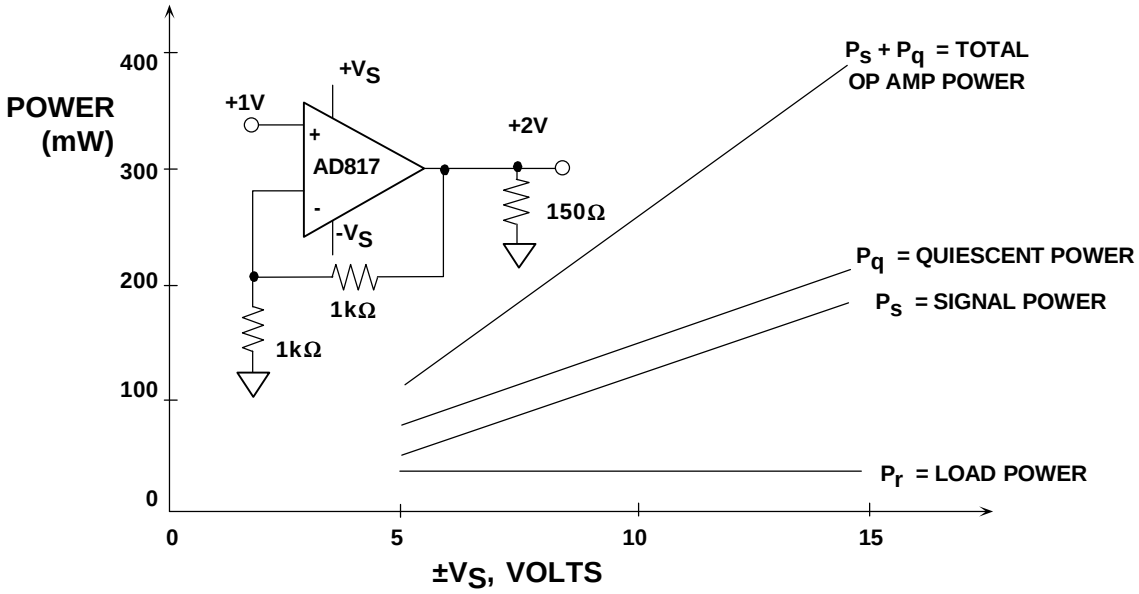
Calculating Power In Various Devices

In all instances of thermal calculations, a basic assumption is that the power is the total for a given package. With many modern devices now using more than one supply, the net total power dissipated will be the sum of all individual supply quiescent powers, plus any load dependent power. For many low output current op amps for example, total power will then be essentially the same as the quiescent. As long as this is safely less than the package can support, there is little worry. However, with some devices operable over a wide range of supply voltages, there are instances where high supply voltages and a medium to high quiescent current plus load current can be a problem.

The AD811 is such an example, being capable of operation from ±5V to ±15V, with a quiescent current of about 16mA. If operated at ±15V, the quiescent dissipation is nearly 500mW, which with a 90°C/W θ_{JA}, will push T_J to about 115°C in a 70°C ambient, high enough for concern. If the signal voltage output for such an amplifier doesn't require the ±15V supplies, then reducing the supplies will lower the quiescent power, and T_J.

To illustrate a general relationship of the power dissipated in an op amp and the power in a load for family of supply voltages, Figure 7.52 was prepared. This is a test simulation of a standard gain-of-2 non inverting amplifier driving a 150Ω load, with 1kΩ gain and feedback resistors. Assuming an input voltage of 1V DC, the 2V output across the net resistor load of 150Ω||2kΩ=140Ω will produce a power P_r of about 29mW. The AD817 amplifier operates over a supply range of ±5V to ±15V, which is the Vs sweep range for the test circuit. The op amp quiescent power P_q increases to 210mW at ±15V, while the signal power P_S dissipated by the op amp increases to 187mW at ±15V. The total power in the op amp is their sum, 397mW at ±15V. Clearly, operating relatively high current and low voltage loads from an op amp does waste considerable power, and lower voltage supplies will be much more efficient, where allowable.

AD817 OP AMP POWER DISSIPATION VS. SUPPLY VOLTAGE



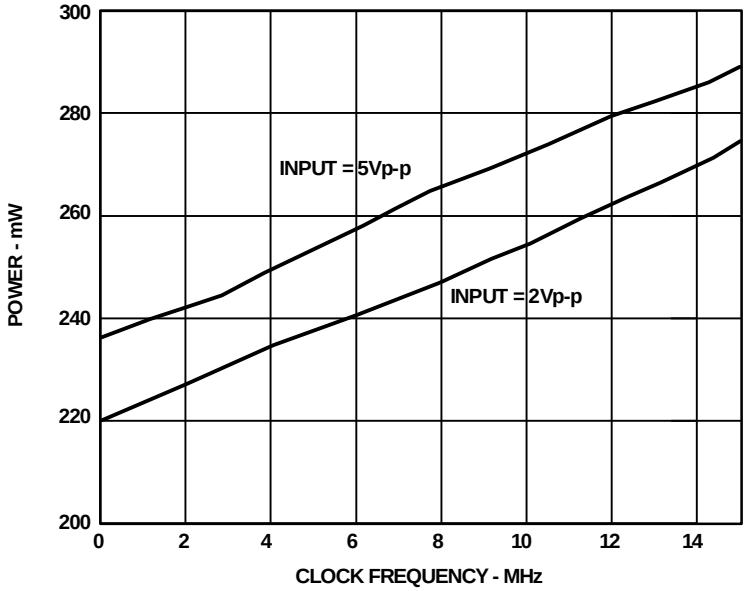
ANALOG DEVICES

7.52

Where appropriate, a clip on DIP compatible heat sink such as the AAVID 580100 can be used [Reference 3]. This series has sinks compatible with ICs of 8 through 40 pin sizes, using a staggered fin design. Performance of these (and all) heat sinks is enhanced by air movement, either through forced convection, or as a minimum, by arranging PCB cards vertically to enhance natural convection.

A/D converters can consume considerable power, although the trend is towards lower voltage and lower power dissipation. Like op amps, they are generally analyzed by adding up the total power in the package, which can then be used with the package's θ_{JA} to compute junction temperature. In adding various power totals, some care should be made to ascertain if any power is *clock dependent*. In some CMOS based designs, there can be appreciable differences in power as a function high/low clock speed as shown in Figure 7.53 for the AD9220 12-bit, 10MSPS ADC.

AD9220 12-BIT, 10MSPS CMOS ADC POWER DISSIPATION VS. SAMPLING CLOCK FREQUENCY



ANALOG DEVICES

7.53

For example, the AD9042 12 bit A/D consumes about 600mW total on two 5V supplies, and its 28 pin DIP package has a θ_{JA} of 34°C/W. What will be the max T_J for this part in a T_A of 70°C? You should get a T_J of 90.4°C ($\Delta T = 0.6W \times 34°C/W = 20.4°C$, so T_J for T_A of 70°C = 70°C + 20.4°C). This particular part is therefore in good shape for this T_A, assuming that there are no adjacent "hot spot" sources to increase the device's effective T_A.

Airflow Control

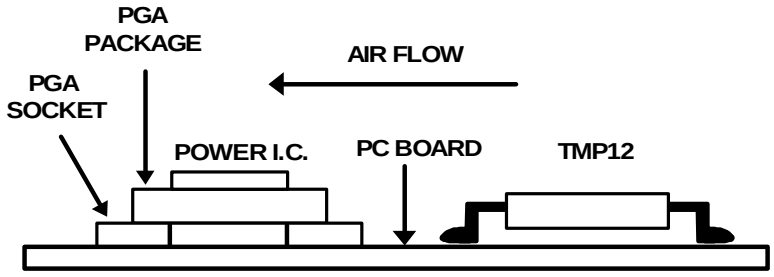
For large power dissipations and/or to maintain low T_J's, forced air movement can be used to increase air flow and aid in heat removal. In its most simple form this can consist of a continuously or thermostatically operated fan, directed across high temperature, high wattage dissipation devices such as CPUs, DSP chips, etc.

Quite often however, more sophisticated temperature control is necessary. Recent temperature monitoring and control ICs such as the TMP12, an airflow temperature sensor IC, lend themselves to such applications.

The TMP12 includes on chip two comparators, a voltage reference, a temperature sensor and a heater. The heater is used to force a predictable internal temperature rise, to match a power IC such as a microprocessor. The temperature sensing and control portions of the IC can then be programmed to respond to the temperature changes and control an external fan, so as to maintain some range of temperature. Compared to a simple thermostat, this allows infinite resolution of user control for control points and ON/OFF hysteresis.

The device is placed in an airstream near the power IC, such that both see the same stream of air, and will thus have like temperature profiles, assuming proper control of the stream. This is shown in basic form by the layout diagram of Figure 7.54.

SYSTEM USE OF TMP12 AIRFLOW SENSOR

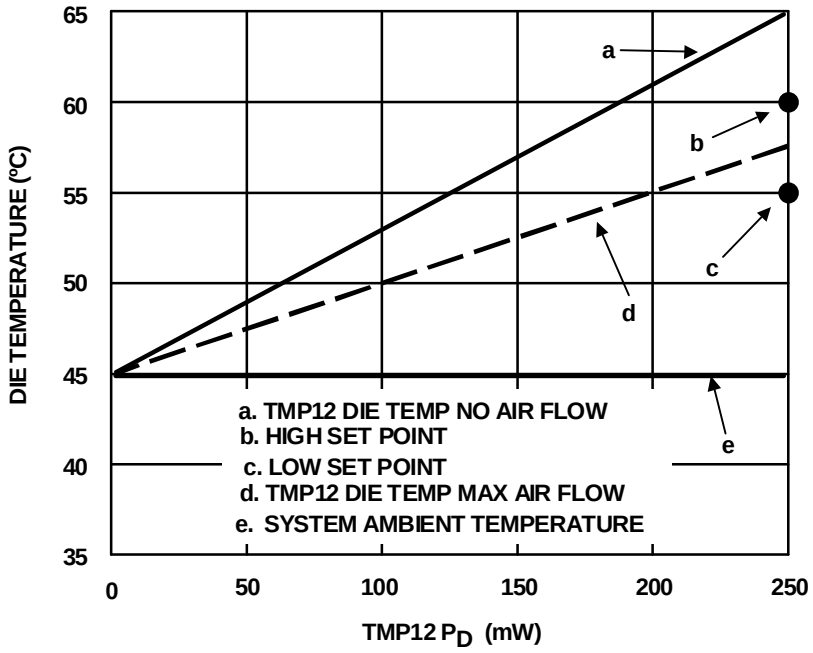


ANALOG DEVICES

7.54

With the TMP12's internal 250mW heater ON and no airflow, the TMP12 thermal profile will look like the curve "A" of Figure 7.55, and will show a 20°C rise above T_A. When airflow is provided, this same dissipation results in a lower temperature, "D". In programming the device for airspeed control, the designer can set up to two switch points, shown here symbolically by "B" and "C", which are HIGH and LOW setpoints, respectively. The basic idea is that when the IC substrate reaches point B in temperature, the external fan will be turned on to create the airstream, and lower the temperature. If the overall system setup is reasonable in terms of thermal profiling, this small IC can thus be used to indirectly control another larger and independent power source with regard to its temperature. Note that the dual mode control need not necessarily be used, in all applications. An unused comparator is simply wired high or low.

TMP12 TEMPERATURE RELATIONSHIPS



ANALOG DEVICES

7.55

Figure 7.56 shows a circuit diagram using the TMP12 as a general purpose controller. The device is connected to a 5V supply, which is also used to power a control relay and the TMP12's internal heater at pin 5. Setpoint programming of the TMP12 is accomplished by the resistor string at pins 4 through 1, R1 - R3. These resistors establish a current drain from the internal reference source at pin 4, which sets up a reference current, I_{REF}, which is set as:

$I_{REF} = (5\mu A/°C \times T_{HYS}) + 7\mu A$

In this expression, T_{HYS} is the hysteresis temperature swing desired about the setpoint, in °C, and the 7µA is recommended minimum loading of the reference. For a 2°C hysteresis for example, I_{REF} is 17µA; for 5°C, it would be 32µA.

Given a desired setpoint temperature in °C, the setpoint can be converted to a corresponding voltage. Although not available externally, the internal temperature dependent voltage of the TMP12 is scaled at 5mV/°C, and is equal to 1.49V at 25°C.

To convert a setpoint temperature to a voltage $V_{SETPOINT}$,

$V_{SETPOINT} = 1.49V + [\ 5mV/°C \times (T_{SETPOINT} - T_{25})\ ]$

where $T_{SETPOINT}$ is the desired setpoint temperature, and T_{25} is 25°C. For a 50°C high setpoint, this works out to be $V_{SETPOINT(HI)} = 1.615V$. For a lower setpoint of 35°C, the voltage $V_{SETPOINT(LO)}$ would be 1.59V.

The divider resistors are then chosen to draw the required current I_{REF} while setting the two tap voltages corresponding to $V_{SETPOINT(HI)}$ and $V_{SETPOINT(LO)}$.

$$R_{TOTAL} = V_{REF} / I_{REF}$$
$$= 2.5V / I_{REF}$$

$$R1 = [V_{REF} - V_{SETPOINT(HI)}] / I_{REF}$$
$$= [2.5V - V_{SETPOINT(HI)}] / I_{REF}$$

$$R2 = [V_{SETPOINT(HI)} - V_{SETPOINT(LO)}] / I_{REF}$$

$$R3 = V_{SETPOINT(LO)} / I_{REF}$$

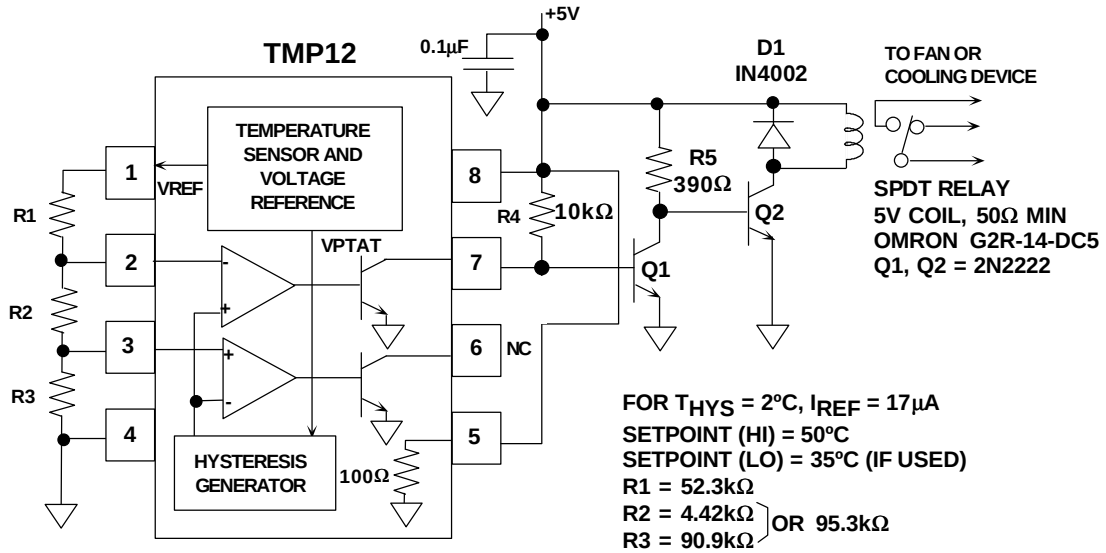
In the example of the figure, the resulting standard values for R1 - R3 correspond to the temperature/voltage setpoint examples noted above. Ideal 1% values shown give resistor related errors of only 0.1°C from ideal. Note that this is error is independent of the TMP12 temperature errors, which are ±2°C.

As noted above, both comparators of the device need not always be used, and in this case the lower comparator output is not used. For a single point 50°C controller, the 35°C setpoint is superfluous. One resistor can be eliminated by making R2 + R3 a single value of 95.3kΩ and connecting pin 3 to GND. Pin 6 should be left as a no-connect. If a greater hysteresis is desired, the resistor values will be proportionally lowered.

It is also important to minimize potential parasitic temperature errors associated with the TMP12. Although the open-collector outputs can sink up to 20mA, it is advised that currents be kept low at this node, to limit any additional temperature rise. The Q1 - Q2 transistor buffer shown in the figure raises the current drive to 100mA, allowing a 50Ω/5V coil to be driven. The relay type shown is general purpose, and many other power interfaces are possible with the TMP12. If used as shown, the relay contacts would be used to turn on a fan for airflow when the active low output at pin 7 changes, indicating the upper setpoint threshold.

A basic assumption of the TMP12's operation is that it will "mimic" another device in temperature rise. Therefore, a practical working system must be arranged and tested for proper airflow channeling, minimal disturbances from adjacent devices, etc. Some experimentation should be expected before a final setup will result.

TMP12 50º SETPOINT CONTROLLER



$$I_{REF} = \frac{V_{REF}}{R1 + R2 + R3}$$

ANALOG DEVICES

7.56

REFERENCES: THERMAL MANAGEMENT

1. *Power Consideration* Discussions, **AD815 Data Sheet**, Analog Devices.

2. *Heat Sinks for Multiwatt*Ò *Packages,* **AAVID Engineering, Inc.**, One Kool Path, Laconia, NH, 03246, (603) 528-3400.

3. *General Catalog,* **AAVID Engineering, Inc.**, One Kool Path, Laconia, NH, 03246, (603) 528-3400.

EMI/RFI CONSIDERATIONS
Adolfo A. Garcia

Electromagnetic interference (EMI) has become a hot topic in the last few years among circuit designers and systems engineers. Although the subject matter and prior art have been in existence for over the last 50 years or so, the advent of portable and high-frequency industrial and consumer electronics has provided a comfortable standard of living for many EMI testing engineers, consultants, and publishers. With the help of EDN Magazine and Kimmel Gerke Associates, this section will highlight general issues of EMC (electromagnetic compatibility) to familiarize the system/circuit designer with this subject and to illustrate proven techniques for protection against EMI.

A PRIMER ON EMI REGULATIONS

The intent of this section is to summarize the different types of electromagnetic compatibility (EMC) regulations imposed on equipment manufacturers, both voluntary and mandatory. Published EMC regulations apply at this time only to equipment and systems, and not to components. Thus, EMI *hardened* equipment does not necessarily imply that each of the components used (integrated circuits, especially) in the equipment must also be EMI *hardened*.

Commercial Equipment

The two driving forces behind commercial EMI regulations are the FCC (Federal Communications Commission) in the U. S. and the VDE (Verband Deutscher Electrotechniker) in Germany. VDE regulations are more restrictive than the FCC's with regard to emissions and radiation, but the European Community will be adding immunity to RF, electrostatic discharge, and power-line disturbances to the VDE regulations, and now requires mandatory compliance. In Japan, commercial EMC regulations are covered under the VCCI (Voluntary Control Council for Interference) standards and, implied by the name, are much looser than their FCC and VDE counterparts.

All commercial EMI regulations primarily focus on *radiated* emissions, specifically to protect nearby radio and television receivers, although both FCC and VDE standards are less stringent with respect to *conducted* interference (by a factor of 10 over radiated levels). The FCC Part 15 and VDE 0871 regulations group commercial equipment into two classes: Class A, for all products intended for business environments; and Class B, for all products used in residential applications. For example, Table 7.1 illustrates the electric-field emission limits of commercial computer equipment for both FCC Part 15 and VDE 0871 compliance.

Radiated Emission Limits for Commercial Computer Equipment

Frequency (MHz)	Class A	Class B

	(at 3 m)	(at 3 m)
30 - 88	300 µV/m	100 µV/m
88 - 216	500 µV/m	150 µV/m
216 - 1000	700 µV/m	200 µV/m

Table 7.1

In addition to the already stringent VDE emission limits, the European Community EMC standards (IEC and IEEE) now requires mandatory compliance to these additional EMI threats: Immunity to RF fields, electrostatic discharge, and power-line disturbances. All equipment/systems marketed in Europe must exhibit an immunity to RF field strengths of 1-10V/m (IEC standard 801-3), electrostatic discharge (generated by human contact or through material movement) in the range of 10-15kV (IEC standard 801-2), and power-line disturbances of 4kV EFTs (extremely fast transients, IEC standard 801-4) and 6kV lightning surges (IEEE standard C62.41).

Military Equipment

The defining EMC specification for military equipment is MIL-STD-461 which applies to radiated equipment emissions and equipment susceptibility to interference. Radiated emission limits are very typically 10 to 100 times more stringent than the levels shown in Table 7.1. Required limits on immunity to RF fields are typically 200 times more stringent (RF field strengths of 5-50mV/m) than the limits for commercial equipment.

Medical Equipment

Although not yet mandatory, EMC regulations for medical equipment are presently being defined by the FDA (Food and Drug Administration) in the USA and the European Community. The primary focus of these EMC regulations will be on immunity to RF fields, electrostatic discharge, and power-line disturbances, and may very well be more stringent than the limits spelled out in MIL-STD-461. The primary objective of the medical EMC regulations is to guarantee safety to humans.

Industrial- and Process-Control Equipment

Presently, equipment designed and marketed for industrial- and process-control applications are not required to meet pre-existing mandatory EMC regulations. In fact, manufacturers are exempt from complying to any standard in the USA. However, since industrial environments are very much electrically *hostile*, all equipment manufacturers will be required to comply with all European Community EMC regulations in 1996.

Automotive Equipment

Perhaps the most difficult and hostile environment in which electrical circuits and systems must operate is that found in the automobile. All of the key EMI threats to

electrical systems exist here. In addition, operating temperature extremes, moisture, dirt, and toxic chemicals further exacerbate the problem. To complicate matters further, standard techniques (ferrite beads, feed-through capacitors, inductors, resistors, shielded cables, wires, and connectors) used in other systems are not generally used in automotive applications because of the cost of the additional components.

Presently, automotive EMC regulations, defined by the very comprehensive SAE Standards J551 and J1113, are not yet mandatory. They are, however, very rigorous. SAE standard J551 applies to vehicle-level EMC specifications, and standard J1113 (functionally similar to MIL-STD-461) applies to all automotive electronic modules. For example, the J1113 specification requires that electronic modules cannot radiate electric fields greater than 300nV/m at a distance of 3 meters. This is roughly 1000 times more stringent than the FCC Part 15 Class A specification. In many applications, automotive manufacturers are imposing J1113 RF field immunity limits on *each of the active components* used in these modules. Thus, in the very near future, automotive manufacturers will require that IC products comply with existing EMC standards and regulations.

EMC Regulations' Impact on Design

In all these applications and many more, complying with mandatory EMC regulations will require careful design of individual circuits, modules, and systems using established techniques for cable shielding, signal and power-line filtering against both small- and large-scale disturbances, and sound multi-layer PCB layouts. The key to success is to incorporate sound EMC principles early in the design phase to avoid time-consuming and expensive redesign efforts.

A DIAGNOSTIC FRAMEWORK FOR EMI/RFI PROBLEM SOLVING

With any problem, a strategy should be developed before any effort is expended trying to solve it. This approach is similar to the scientific method: initial circuit misbehavior is noted, theories are postulated, experiments designed to test the theories are conducted, and results are again noted. This process continues until all theories have been tested and expected results achieved and recorded. With respect to EMI, a problem solving framework has been developed. As shown in Figure 7.57, the model suggested by Kimmel-Gerke in [Reference 1] illustrates that all three elements (a *source*, a *receptor* or *victim*, and a *path* between the two) must exist in order to be considered an EMI problem. The sources of electromagnetic interference can take on many forms, and the ever-increasing number of portable instrumentation and personal communications/computation equipment only adds the number of possible sources and receptors.

A DIAGNOSTIC FRAMEWORK FOR EMI

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ANY INTERFERENCE PROBLEM CAN BE BROKEN DOWN INTO:

- **The SOURCE of interference**

- **The RECEPTOR of interference**
- **The PATH coupling the source to the receptor**

SOURCES	PATHS	RECEPTORS
Microcontroller ◆ **Analog** ◆ **Digital**	**Radiated** ◆ **EM Fields** ◆ **Crosstalk** **Capacitive** **Inductive**	**Microcontroller** ◆ **Analog** ◆ **Digital**
ESD		**Communications** ◆ **Receivers**
Communications Transmitters	**Conducted**	
Power Disturbances	◆ **Signal**	**Other Electronic Systems**
Lightning	◆ **Power** ◆ **Ground**	

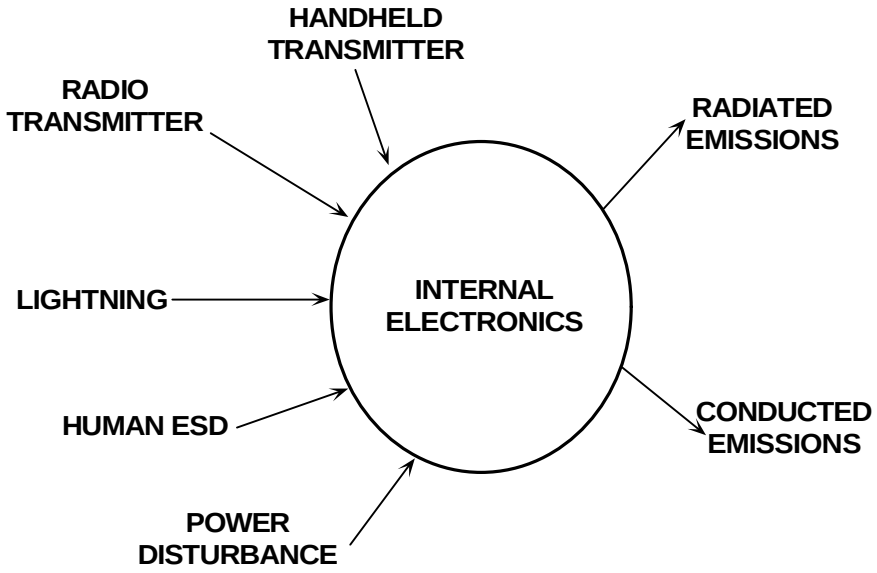
ANALOG DEVICES

7.57

Interfering signals reach the receptor by *conduction* (the circuit or system interconnections) or *radiation* (parasitic mutual inductance and/or parasitic capacitance). In general, if the frequencies of the interference are less than 30MHz, the primary means by which interference is coupled is through the *interconnects*. Between 30MHz and 300MHz, the primary coupling mechanism is *cable radiation and connector leakage*. At frequencies greater than 300MHz, the primary mechanism is *slot and board radiation*. There are many cases where the interference is broadband, and the coupling mechanisms are combinations of the above.

When all three elements exist together, a framework for solving any EMI problem can be drawn from Figure 7.58. There are three types of interference with which the circuit or system designer must contend. The first type of interference is that generated by and emitted from an instrument; this is known as circuit/system *emission* and can be either *conducted* or *radiated*. An example of this would be the personal computer. Portable and desktop computers must pass the stringent FCC Part 15 specifications prior to general use.

THREE TYPES OF INTERFERENCE
EMISSIONS - IMMUNITY - INTERNAL



ANALOG DEVICES

7.58

The second type of interference is circuit or system *immunity*. This describes the behavior of an instrument when it is exposed to large electromagnetic fields, primarily electric fields with an intensity in the range of 1 to 10V/m at a distance of 3 meters. Another term for immunity is *susceptibility*, and it describes circuit/system behavior against radiated or conducted interference.

The third type of interference is *internal*. Although not directly shown on the figure, internal interference can be high-speed digital circuitry within the equipment which affects sensitive analog (or other digital circuitry), or noisy power supplies which can contaminate both analog and digital circuits. Internal interference often occurs between digital and analog circuits, or between motors or relays and digital circuits. In mixed signal environments, the digital portion of the system often interferes with analog circuitry. In some systems, the internal interference reaches such high levels that even very high-speed digital circuitry can affect other low-speed digital circuitry as well as analog circuits.

In addition to the source-path-receptor model for analyzing EMI-related problems, Kimmel Gerke Associates have also introduced the FAT-ID concept [Reference 1]. FAT-ID is an acronym that describes the five key elements inherent in any EMI problem. These five key parameters are: *frequency*, *amplitude*, *time*, *impedance*, and *distance*.

The *frequency* of the offending signal suggests its path. For example, the path of low-frequency interference is often the circuit conductors. As the interference frequency increases, it will take the path of least impedance, usually stray capacitance. In this case, the coupling mechanism is radiation.

Time and frequency in EMI problems are interchangeable. In fact, the physics of EMI have shows that the time response of signals contains all the necessary

information to construct the spectral response of the interference. In digital systems, both the signal rise time and pulse repetition rate produce spectral components according to the following relationship:

$$f_{EMI} = \frac{1}{\pi \cdot t_{rise}} \qquad \text{Eq. 7.1}$$

For example, a pulse having a 1ns rise time is equivalent to an EMI frequency of over 300MHz. This time-frequency relationship can also be applied to high-speed analog circuits, where slew rates in excess of 1000V/µs and gain-bandwidth products greater than 500MHz are not uncommon.

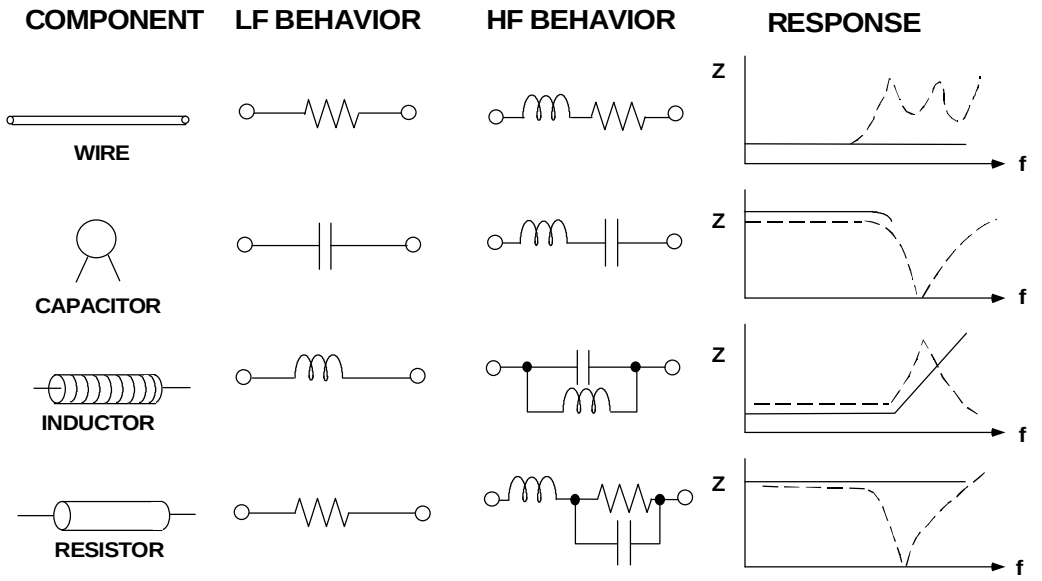
When this concept is applied to instruments and systems, EMI emissions are again functions of signal rise time and pulse repetition rates. Spectrum analyzers and high speed oscilloscopes used with voltage and current probes are very useful tools in quantifying the effects of EMI on circuits and systems.

Another important parameter in the analysis of EMI problems is the physical dimensions of cables, wires, and enclosures. Cables can behave as either passive antennas (receptors) or very efficient transmitters (sources) of interference. Their physical length and their shield must be carefully examined where EMI is a concern. As previously mentioned, the behavior of simple conductors is a function of length, cross-sectional area, and frequency. Openings in equipment enclosures can behave as slot antennas, thereby allowing EMI energy to affect the internal electronics.

PASSIVE COMPONENTS: YOUR ARSENAL AGAINST EMI

Minimizing the effects of EMI requires that the circuit/system designer be completely aware of the primary arsenal in the battle against interference: *passive components*. To use successfully these components, the designer must understand their non-ideal behavior. For example, Figure 7.59 illustrates the *real* behavior of the passive components used in circuit design. At very high frequencies, wires become transmission lines, capacitors become inductors, inductors become capacitors, and resistors behave as resonant circuits.

ALL PASSIVE COMPONENTS EXHIBIT "NON IDEAL" BEHAVIOR



ANALOG DEVICES

7.59

A specific case in point is the frequency response of a simple wire compared to that of a ground plane. In many circuits, wires are used as either power or signal returns, and there is no ground plane. A wire will behave as a very low resistance (less than 0.02Ω/ft for 22-gauge wire) at low frequencies, but because of its parasitic inductance of approximately 20nH/inch, it becomes inductive at frequencies above 13kHz. Furthermore, depending on size and routing of the wire and the frequencies involved, it ultimately becomes a transmission line with an uncontrolled impedance. From our knowledge of RF, unterminated transmission lines become antennas with gain. On the other hand, large area ground planes are much more well-behaved, and maintain a low impedance over a wide range of frequencies. With a good understanding of the behavior of *real* components, a strategy can now be developed to find solutions to most EMI problems.

RADIO FREQUENCY INTERFERENCE

The world is rich in radio transmitters: radio and TV stations, mobile radios, computers, electric motors, garage door openers, electric jackhammers, and countless others. All this electrical activity can affect circuit/system performance and, in extreme cases, may render it inoperable. Regardless of the location and magnitude of the interference, circuits/systems must have a minimum level of immunity to radio frequency interference (RFI). The next section will cover two general means by which RFI can disrupt normal instrument operation: the direct effects of RFI sensitive analog circuits, and the effects of RFI on shielded cables.

Two terms are typically used in describing the sensitivity of an electronic system to RF fields. In communications, radio engineers define *immunity* to be an instrument's *susceptibility to the applied RFI power density at the unit*. In more general EMI analysis, the *electric-field intensity* is used to describe RFI stimulus.

For comparative purposes, Equation 7.2 can be used to convert electric-field intensity to power density and vice-versa:

$$\vec{E}\left(\frac{V}{m}\right) = 61.4\sqrt{P_T\left(\frac{mW}{cm^2}\right)} \quad \text{Eq. 7.2}$$

where E = Electric Field Strength, in volts per meter, and
P_T = Transmitted power, in milliwatts per cm^2.

From the standpoint of the source-path-receptor model, the *strength of the electric field*, E, surrounding the receptor is a function of *transmitted power*, *antenna gain*, and *distance* from the source of the disturbance. An approximation for the electric-field intensity (for both near- and far-field sources) in these terms is given by Equation 7.3:

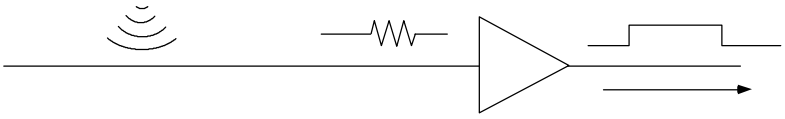
$$\vec{E}\left(\frac{V}{m}\right) = 5.5\left(\frac{\sqrt{P_T \cdot G_A}}{d}\right) \quad \text{Eq. 7.3}$$

where E = Electric field intensity, in V/m;
P_T = Transmitted power, in mW/cm^2;
G_A = Antenna gain (numerical); and
d = distance from source, in meters

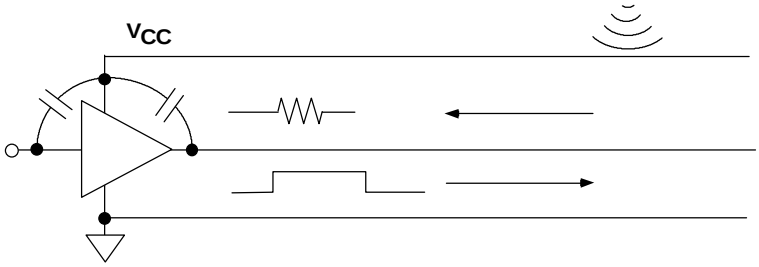
For example, a 1W hand-held radio at a distance of 1 meter can generate an electric-field of 5.5V/m, whereas a 10kW radio transmission station located 1km away generates a field smaller than 0.6V/m.

Analog circuits are generally more sensitive to RF fields than digital circuits because analog circuits, operating at high gains, must be able to resolve signals in the microvolt/millivolt region. Digital circuits, on the other hand, are more immune to RF fields because of their larger signal swings and noise margins. As shown in Figure 7.60, RF fields can use inductive and/or capacitive coupling paths to generate noise currents and voltages which are amplified by high-impedance analog instrumentation. In many cases, out-of-band noise signals are detected and rectified by these circuits. The result of the RFI rectification is usually unexplained offset voltage shifts in the circuit or in the system.

RFI CAN CAUSE RECTIFICATION IN SENSITIVE ANALOG CIRCUITS



■ **INPUTS PICK UP HIGH FREQUENCY ENERGY ON SIGNAL LINE, WHICH IS DETECTED BY THE AMPLIFIER**



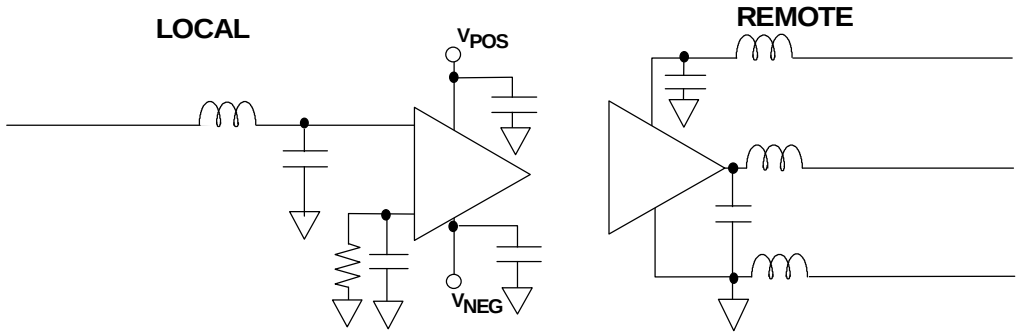
■ **OUTPUT DRIVERS CAN BE JAMMED, TOO: ENERGY COUPLES BACK TO INPUT VIA V_{CC} OR SIGNAL LINE AND THEN IS DETECTED OR AMPLIFIED**

ANALOG DEVICES

7.60

There are techniques that can be used to protect analog circuits against interference from RF fields (see Figure 7.61). The three general points of RFI coupling are *signal inputs*, *signal outputs*, and *power supplies*. At a minimum, all power supply pin connections on analog and digital ICs should be decoupled with 0.1µF ceramic capacitors. As was shown in Reference 3, low-pass filters, whose cutoff frequencies are set no higher than 10 to 100 times the signal bandwidth, can be used at the inputs and the outputs of signal conditioning circuitry to filter noise.

KEEPING RFI AWAY FROM ANALOG CIRCUITS



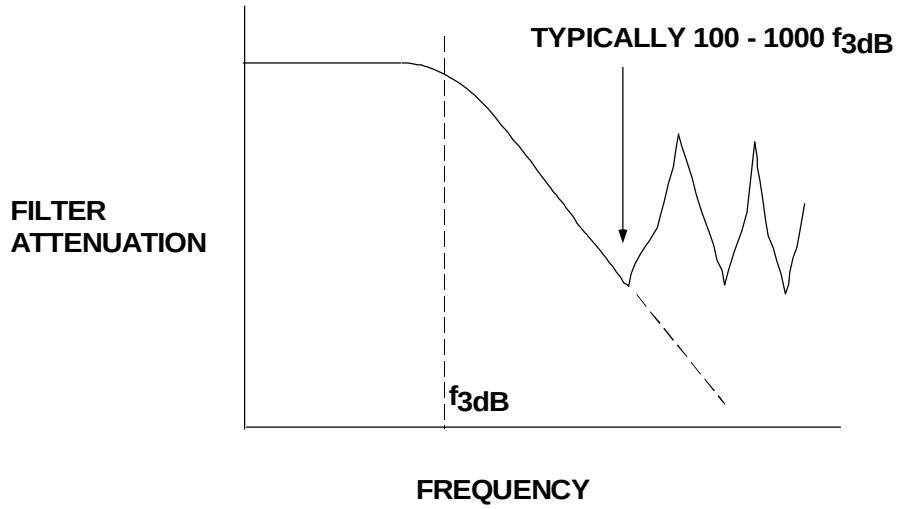
- **Decouple all voltage supplies to analog chip with high-frequency capacitors**
- **Use high-frequency filters on all lines that leave the board**
- **Use high-frequency filters on the voltage reference if it is not grounded**

ANALOG DEVICES

7.61

Care must be taken to ensure that the low pass filters (LPFs) are effective at the highest RF interference frequency expected. As illustrated in Figure 7.62, real low-pass filters may exhibit *leakage* at high frequencies. Their inductors can lose their effectiveness due to parasitic capacitance, and capacitors can lose their effectiveness due to parasitic inductance. A rule of thumb is that a conventional low-pass filter (made up of a single capacitor and inductor) can begin to *leak* when the applied signal frequency is 100 to 1000 higher than the filter's cutoff frequency. For example, a 10kHz LPF would not be considered very efficient at filtering frequencies above 1MHz.

A SINGLE LOW PASS FILTER LOSES EFFECTIVENESS AT 100 - 1000 f_{3dB}

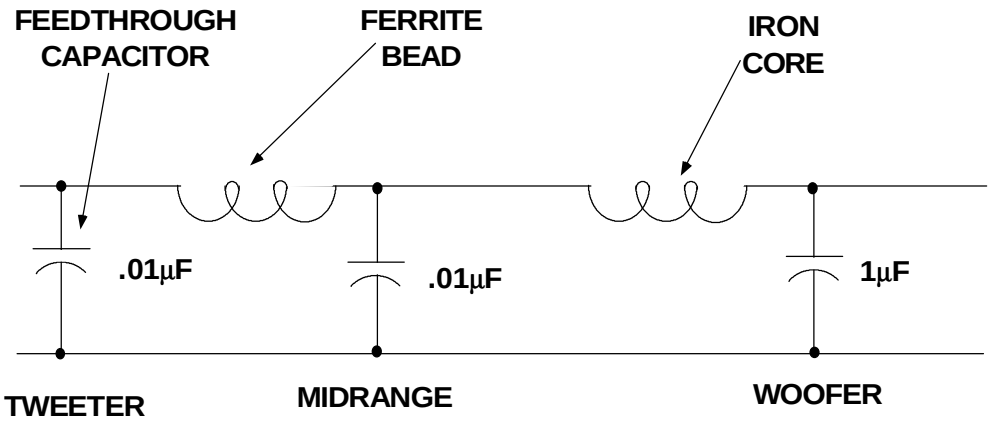


ANALOG DEVICES

7.62

Rather than use one LPF stage, it is recommended that the interference frequency bands be separated into *low-band*, *mid-band*, and *high-band*, and then use individual filters for each band. Kimmel Gerke Associates use the stereo speaker analogy of *woofer-midrange-tweeter* for RFI low-pass filter design illustrated in Figure 7.63. In this approach, low frequencies are grouped from 10kHz to 1MHz, mid-band frequencies are grouped from 1MHz to 100MHz, and high frequencies grouped from 100MHz to 1GHz. In the case of a shielded cable input/output, the high frequency section should be located close to the shield to prevent high-frequency leakage at the shield boundary. This is commonly referred to as *feed-through* protection. For applications where shields are not required at the inputs/outputs, then the preferred method is to locate the high frequency filter section as close the analog circuit as possible. This is to prevent the possibility of pickup from other parts of the circuit.

MULTISTAGE FILTERS ARE MORE EFFECTIVE



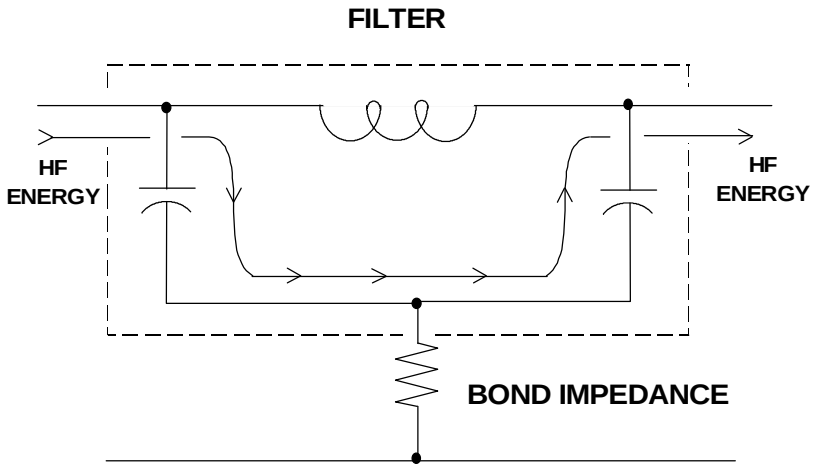
STEREO SPEAKER ANALOGY

ANALOG DEVICES

7.63

Another cause of filter failure is illustrated in Figure 7.64. If there is any impedance in the ground connection (for example, a long wire or narrow trace connected to the ground plane), then the high-frequency noise uses this impedance path to bypass the filter completely. Filter grounds must be broadband and tied to low-impedance points or planes for optimum performance. High frequency capacitor leads should be kept as short as possible, and low-inductance surface-mounted ceramic chip capacitors are preferable.

NON-ZERO (INDUCTIVE AND/OR RESISTIVE) FILTER GROUND REDUCES EFFECTIVENESS

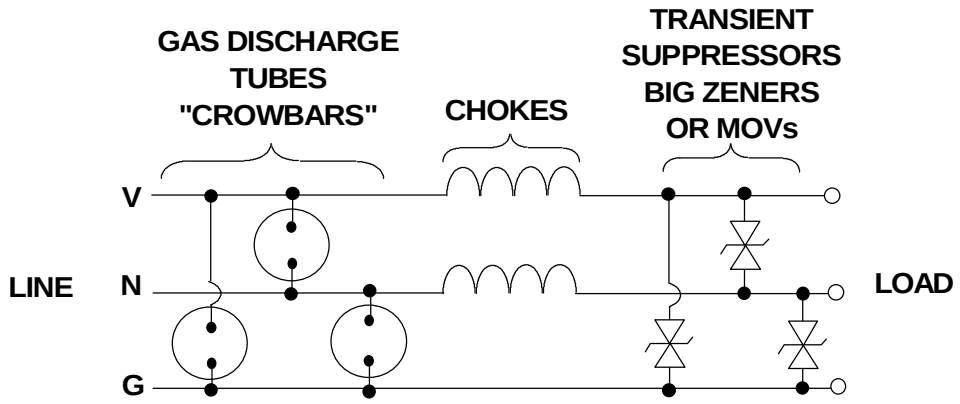


SOLUTIONS FOR POWER-LINE DISTURBANCES

The goal of this next section is not to describe in detail all the circuit/system failure mechanisms which can result from power-line disturbances or faults. Nor is it the intent of this section to describe methods by which power-line disturbances can be prevented. Instead, this section will describe techniques that allow circuits and systems to accommodate *transient* power-line disturbances.

Figure 7.65 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes (clamps) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.

POWER LINE DISTURBANCES CAN GENERATE EMI



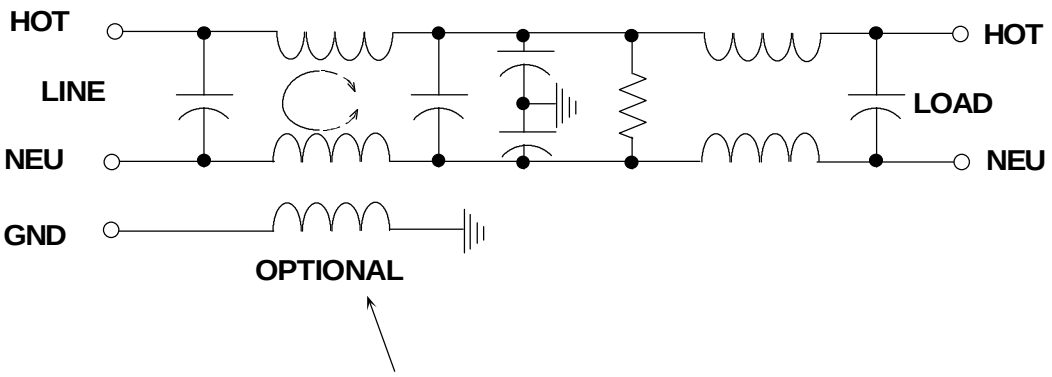
■ **COMMON-MODE AND DIFFERENTIAL MODE PROTECTION**

ANALOG DEVICES

7.65

Commercial EMI filters, as illustrated in Figure 7.66, can be used to filter less catastrophic transients or high-frequency interference. These EMI filters provide both common-mode and differential mode filtering as in Figure 7.66. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of this choke cannot be too large, however, because its resistance may affect power-line fault clearing. These filters work in both directions: they are not only protect the equipment from surges on the power line but also prevent transients from the internal switching power supplies from corrupting the power line.

SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER



NOTE: OPTIONAL CHOKE ADDED FOR COMMON-MODE PROTECTION

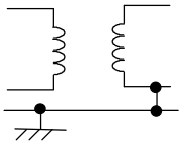
ANALOG DEVICES

7.66

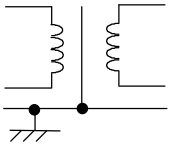
Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1MHz), or for transients with rise and fall times greater than 300ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10ns) or those caused by high-amplitude electrostatic discharge (1 to 3ns). As illustrated in Figure 7.67, isolation transformers can be designed for various levels of differential- or common-mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.

FARADAY SHIELDS IN ISOLATION TRANSFORMERS PROVIDE INCREASING LEVELS OF PROTECTION

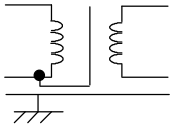
- **STANDARD TRANSFORMER - NO SHIELD**
  - NOTE CONNECTION FROM SECONDARY TO SAFETY GROUND TO ELIMINATE GROUND-TO-NEUTRAL VOLTAGE



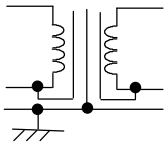
- **SINGLE FARADAY SHIELD**
  - CONNECT TO SAFETY GROUND FOR COMMON-MODE PROTECTION



- **SINGLE FARADAY SHIELD**
  - CONNECT TO NOISY-SIDE NEUTRAL WIRE FOR DIFFERENTIAL-MODE PROTECTION



- **TRIPLE FARADAY SHIELD**
  - CONNECT TO SAFETY GROUND FOR COMMON MODE
  - CONNECT TO NEUTRALS FOR DIFFERENTIAL MODE



ANALOG DEVICES

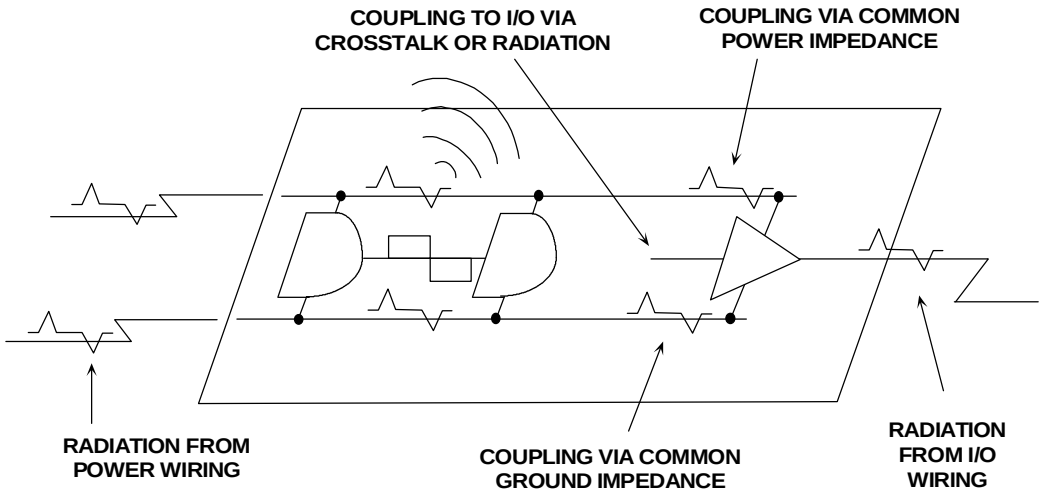
7.67

PRINTED CIRCUIT BOARD DESIGN FOR EMI PROTECTION

This section will summarize general points regarding the most critical portion of the design phase: the printed circuit board layout. It is at this stage where the performance of the system is most often compromised. This is not only true for signal-path performance, but also for the system's susceptibility to electromagnetic interference and the amount of electromagnetic energy radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

Figure 7.68 is a real-world printed circuit board layout which shows all the paths through which high-frequency noise can couple/radiate into/out of the circuit. Although the diagram shows digital circuitry, the same points are applicable to precision analog, high-speed analog, or mixed analog/digital circuits. Identifying critical circuits and paths helps in designing the PCB layout for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

METHODS BY WHICH HIGH FREQUENCY ENERGY COUPLES AND RADIATES INTO CIRCUITRY VIA PLACEMENT



ANALOG DEVICES

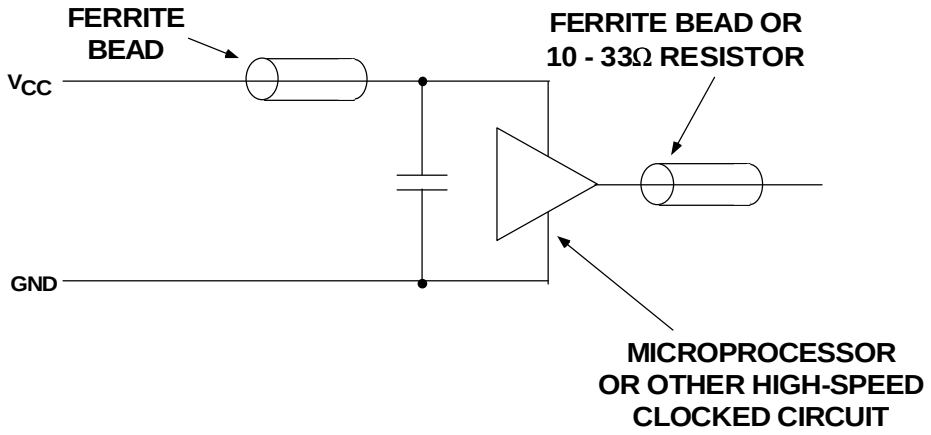
7.68

A key point in minimizing noise problems in a design is to *choose devices no faster than actually required by the application*. Many designers assume that faster is better: fast logic is better than slow, high bandwidth amplifiers are clearly better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed is not required by the system. Unfortunately, faster is not better, but worse where EMI is concerned.

Many fast DACs and ADCs have digital inputs and outputs with rise and fall times in the nanosecond region. Because of their wide bandwidth, the sampling clock and the digital inputs and can respond to any form of high frequency noise, even glitches as narrow as 1 to 3ns. These high speed data converters and amplifiers are easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. Adding a small ferrite bead just before the decoupling capacitor as shown in Figure 7.69 is very effective in filtering high frequency noise on the supply lines. For those circuits that require bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce the emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

POWER SUPPLY FILTERING AND SIGNAL LINE SNUBBING GREATLY REDUCES EMI EMISSIONS



ANALOG DEVICES

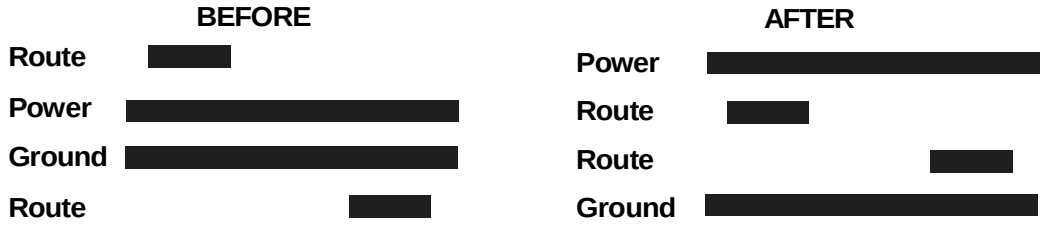
7.69

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution, and critical paths routed by hand.

Properly designed multilayer printed circuit boards can reduce EMI emissions and increase immunity to RF fields by a factor of 10 or more compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes nor analog and digital power planes.

The preferred multi-layer board arrangement is to embed the signal traces between the power and ground planes, as shown in Figure 7.70. These low-impedance planes form very high-frequency *stripline* transmission lines with the signal traces. The return current path for a high frequency signal on a trace is located directly above and below the trace on the ground/power planes. The high frequency signal is thus contained inside the PCB, thereby minimizing emissions. The embedded signal trace approach has an obvious disadvantage: debugging circuit traces that are hidden from plain view is difficult.

"TO EMBED OR NOT TO EMBED" THAT IS THE QUESTION



- **Advantages of Embedding**
  - Lower impedances, therefore lower emissions and crosstalk
    - Reduction in emissions and crosstalk is significant above 50MHz
  - Traces are protected
- **Disadvantages of Embedding**
  - Lower interboard capacitance, harder to decouple
  - Impedances may be too low for matching
  - Hard to prototype and troubleshoot buried traces

ANALOG DEVICES

7.70

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance and if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 7.71 for a number of logic families.

LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches / ns
Reprinted from EDN Magazine (January 20,1994), © CAHNERS PUBLISHING COMPANY 1995, A Division of Reed Publishing USA

DIGITAL IC FAMILY	t_r, t_f (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50

t_r = rise time of signal in ns
t_f = fall time of signal in ns

- **For analog signals @ f_{max}, calculate $t_r = t_f = 0.35 / f_{max}$**

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime, t_r, can be calculated using the equation $t_r = 0.35/f_{max}$. The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

Equation 7.4 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_O(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98d}{0.89w + t}\right] \quad \text{Eq. 7.4}$$

where ε_r = dielectric constant of printed circuit board material;
d = thickness of the board between metal layers, in mils;
w = width of metal trace, in mils; and
t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq. 7.5:

$$t_{pd}(ns/ft) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \quad \text{Eq. 7.5}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 (ε_r=4.7) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88Ω and 1.7ns/ft (7"/ns), respectively. Transmission lines can be effectively terminated in several ways depending on the application, as described in Section 2 of this book.

REFERENCES ON EMI/RFI

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4. Henry Ott, **Noise Reduction Techniques In Electronic Systems**, **Second Edition**, New York, John Wiley & Sons, 1988.

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7. B.Slattery and J.Wynne, *Design and Layout of a Video Graphics System for Reduced EMI*, **Analog Devices Application Note AN-333**.

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9. A. Rich, *Understanding Interference-Type Noise*, **Analog Dialogue**, 16-3, 1982, pp. 16-19.

10. A. Rich, *Shielding and Guarding*, **Analog Dialogue**, 17-1, 1983, pp. 8-13.

11. **EMC Test & Design**, Cardiff Publishing Company, Englewood, CO. An excellent, general purpose trade journal on issues of EMI and EMC.

SHIELDING CONCEPTS
Adolfo Garcia, John McDonald

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1,2, and 6 cited at the end of the section for more detailed information.

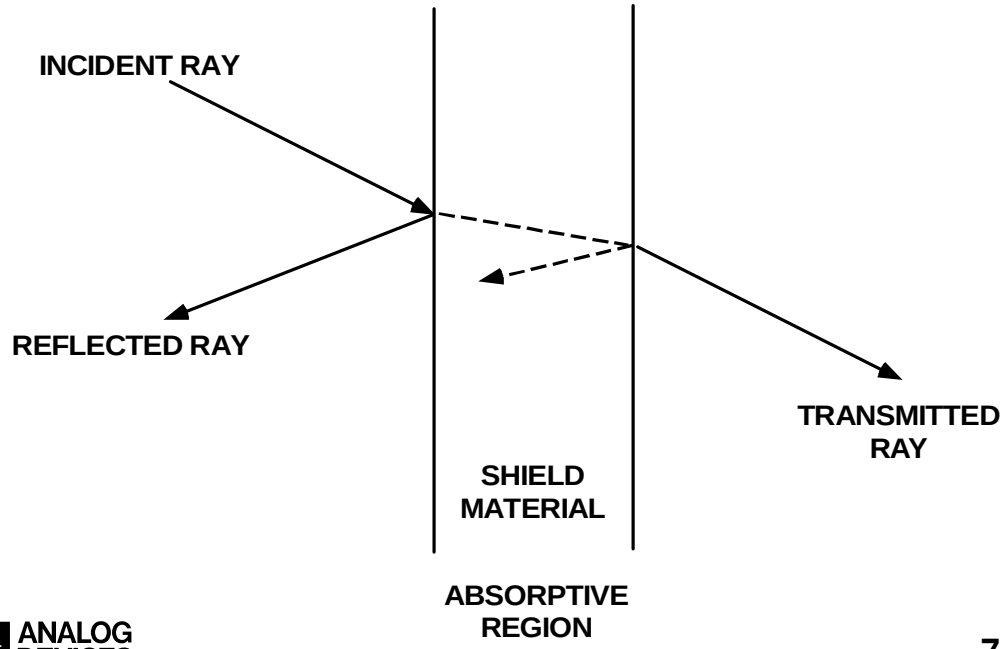
Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_0 = 377\Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377Ω. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. Both concepts are illustrated in Figure 7.72. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS



ANALOG DEVICES

7.72

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(\text{dB}) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \quad \text{Eq. 7.6}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;
μ_r = relative permeability of the shielding material, in Henries per meter;
f = frequency of the interference, and
r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(\text{dB}) = 14.6 + 10\log_{10}\left[\frac{f r^2 \sigma_r}{\mu_r}\right] \quad \text{Eq. 7.7}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(\text{dB}) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \quad \text{Eq. 7.8}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(\text{dB}) = 3.34\ t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 7.9}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_S, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Figure 7.73.

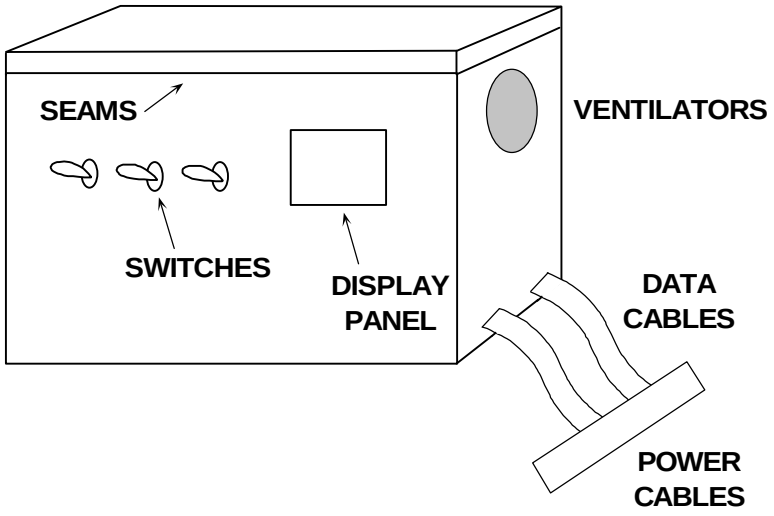
IMPEDANCE AND SKIN DEPTHS FOR VARIOUS SHIELDING MATERIALS

Material	Conductivity σ_r	Permeability μ_r	Shield Impedance $\lvert Z_S \rvert$	Skin Depth δ (inch)
Cu	1	1	$3.68E-7 \cdot \sqrt{f}$	$\frac{2.6}{\sqrt{f}}$
Al	1	0.61	$4.71E-7 \cdot \sqrt{f}$	$\frac{3.3}{\sqrt{f}}$
Steel	0.1	1,000	$3.68E-5 \cdot \sqrt{f}$	$\frac{0.26}{\sqrt{f}}$
μ Metal	0.03	20,000	$3E-4 \cdot \sqrt{f}$	$\frac{0.11}{\sqrt{f}}$

where $s_o = 5.82 \times 10^7$ S/m
$\mu_o = 4p \times 10^{-7}$ H/m
$e_o = 8.85 \times 10^{-12}$ F/m

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation (see Figure 7.74). Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

ANY OPENING IN AN ENCLOSURE CAN ACT AS AN EMI WAVEGUIDE BY COMPROMISING SHIELDING EFFECTIVENESS



The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 7.10 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness}\,(\text{dB}) = 20\log_{10}\left(\frac{\lambda}{2\cdot L}\right) \qquad \text{Eq. 7.10}$$

where λ = wavelength of the interference and
L = maximum dimension of the opening

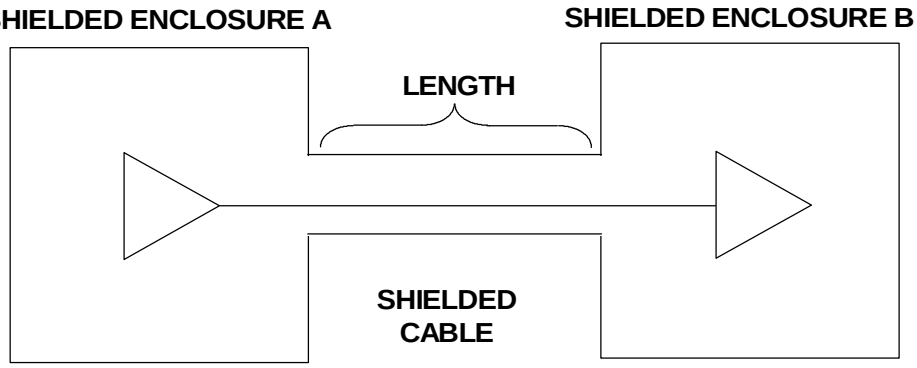
Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is

preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.

Sensors and Cable Shielding

The improper use of cables and their shields is a significant contributor to both radiated and conducted interference. As illustrated in Figure 7.75, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness.

LENGTH OF SHIELDED CABLES DETERMINES AN "ELECTRICALLY LONG" OR "ELECTRICALLY SHORT" APPLICATION



FULLY SHIELDED ENCLOSURES CONNECTED BY FULLY SHIELDED CABLE KEEP ALL INTERNAL CIRCUITS AND SIGNAL LINES INSIDE THE SHIELD.
- **TRANSITION REGION: 1/20 WAVELENGTH**

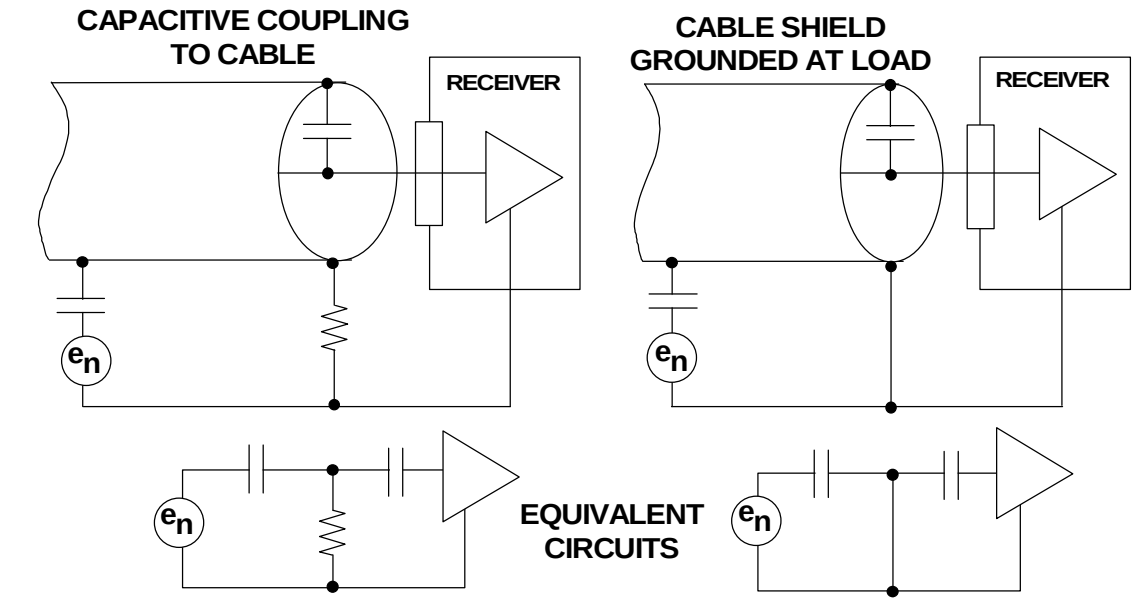
ANALOG DEVICES

7.75

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable. To protect circuits against low-frequency electric-field pickup, only one end of the shield should be returned to a

low-impedance point. A generalized example of this mechanism is illustrated in Figure 7.76.

CONNECT THE SHIELD AT ONE POINT AT THE LOAD TO PROTECT AGAINST LOW FREQUENCY (50/60Hz) THREATS



ANALOG DEVICES

7.76

In this example, the shield is grounded at the receiver. An exception to this approach (which will be highlighted again later) is the case where line-level (>1Vrms) audio signals are transmitted over long distances using twisted pair, shielded cables. In these applications, the shield again offers protection against low-frequency interference, and an accepted approach is to ground the shield at the driver end (LF and HF ground) and ground it at the receiver with a capacitor (HF ground only).

In those applications where the length of the cable is *electrically long*, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure. Low-frequency ground loops can be eliminated by replacing one of the DC shield connections to ground with a low inductance 0.01µF capacitor. This capacitor prevents low frequency ground loops and shunts high frequency interference to ground.

Shielded Twisted Pair Cable Grounding Examples

The environments in which analog systems operate are often rich in sources of EMI. Common EMI noise sources include power lines, logic signals, switching power supplies, radio stations, electric lighting, and motors. Noise from these sources can easily couple into long analog signal paths, such as cables, which act as efficient antennas. Shielded cables protect signal conductors from electric field (E-field) interference by providing low impedance paths to ground at the offending frequencies. Aluminum foil, copper, and braided stainless steel are materials very commonly used for cable shields due to their low impedance properties.

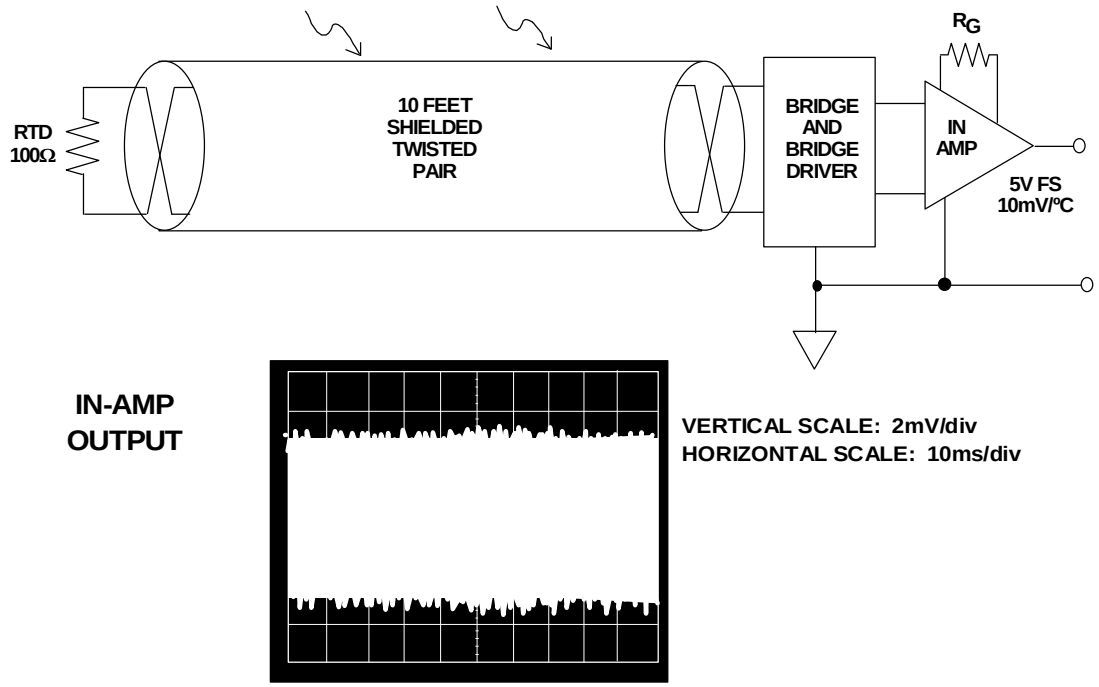
Simply increasing the separation between the noise source and the cable will yield significant additional attenuation due to reduced coupling, but shielding is still required in most applications involving remote sensors.

There are two paths from an EMI source to a susceptible cable: capacitive (or E-field) and magnetic (or H-field) coupling. Capacitive coupling occurs when parasitic capacitance exists between a noise source and the cable. The amount of parasitic capacitance is determined by the separation, shape, orientation, and the medium between the source and the cable.

Magnetic coupling occurs through parasitic mutual inductance when a magnetic field is coupled from one conductor to another. Parasitic mutual inductance depends on the shape and relative orientation of the circuits in question, the magnetic properties of the medium, and is directly proportional to conductor loop area. Minimizing conductor loop area reduces magnetic coupling proportionally.

Shielded *twisted pair* cables offer further noise immunity to magnetic fields. Twisting the conductors together reduces the net loop area, which has the effect of canceling any magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero.

To study the shielding problem, a precision *RTD (Resistance Temperature Detector)* amplifier circuit was used as the basis for a series of experiments. A remote 100Ω RTD was connected to the bridge, bridge driver, and the bridge amplifier circuit (Figure 7.77) using 10 feet of a shielded twisted pair cable. The RTD is one element of a 4-element bridge (the three other resistor elements are located in the bridge and bridge driver circuit). The gain of the instrumentation amplifier was adjusted so that the sensitivity at the output was 10mV/°C, with a 5V full scale. Measurements were made at the output of the instrumentation amplifier with the shield grounded in various ways. The experiments were conducted in lab standard environment where a considerable amount of electronic equipment was in operation.



ANALOG DEVICES

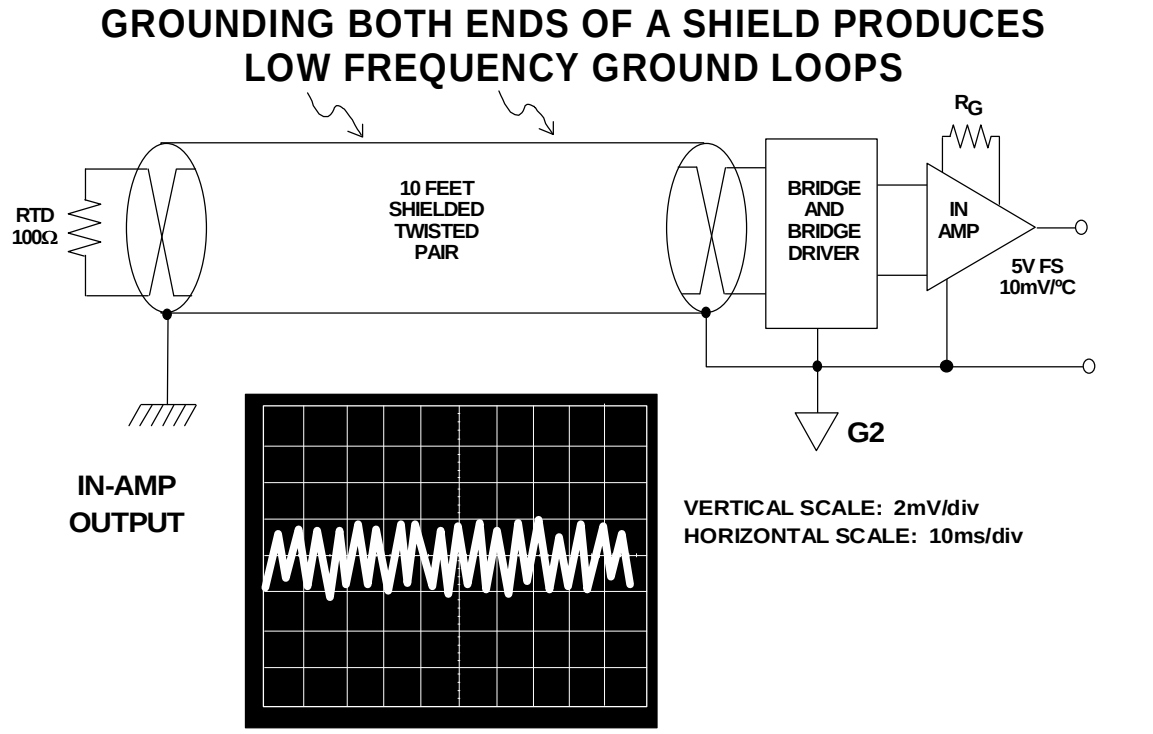
7.77

The first experiment was conducted with the shield ungrounded. As shown in Figure 7.77, shields left floating are not useful and offer no attenuation to EMI-induced noise, in fact, they act as antennas. Capacitive coupling is unaffected, because the floating shield provides a coupling path to the signal conductors. Most cables exhibit parasitic capacitances between 10-30pF/ft. Likewise, HF magnetically coupled noise is not attenuated because the floating cable shield does not alter either the geometry or the magnetic properties of the cable conductors. LF magnetic noise is not attenuated significantly, because most shield materials absorb very little magnetic energy.

To implement effective EMI/RFI shielding, the shield must be grounded. A grounded shield reduces the value of the impedance of the shield to ground to small values. Implementing this change will reduce the amplitude of the E-Field noise substantially.

Designers often ground both ends of a shield in an attempt to reduce shield impedance and gain further E-Field attenuation. Unfortunately, this approach can create a new set of potential problems. The AC and DC ground potentials are generally different at each end of the shield. Low-frequency ground loop current is created when both ends of a shield are grounded. This low frequency current flows through the large loop area of the shield and couples into the center conductors through the parasitic mutual inductance. If the twisted pairs are precisely balanced, the induced voltage will appear as a common-mode rather than a differential voltage. Unfortunately, the conductors may not be perfectly balanced, the sensor and excitation circuit may not be fully balanced, and the common mode rejection at the receiver may not be sufficient. There will therefore be some differential noise voltage developed between the conductors at the output end, which is amplified and

appears at the final output of the instrumentation amplifier. With the shields of the experimental circuit grounded at both ends, the results are shown in Figure 7.78.

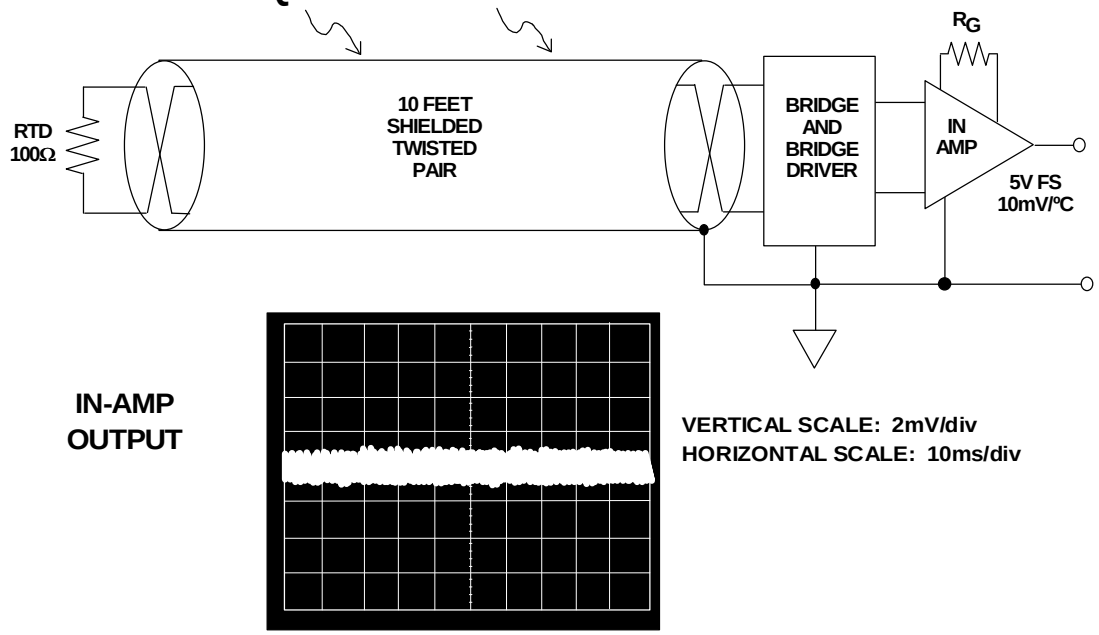


ANALOG DEVICES

7.78

Figure 7.79 illustrates a properly grounded system with good electric field shielding. Notice that the ground loop has been eliminated. The shield has a single point ground, located at the signal conditioning circuitry, and noise coupled into the shield is effectively shunted into the receiver ground and does not appear at the output of the instrumentation amplifier.

GROUNDING SHIELD AT RECEIVER END SHUNTS LOW- AND HIGH-FREQUENCY NOISE INTO RECEIVER GROUND



IN-AMP OUTPUT

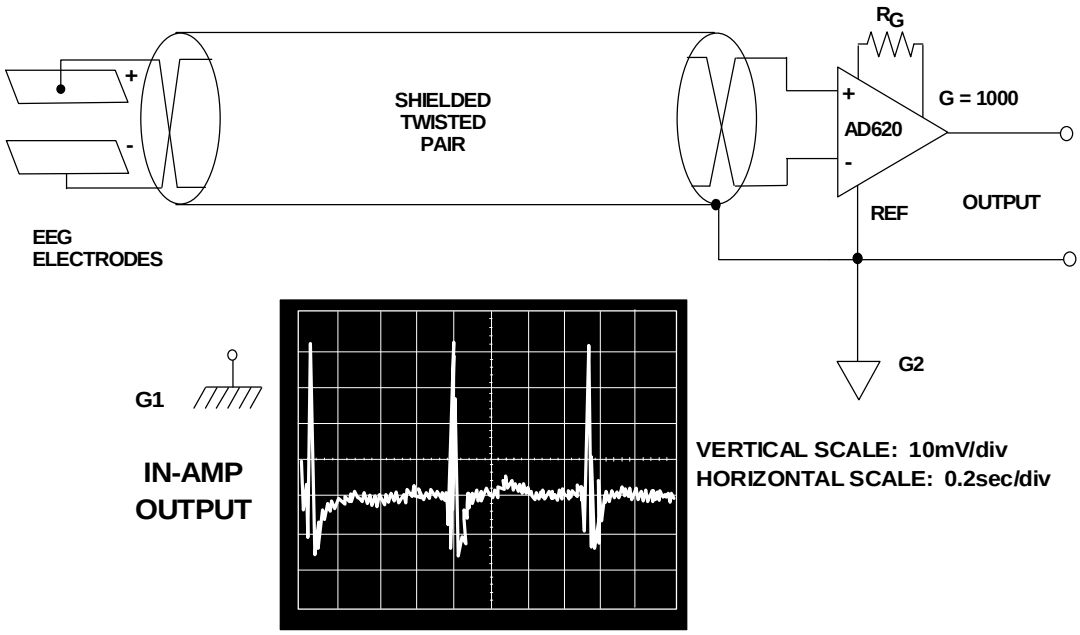
VERTICAL SCALE: 2mV/div
HORIZONTAL SCALE: 10ms/div

ANALOG DEVICES

7.79

Figure 7.80 shows an example of a remotely located, ungrounded, passive sensor (ECG electrodes) which is connected to a high-gain, low power AD620 instrumentation amplifier through a shielded twisted pair cable. Note that the shield is properly grounded at the signal conditioning circuitry. The AD620 gain is 1000× , and the amplifier is operated on ±3V supplies. Notice the absence of 60Hz interference in the amplifier output.

FOR UNGROUNDED PASSIVE SENSORS, GROUND SHIELD AT THE RECEIVING END



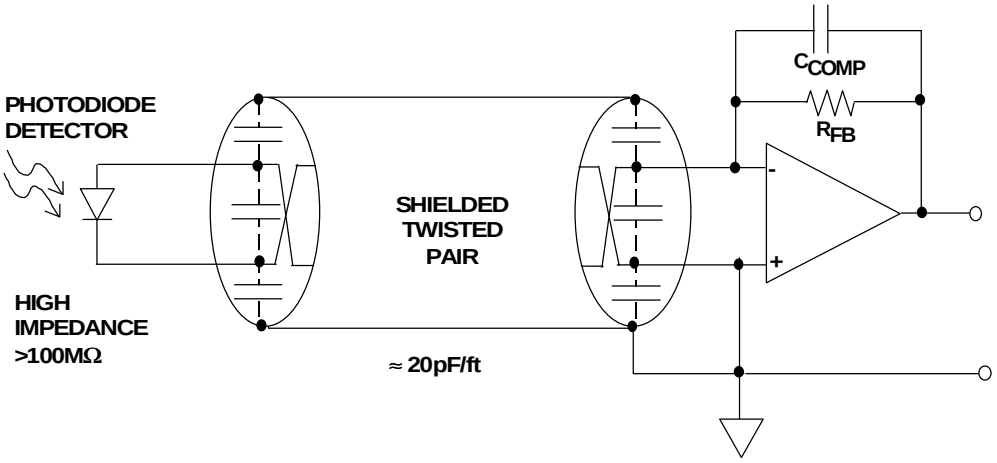
ANALOG DEVICES

7.80

Most high impedance sensors generate low-level current or voltage outputs, such as a photodiode responding to incident light. These low-level signals are especially susceptible to EMI, and often are of the same order of magnitude as the parasitic parameters of the cable and input amplifier.

Even properly shielded cables can degrade the signals by introducing parasitic capacitance that limits bandwidth, and leakage currents that limit sensitivity. An example is shown in Figure 7.81, where a high-impedance photodiode is connected to a preamp through a long shielded twisted pair cable. Not only will the cable capacitance limit bandwidth, but cable leakage current limits sensitivity. A pre-amplifier, located close to the high-impedance sensor, is recommended to amplify the signal and to minimize the effect of cable parasitics.

SHIELDS ARE NOT EFFECTIVE WITH HIGH IMPEDANCE REMOTE SENSORS



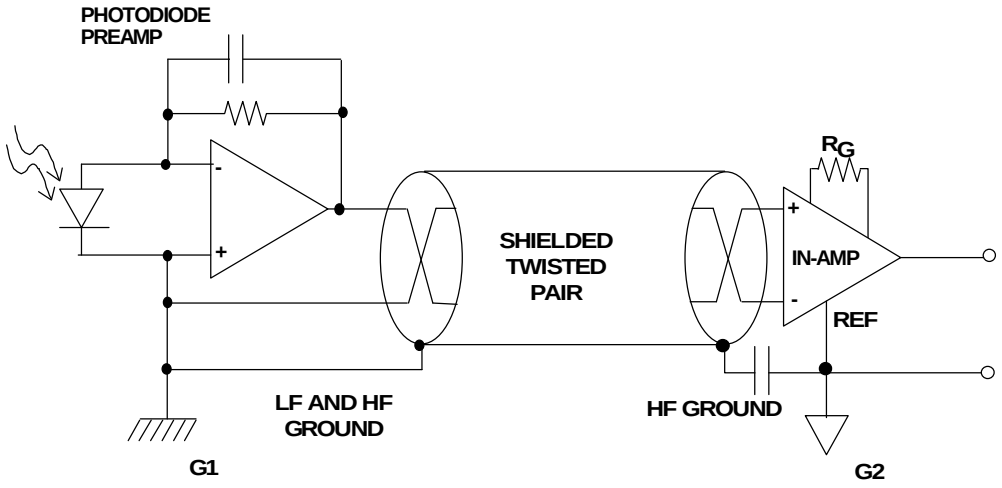
- CABLE CAPACITANCE LIMITS BANDWIDTH
- CABLE LEAKAGE CURRENT LIMITS SENSITIVITY

ANALOG DEVICES

7.81

Figure 7.82 is an example of a high-impedance photodiode detector and pre-amplifier, driving a shielded twisted pair cable. Both the amplifier and the shield are grounded at a remote location. The shield is connected to the cable driver common, G1, ensuring that the signal and the shield at the driving end are both referenced to the same point. The capacitor on the receiving side of the cable shunts high frequency noise on the shield into ground G2 without introducing a low-frequency ground loop. This popular grounding scheme is known as *hybrid* grounding.

REMOTELY LOCATED HIGH IMPEDANCE SENSOR WITH PREAMP

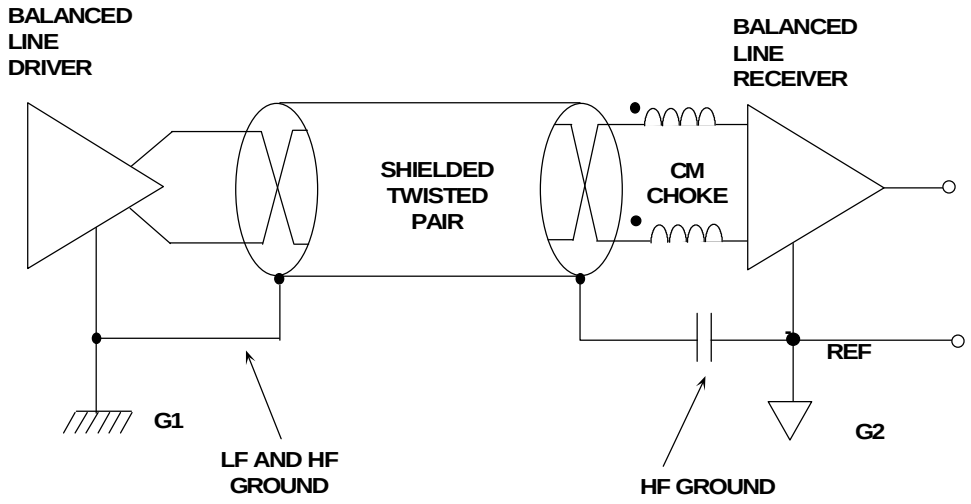


ANALOG DEVICES

7.82

Figure 7.83 illustrates a balanced active line driver with a hybrid shield ground implementation. When a system's operation calls for a wide frequency range, the hybrid grounding technique often provides the best choice (Reference 8). The capacitor at the receiving end shunts high-frequency noise on the shield into G2 without introducing a low-frequency ground loop. At the receiver, a common-mode choke can be used to help prevent RF pickup entering the receiver, and subsequent RFI rectification (see References 9 and 10). Care should be taken that the shields are grounded to the chassis entry points to prevent contamination of the signal ground (Reference 11).

HYBRID (LF AND HF) GROUNDING WITH ACTIVE DRIVER



ANALOG DEVICES

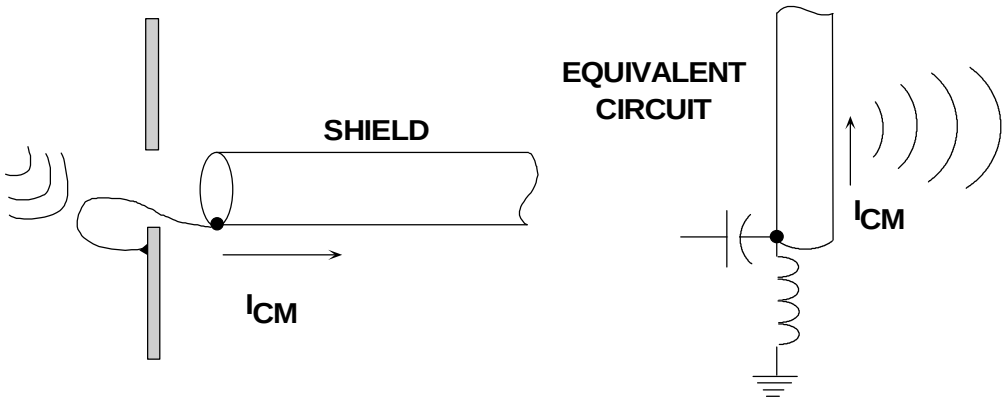
7.83

To summarize this discussion, shield grounding techniques must take into account the type and the configuration of the sensor as well as the nature of the interference. When a low-impedance passive sensor is used, grounding the shield to the receiving end is the best choice. Active sensor shields should generally be grounded at the source (direct connection to source ground) and at the receiver (connect to receiver ground using a capacitor). This hybrid approach minimizes high-frequency interference and prevents low-frequency ground loops. Shielded twisted conductors offer additional protection against shield noise because the coupled noise occurs as a common-mode, and not a differential signal.

The best shield can be compromised by poor connection techniques. Shields often use “pig-tail” connections to make the connection to ground. A “pig-tail” connection is a single wire connection from shield to either chassis or circuit ground. This type of connection is inexpensive, but at high frequency, it does not provide low impedance. Quality shields do not leave large gaps in the cable/instrument shielding system. Shield gaps provide paths for high frequency EMI to enter the system. The cable shielding system should include the cable end connectors. Ideally, cable shield connectors should make 360° contact with the chassis ground.

As shown in Figure 7.84, pigtail terminations on cables very often cause systems to fail radiated emissions tests because high-frequency noise has coupled into the cable shield, generally through stray capacitance. If the length of the cable is considered *electrically long* at the interference frequency, then it can behave as a very efficient quarter-wave antenna. The cable pigtail forms a matching network, as shown in the figure, to radiate the noise which coupled into the shield. In general, pigtails are only recommended for applications below 10kHz, such as 50/60Hz interference protection. For applications where the interference is greater than 10kHz, shielded connectors, electrically and physically connected to the chassis, should be used.

"SHIELDED" CABLE CAN CARRY HIGH FREQUENCY CURRENT AND BEHAVES AS AN ANTENNA



I_{CM} = COMMON-MODE CURRENT

ANALOG DEVICES

7.84

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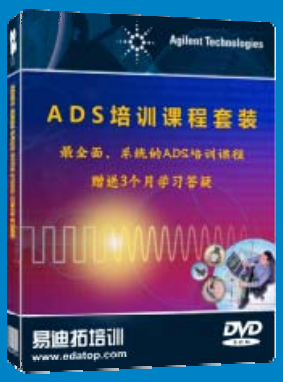

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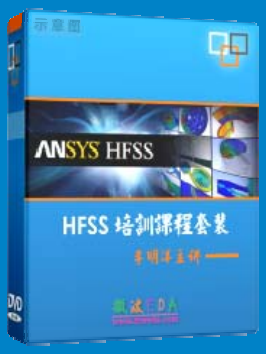

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套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

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