I²S bus specification

1.0 INTRODUCTION

Many digital audio systems are being introduced into the consumer audio market, including compact disc, digital audio tape, digital sound processors, and digital TV-sound. The digital audio signals in these systems are being processed by a number of (V)LSI ICs, such as:

- A/D and D/A converters;
- digital signal processors;
- error correction for compact disc and digital recording;
- digital filters;
- digital input/output interfaces.

Standardized communication structures are vital for both the equipment and the IC manufacturer, because they increase system flexibility. To this end, we have developed the inter-IC sound (I²S) bus – a serial link especially for digital audio.

2.0 BASIC SERIAL BUS REQUIREMENTS

The bus has only to handle audio data, while the other signals, such as sub-coding and control, are transferred separately. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used consisting of a line for two time-multiplexed data channels, a word select line and a clock line.

Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock, word-select signal and data. In complex systems however, there may be several transmitters and receivers, which makes it difficult to define the master. In such systems, there is usually a system master controlling digital audio data-flow between the various ICs. Transmitters then, have to generate data under the control of an external clock, and so act as a slave. Figure 1 illustrates some simple system configurations and the basic interface timing. Note that the system master can be combined with a transmitter or receiver, and it may be enabled or disabled under software control or by pin programming.
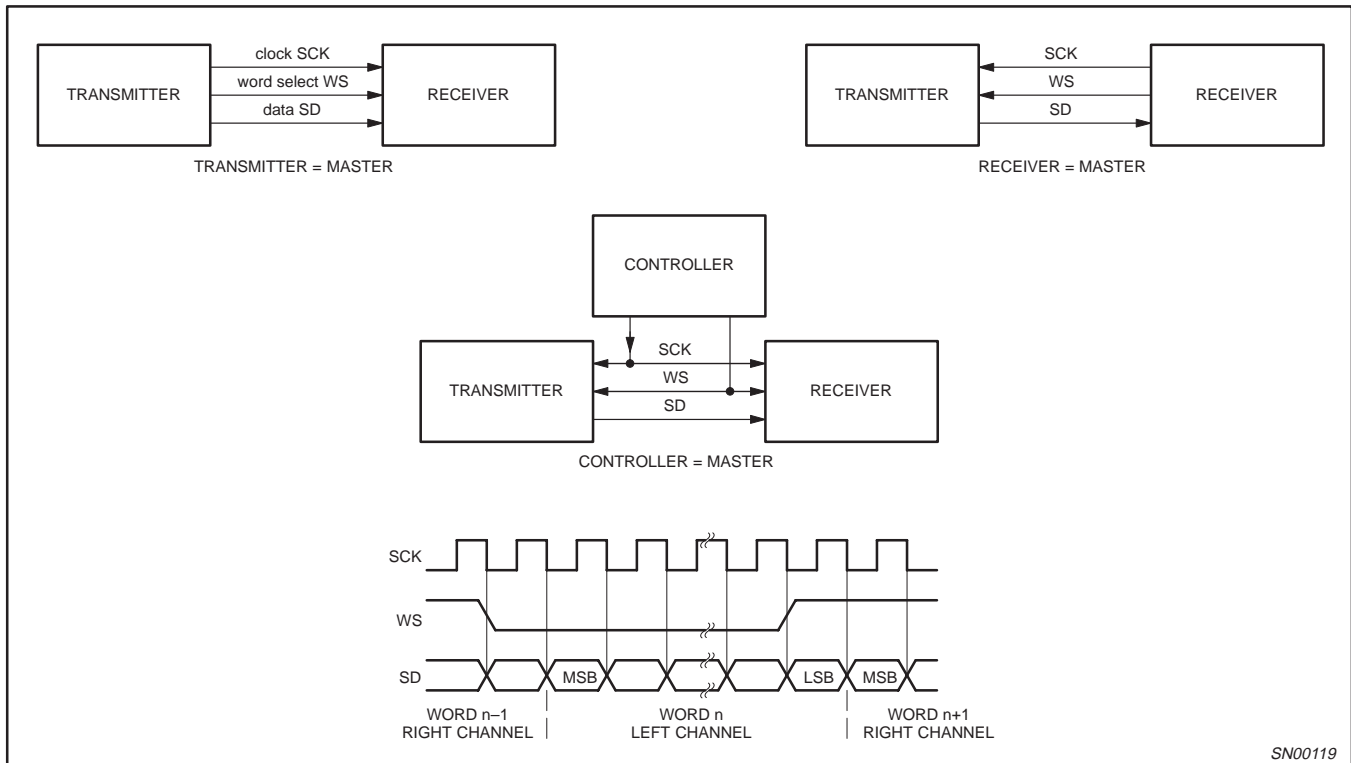

Figure 1. Simple System Configurations and Basic Interface Timing

I²S bus specification

3.0 THE I²S BUS

As shown in Figure 1, the bus has three lines:

- continuous serial clock (SCK);
- word select (WS);
- serial data (SD);

and the device generating SCK and WS is the master.

3.1 Serial Data

Serial data is transmitted in two's complement with the MSB first. The MSB is transmitted first because the transmitter and receiver may have different word lengths. It isn't necessary for the transmitter to know how many bits the receiver can handle, nor does the receiver need to know how many bits are being transmitted.

When the system word length is greater than the transmitter word length, the word is truncated (least significant data bits are set to '0') for data transmission. If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally. And so, the MSB has a fixed position, whereas the position of the LSB depends on the word length. The transmitter always sends the MSB of the next word one clock period after the WS changes.

Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge (see Figure 2 and Table 1).

3.2 Word Select

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left);
- WS = 1; channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word (see Figure 1).

4.0 TIMING

In the I²S format, any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input. This means, taking into account the propagation delays between master clock and the data and/or word-select signals, that the total delay is simply the sum of:

- the delay between the external (master) clock and the slave's internal clock; and
- the delay between the internal clock and the data and/or word-select signals.

For data and word-select inputs, the external to internal clock delay is of no consequence because it only lengthens the effective set-up time (see Figure 2). The major part of the time margin is to accommodate the difference between the propagation delay of the transmitter, and the time required to set up the receiver.

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device. This means that higher data rates can be used in the future.
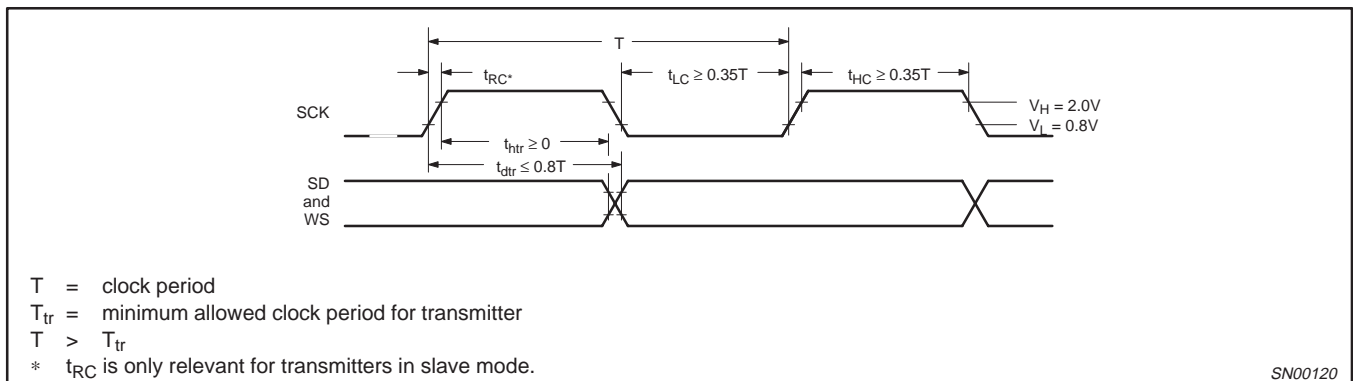

T = clock period
T_{tr} = minimum allowed clock period for transmitter
$T > T_{tr}$
∗ t_{RC} is only relevant for transmitters in slave mode.

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Figure 2. Timing for I²S Transmitter

I^{2}S bus specification

T = clock period
T$_r$ = minimum allowed clock period for transmitter
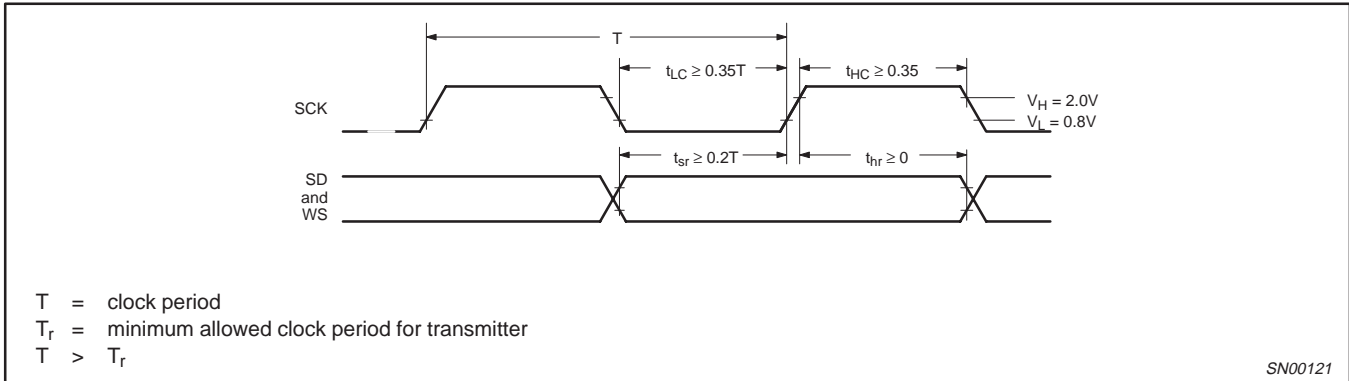T > T$_r$

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Figure 3. Timing for I^{2}S Receiver

Note that the times given in both Figures 2 and 3 are defined by the transmitter speed. The specification of the receiver has to be able to match the performance of the transmitter

Example: Master transmitter with data rate of 2.5MHz ($\pm$10%) (all values in ns)

	MIN	TYP	MAX	CONDITION
clock period T	360	400	440	T$_{tr}$ = 360
clock HIGH t$_{HC}$	160			min > 0.35T = 140 (at typical data rate)
clock LOW t$_{LC}$	160			min > 0.35T = 140 (at typical data rate)
delay t$_{dtr}$			300	max < 0.80T = 320 (at typical data rate)
hold time t$_{htr}$	100			min > 0
clock rise-time t$_{RC}$			60	max > 0.15T$_{tr}$ = 54 (only relevant in slave mode)

Example: Slave receiver with data rate of 2.5MHz ($\pm$10%) (all values in ns)

	MIN	TYP	MAX	CONDITION
clock period T	360	400	440	T$_{tr}$ = 360
clock HIGH t$_{HC}$	110			min < 0.35T = 126
clock LOW t$_{LC}$	110			min < 0.35T = 126
set-up time t$_{sr}$	60			min < 0.20T = 72
hold time t$_{htr}$	0			min < 0

I^{2}S bus specification

Table 1. Timing for I^{2}S transmitters and receivers

| | TRANSMITTER | | | | RECEIVER | | | | |
| | LOWER LIMIT | | UPPER LIMIT | | LOWER LIMIT | | UPPER LIMIT | | |
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	NOTES
Clock period T	T_{tr}				T_r				1
MASTER MODE: clock generated by transmitter or receiver:									
HIGH t_{HC}	$0.35T_{tr}$				$0.35T_{tr}$				2a
LOW t_{LC}	$0.35T_{tr}$				$0.35T_{tr}$				2a
SLAVE MODE: clock accepted by transmitter or receiver:									
HIGH t_{HC}		$0.35T_{tr}$				$0.35T_r$			2b
LOW t_{LC}		$0.35T_{tr}$				$0.35T_r$			2b
rise-time t_{RC}			$0.15T_{tr}$						3
TRANSMITTER:									
delay t_{dtr}				0.8T					4
hold time t_{htr}	0								3
RECEIVER:									
set-up time t_{sr}						$0.2T_r$			5
hold time t_{hr}						0			5

All timing values are specified with respect to high and low threshold levels.

NOTES:

1. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
2a. At all data rates in the master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason t_{HC} and t_{LC} are specified with respect to T.
2b. In the slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used (see Figure 3).
3. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
4. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient set-up time.
5. The data set-up and hold time must not be less than the specified receiver set-up and hold time.
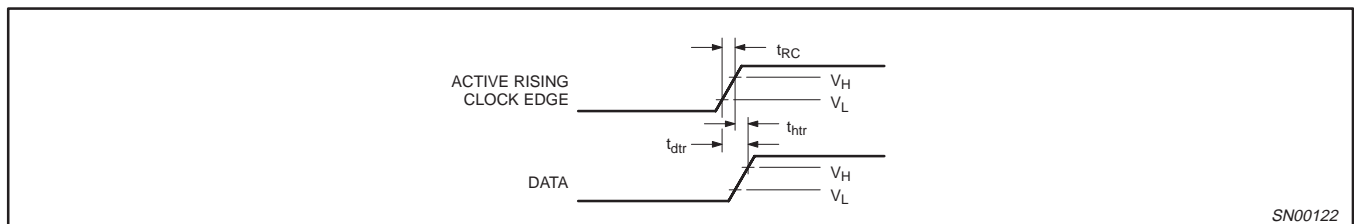

Figure 4. Clock rise-time definition with respect to the voltage levels

I²S bus specification

5.0 VOLTAGE LEVEL SPECIFICATION

5.1 Output Levels
V_L < 0.4V
V_H > 2.4V both levels able to drive one standard TTL input (I_{IL} = –1.6mA and
I_{IH} = 0.04mA).

5.2 Input Levels
V_{IL} = 0.8V
V_{IH} = 2.0V

Note: At present, TTL is considered a standard for logic levels. As other IC (LSI) technologies become popular, other levels will also be supported.

6.0 POSSIBLE HARDWARE CONFIGURATIONS

6.1 Transmitter (see Figure 5)
At each WS-level change, a pulse WSP is derived for synchronously parallel-loading the shift register. The output of one of the data latches is then enabled depending on the WS signal. Since the serial data input is zero, all the bits after the LSB will also be zero.

6.2 Receiver (see Figure 6)
Following the first WS-level change, WSP will reset the counter on the falling edge of SCK. After decoding the counter value in a "1 out of n" decoder, the MSB latch (B1) is enabled (EN1 = 1), and the first serial data bit (the MSB) is latched into B1 on the rising edge of SCK. As the counter increases by one every clock pulse, subsequent data bits are latched into B2 to Bn.

On the next WS-level change, the contents of the n latches are written in parallel, depending on WSD, into either the left or the right data-word latch. After this, latches B2 to Bn are cleared and the counter reset. If there are more than n serial data bits to be latched, the counter is inhibited after Bn (the receiver's LSB) is filled and subsequent bits are ignored.

Note: The counter and decoder can be replaced by an n-bit shift-register (see Figure 7) in which a single '1' is loaded into the MSB position when WSP occurs. On every subsequent clock pulse, this '1' shifts one place, enabling the N latches. This configuration may prove useful if the layout has to be taken into account.
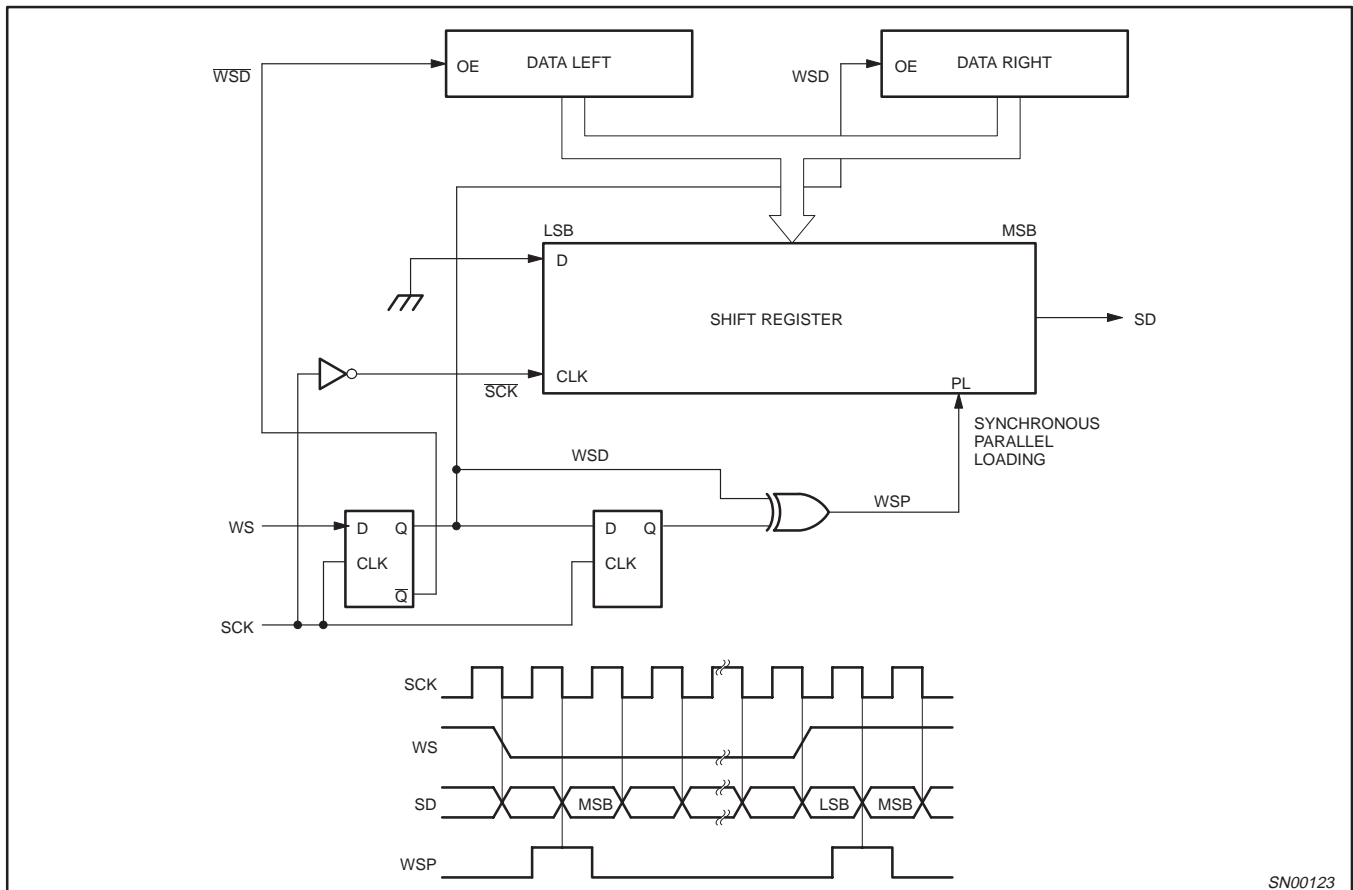

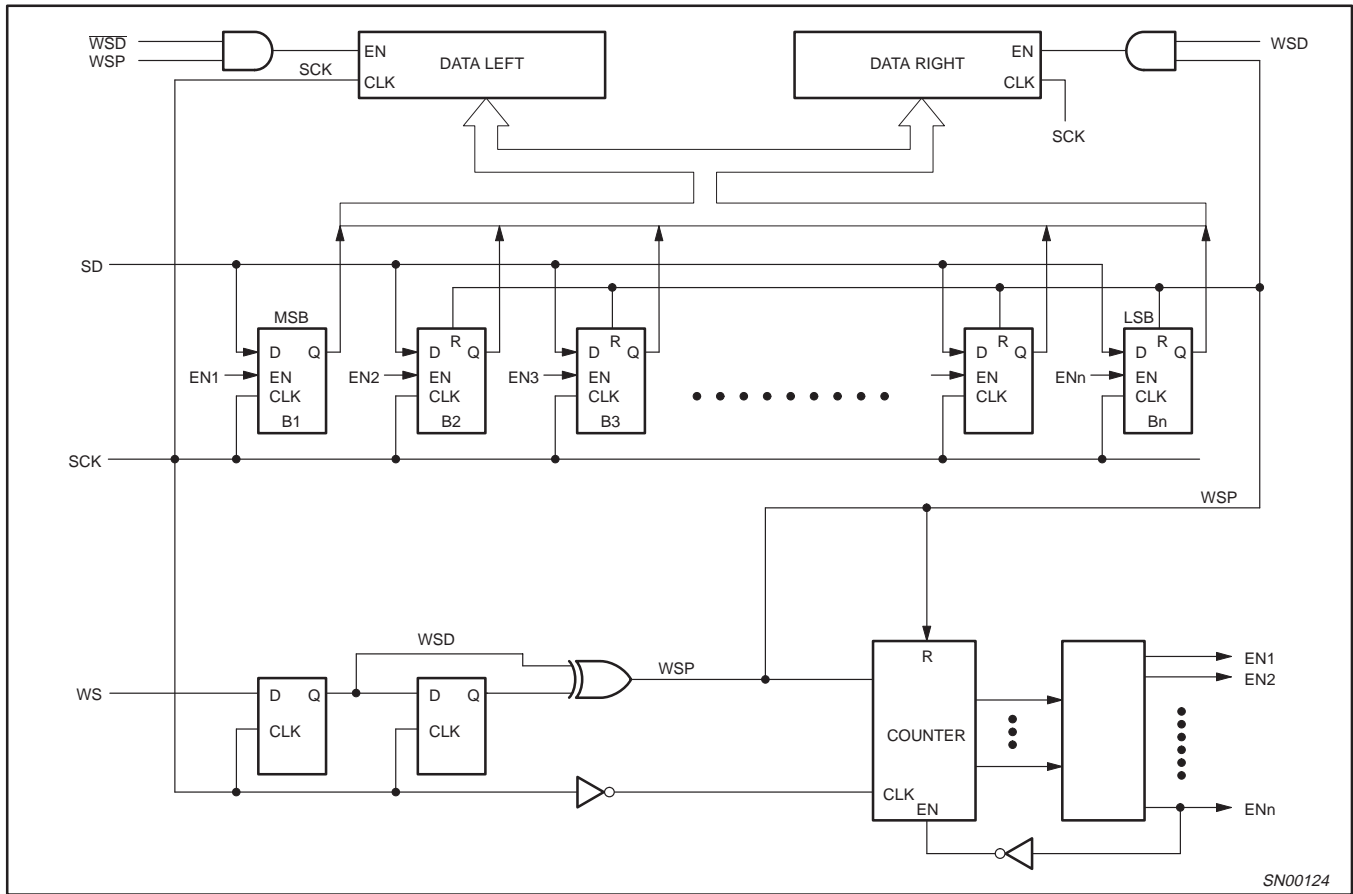Figure 5. Possible transmitter configuration

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**Figure 6. Possible receiver configuration. The latches and the counter use synchronous set,
reset and enable inputs, where set overrules the reset input, and reset overrules the enable input.**
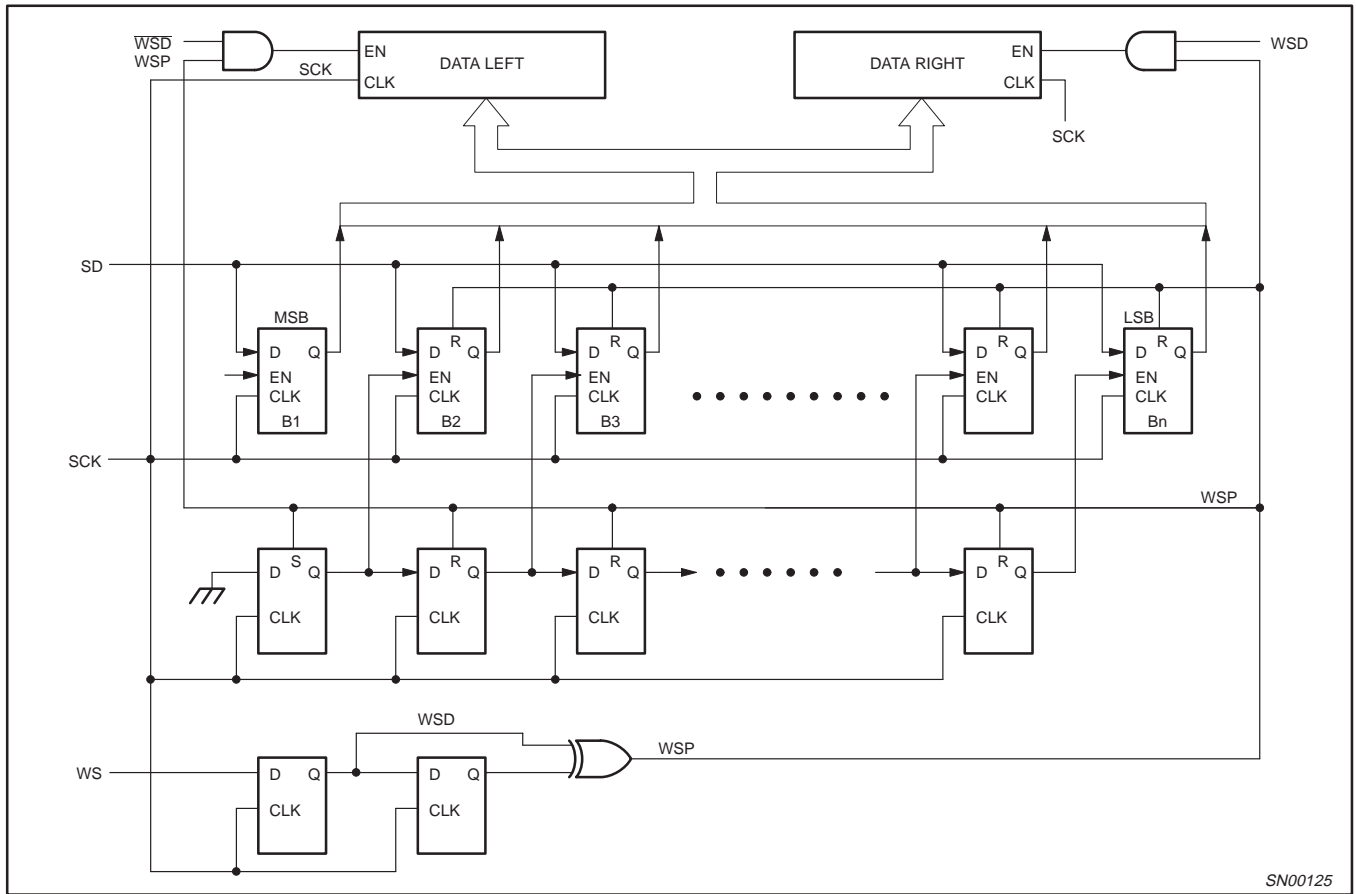
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Figure 7. Possible receiver configuration, using an n-bit shift-register to enable control of data input register.

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