# VC0568-V33

**Mobile Phone Video Processor**

**Datasheet**

**Version 1.2a**

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# 1. Overview

VC0568 is a mega-pixel camera controller chip for mobile application. It enables camera phone to capture and display still image and video clip at real-time on mobile phone screen. By using VC0568, the burden on mobile phone host CPU to process image and graphics can be reduced dramatically.

With direct interface to CMOS/CCD image sensor and LCD display module, VC0568 can provide high-quality, low-latency video stream to most popular LCD panels with desired resolution and color depth. VC0568's image pipeline integrates Image Signal Processing unit, Image Post Processing unit, JPEG codec as well as JPEG buffer allocated from the on-chip 384KB SRAM for storing 1.3M-resolution JPEG images. A powerful yet flexible image sizer embedded in VC0568 further allows mobile phone users to perform up to 16x digital zoom and pan function in viewfinder, capture and display mode. The on-chip JPEG codec may also be employed by host CPU for various encoding/decoding tasks.

Within its display sub-module, VC0568 provides Graphics RAM which allocated from the on-chip 384KB SRAM for host CPU to write to LCD panel directly. VC0568 supports overlay and alpha-blending functions between video stream and the graphics from host CPU, along with an integrated graphics engine delivering graphics acceleration for clipping, line drawing, BitBLT, etc. VC0568 also provides a direct path from host CPU to LCD panel.

VC0568 comes with 100-pin fpBGA package at 7mm x 7mm footprint.

VC0568 has the following applications

- Mobile Phones
- Personal Digital Assistants
- Wireless Communicators
- Video Phones

## 2. Feature

- **System Architecture**
  - Provide a transparent, flexible physical bridge between mobile phone baseband processor, image sensor and LCD panel
  - With camera function off, host CPU can refresh LCD directly
  - To add camera function, mobile phone design only need minimal change with the help of VC0568 and a API set provided by Vimicro

- **Low Power Design**
  - Power Consumption is optimized from Architecture to Circuit Design
  - 100uA in sleep mode
  - 20mA in preview mode in 160x120 @ 30fps
  - 1.8V for core
  - 2.5, 2.85, 3.0, 3.3 V for I/O

- **Small Form Factor**
  - 7 mm x 7 mm

- **Host Interface**
  - Support ARM, 80-type and 68-type bus
  - In-direct addressing mode:
    - 1-bit address bus and 16-bit data bus
    - 1-bit address bus and 8-bit data bus

- **Sensor Interface**
  - Support off-shelf CIF/VGA CMOS and CCD sensors
  - Support off-shelf 1.3Mega pixel CMOS and CCD sensors
  - 8 bit RGB Bayer or 8 bit YUV input
  - Strobe flash timing control

- **Image Signal Processing**
  - Real-time dead-pixel detection and compensation
  - Auto exposure
  - Auto white balance
  - Auto gain control
  - Auto focus control
  - Programmable AE/AWB windows
  - Auto flicker detection and cancellation
  - Edge-adaptive CFA interpolation (5x5 matrix)
  - Configurable gamma correction
  - Configurable color correction
  - Configurable white balancing
  - Configurable brightness, color saturation and hue

- Back light compensation
- Configurable image noise reduction
- Configurable image sharpness control

- **JPEG codec**
  - Standard baseline JPEG codec with dynamic bit-rate control
  - Encoding: 4:2:2, 4:1:1, 4:2:0
  - Decoding: 4:4:4, 4:2:2, 4:1:1, 4:2:0

- **Image sizer and digital zoom**
  - Programmable image sub-sampling with anti-aliasing filtering
  - Programmable image dithering
  - Up to 16x digital zoom during preview, capture, postview
    - Up to 2x for SXGA
    - Up to 4x for VGA
    - Up to 8x for SIF
    - Up to 16x for QSIF

- **Programmable image resolution and data format**
  - Programmable output image resolution including standard resolutions:
    - 1280 x 960
    - 1024 x 768
    - 800 x 600
    - 640 x 480
    - 320 x 240
    - 160 x 120
    - Thumbnail (40x30)
  - Multiple output image formats
    - JPEG
    - RGB: 888, 666, 565, 444
    - Gray

- **LCD Controller Interface**
  - Support dual LCD panels
  - Support TFT or STN LCD panels
  - Supports LCD with following bit-depth: 8/12/16/18/24
  - Supports LCD with following size: 160 x 120 ~ 320 x 240
  - Support Picture-in-Picture function
  - Separate controls for layer A and layer B
  - Support Backlight white LED control via GPIO
  - Support Illumination LED control via GPIO

- **2-D Hardware Acceleration Engine**
  - Enhanced BitBLT

- ROPs
- All-angle (Bresenham) line drawing
- Clip

- **Video Post-processing**
  - Overlay between video and host graphics
  - Alpha-blending between video and host graphics
  - Image rotation (90, 180 and 270 degree)
  - Mirror (horizontal and vertical)
  - Special image effects:
    - Monochrome
    - Sepia
    - Special color
    - Negative
    - Relief
    - Sketch

# 3.Pin Layout

## 3.1 VC0568 Pin-out Diagram

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | CONF[2] | LCD_DATA[0] | OVDD8 | RSTN | CS_CLK | CS_VSYNC | LCD_RDN | LCD_DATA[14] | LCD_DATA[12] | OVDD7 | CPU_ADDR[5] | CPU_A8 |
| B | LCD_DATA[1] | OVSS8 | CONF[1] | INT | CS_RSTN | DVSS4 | DVDD4 | LCD_DATA[13] | CPU_ADDR[7] | CPU_ADDR[6] | CPU_ADDR[4] | CPU_RS |
| C | CPU_DATA[1] | CPU_DATA[0] | | | | | | | | | CS_ENB | OVDD6 |
| D | OVDD1 | CPU_DATA[2] | | CONF[0] | CS_HSYNC | LCD_WRN | LCD_DATA[15] | OVSS7 | OVSS6 | | LCD_RS | CS_PWDN |
| E | LCD_DATA[2] | CPU_DATA[3] | | OVSS1 | | | | | LCD_RST | | CS_SCK | CS_SDA |
| F | GPIO[1] | GPIO[0] | | LCD_DATA[3] | | | | | DVSS3 | | DVDD3 | XCLK |
| G | CPU_WBEN[0] | DVDD1 | | DVSS1 | | | | | LCD_DATA[11] | | VDDA | VSSA |
| H | CPU_WEN | CPU_OEN | | CPU_WBEN[1] | | | | | OVSS5 | | LCD_DATA[9] | LCD_DATA[10] |
| J | CS_DATA[6] | CS_DATA[7] | | CS_DATA[5] | OVSS3 | LCD_DATA[7] | GPIO[4] | LCD_CS1N | OVSS4 | | LCD_DATA[8] | OVDD5 |
| K | OVDD2 | CS_DATA[4] | | | | | | | | | CPU_ADDR[2] | CPU_ADDR[3] |
| L | LCD_DATA[4] | OVSS2 | CPU_DATA[4] | CPU_DATA[6] | CPU_DATA[7] | DVDD2 | GPIO[2] | CPU_CS1N | CPU_CS2N | CS_DATA[2] | CPU_ADDR[0] | CPU_ADDR[1] |
| M | TEST | LCD_DATA[5] | CPU_DATA[5] | OVDD3 | LCD_DATA[6] | DVSS2 | GPIO[3] | LCD_CS2N | OVDD4 | CS_DATA[3] | CS_DATA[1] | CS_DATA[0] |



Figure 3-1 VC0568 fpBGA-100 Pin-out Diagram – Top View

### 3.2 Pin description

| Pin Name | I/O TYPE | Ball Pad | Remark |
|---|---|---|---|
| LCD_DATA[0] | B | A2 | Data bus to the LCD panel, bit [0] |
| LCD_DATA[1] | B | B1 | Data bus to the LCD panel, bit [1] |
| CPU_DATA[0] | B | C2 | Data bus between host CPU and VC0568, bit [0] |
| CPU_DATA[1] | B | C1 | Data bus between host CPU and VC0568, bit [1] |
| OVSS1 | G | E4 | IO ground |
| OVDD1 | P | D1 | IO power |
| CPU_DATA[2] | B | D2 | Data bus between host CPU and VC0568, bit [2] |
| CPU_DATA[3] | B | E2 | Data bus between host CPU and VC0568, bit [3] |
| LCD_DATA[2] | B | E1 | Data bus to the LCD panel, bit [2] |
| LCD_DATA[3] | B | F4 | Data bus to the LCD panel, bit [3] |
| GPIO[0] | B, PU | F2 | Global purpose IO pin, bit [0] |
| GPIO[1] | B, PU | F1 | Global purpose IO pin, bit [1] |
| DVSS1 | G | G4 | Core ground |
| DVDD1 | P | G2 | Core power |
| CPU_WBEN[0] | I | G1 | Write byte enable, bit 0 |
| CPU_WBEN[1] | I | H4 | Write byte enable, bit 1 |
| CPU_WEN | I | H1 | Write signal, active low |
| CPU_OEN | I | H2 | Output enable, active low |
| CS_DATA[7] | B, PD | J2 | Video data input from camera module, bit [7] |
| CS_DATA[6] | B, PD | J1 | Video data input from camera module, bit [6] |
| CS_DATA[5] | B, PD | J4 | Video data input from camera module, bit [5] |
| CS_DATA[4] | B, PD | K2 | Video data input from camera module, bit [4] |
| OVDD2 | P | K1 | IO power |
| OVSS2 | G | L2 | IO ground |
| TEST | I | M1 | Test mode enable |
| LCD_DATA[4] | B | L1 | Data bus to the LCD panel, bit [4] |
| LCD_DATA[5] | B | M2 | Data bus to the LCD panel, bit [5] |
| CPU_DATA[4] | B | L3 | Data bus between host CPU and VC0568, bit [4] |
| CPU_DATA[5] | B | M3 | Data bus between host CPU and VC0568, bit [5] |
| OVSS3 | G | J5 | IO ground |
| OVDD3 | P | M4 | IO power |
| CPU_DATA[6] | B | L4 | Data bus between host CPU and VC0568, bit |

| | | | |
|---|---|---|---|
| | | | [6] |
| CPU_DATA[7] | B, | L5 | Data bus between host CPU and VC0568, bit [7] |
| LCD_DATA[6] | B | M5 | Data bus to the LCD panel, bit [6] |
| LCD_DATA[7] | B | J6 | Data bus to the LCD panel, bit [7] |
| DVSS2 | G | M6 | Core ground |
| DVDD2 | P | L6 | Core power |
| GPIO[2] | B, PU | L7 | Global purpose IO pin, bit [2] |
| GPIO[3] | B, PU | M7 | Global purpose IO pin, bit [3] |
| GPIO[4] | B, PU | J7 | Global purpose IO pin, bit [4] |
| LCD_CS1N | B | J8 | LCD Chip Select for main panel |
| LCD_CS2N | B | M8 | LCD Chip Select for sub panel |
| CPU_CS1N | I | L8 | Chip select 1, active low |
| CPU_CS2N | I | L9 | Chip select 2, active low |
| OVDD4 | P | M9 | IO power |
| OVSS4 | G | J9 | IO ground |
| CS_DATA[3] | B, PD | M10 | Video data input from camera module, bit [3] |
| CS_DATA[2] | B, PD | L10 | Video data input from camera module, bit [2] |
| CS_DATA[1] | B, PD | M11 | Video data input from camera module, bit [1] |
| CS_DATA[0] | B, PD | M12 | Video data input from camera module, bit [0] |
| CPU_ADDR[0] | B | L11 | Address bus between host CPU and VC0568, bit [0] |
| CPU_ADDR[1] | B | L12 | Address bus between host CPU and VC0568, bit [1] |
| CPU_ADDR[2] | B | K11 | Address bus between host CPU and VC0568, bit [2] |
| CPU_ADDR[3] | B | K12 | Address bus between host CPU and VC0568, bit [3] |
| OVSS5 | G | H9 | IO ground |
| OVDD5 | P | J12 | IO power |
| LCD_DATA[8] | B | J11 | Data bus between host CPU and VC0568, bit [8] |
| LCD_DATA[9] | B | H11 | Data bus between host CPU and VC0568, bit [9] |
| LCD_DATA[10] | B | H12 | Data bus between host CPU and VC0568, bit [10] |
| LCD_DATA[11] | B | G9 | Data bus between host CPU and VC0568, bit [11] |
| VDDA | P | G11 | PLL power |
| VSSA | G | G12 | PLL ground |
| DVSS3 | G | F9 | Core ground |
| DVDD3 | P | F11 | Core power |
| CS_SCK | B | E11 | Serial clock for camera module control |

| | | | |
|---|---|---|---|
| CS_SDA | B | E12 | Serial data for camera module control |
| LCD_RST | B | E9 | LCD panel reset |
| LCD_RS | B | D11 | LCD Register Select index and command register |
| CS_PWDN | B | D12 | Power down signal of camera module |
| CS_ENB | B | C11 | Camera module enable signal |
| OVDD6 | P | C12 | IO power |
| XCLK | I | F12 | Clock from the host CPU or oscillator |
| OVSS6 | G | D9 | IO ground |
| CPU_RS | I, PD | B12 | Register select |
| CPU_A8 | I, PD | A12 | Address bus / HOST register select |
| CPU_ADDR[4] | B | B11 | Address bus between host CPU and VC0568, bit [4] |
| CPU_ADDR[5] | B | A11 | Address bus between host CPU and VC0568, bit [5] |
| CPU_ADDR[6] | B | B10 | Address bus between host CPU and VC0568, bit [6] |
| CPU_ADDR[7] | B | B9 | Address bus between host CPU and VC0568, bit [7] |
| OVDD7 | P | A10 | IO power |
| OVSS7 | G | D8 | IO ground |
| LCD_DATA[12] | B | A9 | Data bus between host CPU and VC0568, bit [12] |
| LCD_DATA[13] | B | B8 | Data bus between host CPU and VC0568, bit [13] |
| LCD_DATA[14] | B | A8 | Data bus between host CPU and VC0568, bit [14] |
| LCD_DATA[15] | B | D7 | Data bus between host CPU and VC0568, bit [15] |
| LCD_WRN | B | D6 | LCD Write strobe to be asserted in write operation |
| LCD_RDN | B | A7 | LCD Read strobe to be asserted in read operation |
| DVDD4 | P | B7 | Core power |
| DVSS4 | G | B6 | Core ground |
| CS_VSYNC | B, PD | A6 | Vertical synchronous signal to/from camera module |
| CS_HSYNC | B, PD | D5 | Horizontal synchronous signal to/from camera module |
| CS_CLK | B, | A5 | Synchronous clock of camera data transfer (max.27MHz) |
| CS_RSTN | B, | B5 | Camera module reset signal |
| INT | B, | B4 | Interrupt to the host CPU |

| | | | |
|---|---|---|---|
| RSTN | I, S | A4 | Reset signal, active low |
| OVDD8 | P | A3 | IO power |
| OVSS8 | G | B2 | IO ground |
| CONF[0] | I | D4 | Configuration pin for CPU bus, bit 0 |
| CONF[1] | I | B3 | Configuration pin for CPU bus, bit 1 |
| CONF[2] | I | A1 | Configuration pin for CPU bus, bit 2 |

I = Input
O = Output
B = Bi-directional
P = Power
G = Ground
PD = Pull down
PU = Pull up
S = Schmitt trigger

# 4. System block diagram

Figure 4-1 shows the system block diagram of a typical camera phone. VC0568 is the bridge between the baseband processor and LCD module, enabling mobile phones to capture and display still images and video clips at real-time. Most of the display and camera functions are conducted by VC0568, which will greatly reduce the burden on host CPU for computation-intensive image and graphics processing.

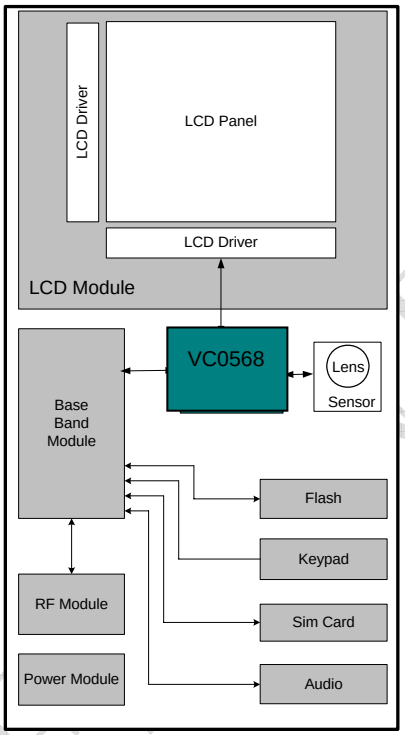



Figure 4-1 VC0568 system block diagram

## 5. Chip block diagram

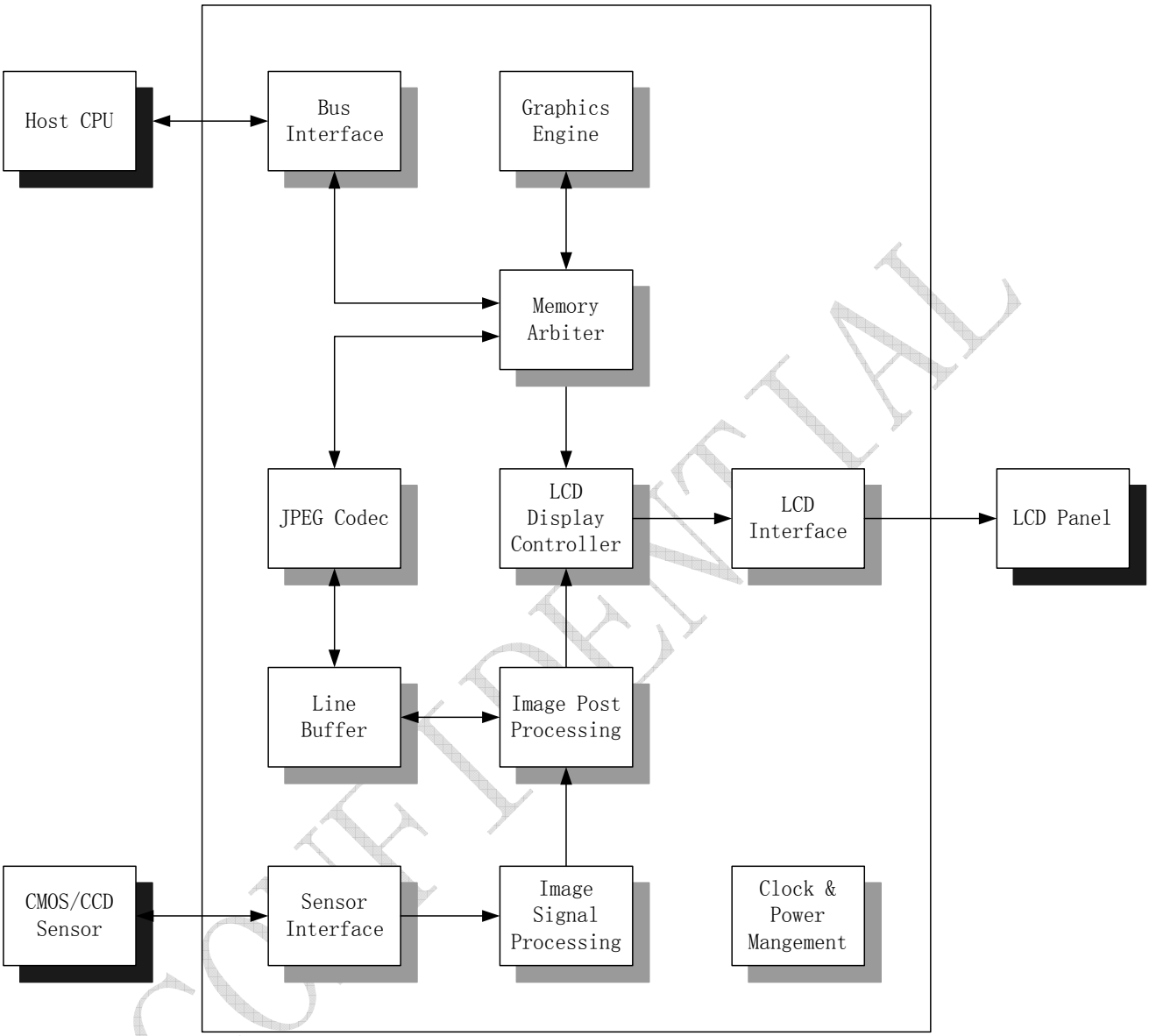



Figure 5-1 VC0568 Block Diagram

The main internal blocks in VC0568 are:

- **Sensor interface (SIF)**

The image data of the YUV422 format or Bayer pattern is captured synchronously. The sensor clock is generated by VC0568 and it can be adjusted according to the requirement with the maximum 27 MHz, and the pixel rate can up to 13.5M. The maximum resolution from the sensor is 1.3Mega pixel. Serial bus interface is supported for controlling the sensor.

- **Image signal processing (ISP)**

If the image data from the sensor is in RGB Bayer format, the ISP unit is used to convert it into YUV422 format. The ISP unit includes CFA-interpolation, noise reduction, sharpness enhancement, color correction, gamma correction, etc.

- **Image post processing (IPP)**

This module is used to add some special effects on the image for capture and display, such as relief, sephia, color range, negative, etc. The resolution of the input image from the sensor or host CPU may be not suit for display or capture, so we should convert it to appropriate size according to the screen display size or the capture resolution initialized by the user.

- **LCD display controller (LCDC)**

This module generates the correct data for LCD panel to display. Alpha blending and overlay function between video and graphics from host CPU are supported. Rotation (90, 180 and 270 degree), mirror (horizontal and vertical) and gamma correction on video plane are all supported in this module.

- **LCD panel interface (LCDIF)**

VC0568 supports TFT and STN-type LCD panels up to CIF resolution (352x288). It communicates with the LCD panel through standard asynchronous 8/16 bit data bus with the color depth of 4/8/12/16/18 bit per pixel. Direct interface between host CPU and LCD panel is also supported.

- **JPEG codec (JPEG)**

VC0568 has an embedded JPEG codec for both image compression and decompression. The input of the encoder comes from either the sensor or the host CPU under different working modes, and the output of the encoder is saved in on-chip SRAM for host CPU to read. The input of the decoder is from the on-chip SRAM which can be accessed by the host CPU and the decompressed data is sent back to host CPU or LCD display. The JPEG CODEC supports YUV422, YUV411, YUV420, YUV400 data format.

- **Memory Arbiter (MARB)**

The built-in 384KByte SRAM is used for storing the JPEG image data and graphics data. The size and position of graphics buffer and JPEG buffer can be configured dynamically. Some modules, such as JPEG, BIU, GE, STO, LCDC and IPP will address the on-chip SRAM. The memory arbiter will arrange the request from these modules and then response correctly.

- **Line buffer (LBUF)**

Two sets of 8-line buffer (1280x8x2 Bytes) are built in VC0568 for converting the data from line sequence to block sequence in capture mode and from block sequence to line sequence in display mode and decoder mode. The line buffer unit controls data read/write access to 8-Line Buffer. The two sets of 8-line buffer is configured as ping-pang architecture in capture and display modes. In decoder mode, one set is used as the FIFO to change

block sequence to line sequence and the other is used for data storage after resizing.

- **Bus interface (BIU)**

The host CPU can read/write the control registers and on-chip SRAM of VC0568 via host interface unit. VC0568 supports most popular CPUs such as ARM, XScale, and other 60/80-series CPUs. The data bus is 8bit/16bit (synchronous or asynchronous). The internal control bus is AMBA.

- **Graphics Engine (GE)**

VC0568 comes with a powerful graphics engine along with on-chip graphics buffer for 2D graphics acceleration operations such as BitBLT, ROPs, and line drawing. The on-chip SRAM is used as the display memory. The input to the graphics engine either comes from the host CPU or the display memory. With the built-in graphics engine, the host CPU is freed from most of the display function.

- **System Controller (CPM, including clock, reset and power management)**

VC0568 has a variety of power management mechanisms to reduce power consumption. The internal clock can be stopped or modified by the clock control registers, and the internal PLL oscillation may be stopped under PLL bypass mode (note that the performance depends on the input clock frequency in PLL bypass mode). Also, the gated clock function stops the clock of non-operation block automatically. This unit also controls the action of the on-chip analog phase-locked-loop (PLL).

## 6. Chip Configuration

The CONF pin is used to configure the chip and should be connected to the VSS or VDD before chip reset.

| Configuration input | Description |
|---|---|
| CONF[2:0] | Host bus interface type<br>“000” : type 0;<br>“001” : type 1;<br>“010” : type 2;<br>“011” : type 3;<br>“100” : type 4;<br>“101” : type 5;<br>“110” : type 6;<br>“111” : type 7; |

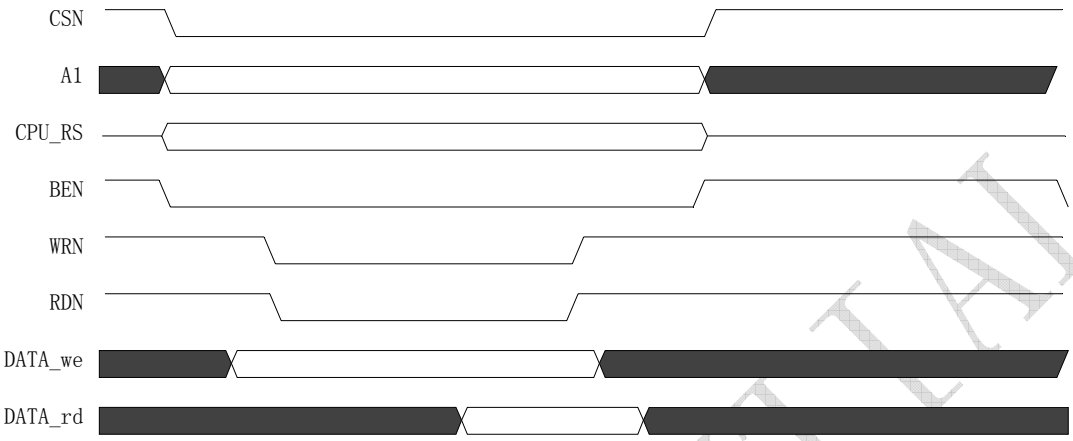
For different bus type, the host interface pin can have different mapping, which can be seen in the following table.

| Pin name | Type0 | Type1 | Type2 | Type3 | Type4 | Type5 | Type6 | Type7 |
|---|---|---|---|---|---|---|---|---|
| ADDR [7:0] | DATA [15:8] | DATA [15:8] | DATA [15:8] | DATA [15:8] | ADDR [7:0] | ADDR [7:0] | ADDR [7:0] | ADDR [7:0] |
| CPU_A8 | A1 | A1 | A1 | A1 | CPU_A8 | CPU_A8 | CPU_A8 | CPU_A8 |
| CPU_RS | Low | Low | Low | Low | CPU_RS | CPU_RS | CPU_RS | CPU_RS |
| DATA | DATA [7:0] | DATA [7:0] | DATA [7:0] | DATA [7:0] | DATA [7:0] | DATA [7:0] | DATA [7:0] | DATA [7:0] |
| CSN | CS# | CS# | CS# | CS# | CS# | CS# | CS# | CS# |
| RDN | RD# | RD# | RDL# | high | RD# | RD# | RDL# | high |
| WEN | WR# | high | WRL# | R/W# | WR# | high | WRL# | R/W# |
| BEN[1] | UBE# | WRU# | RDU# | UDS# | UBE# | WRU# | RDU# | UDS# |
| BEN[0] | LBE# | WRL# | WRU# | LDS# | LBE# | WRL# | WRU# | LDS# |

A1: address/data select pin
RDL#: read data low byte enable
RDU#: read data high byte enable
WRL#: write data low byte enable
WRU#: write data high byte enable
R/W#: CPU write/read signal (68 type)
UBE#: upper byte enables
LBE#: low byte enables
LDS#: low data select pin

UDS#: upper data select pin

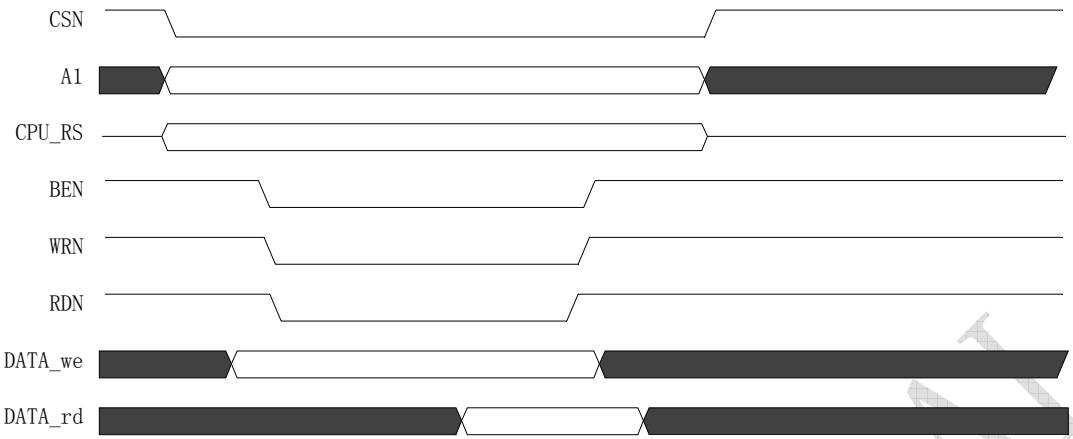
## 6.1 Multiplex 80 Type0




Note: WRN and RDN share using the BEN and don't care the CPU_RS value.

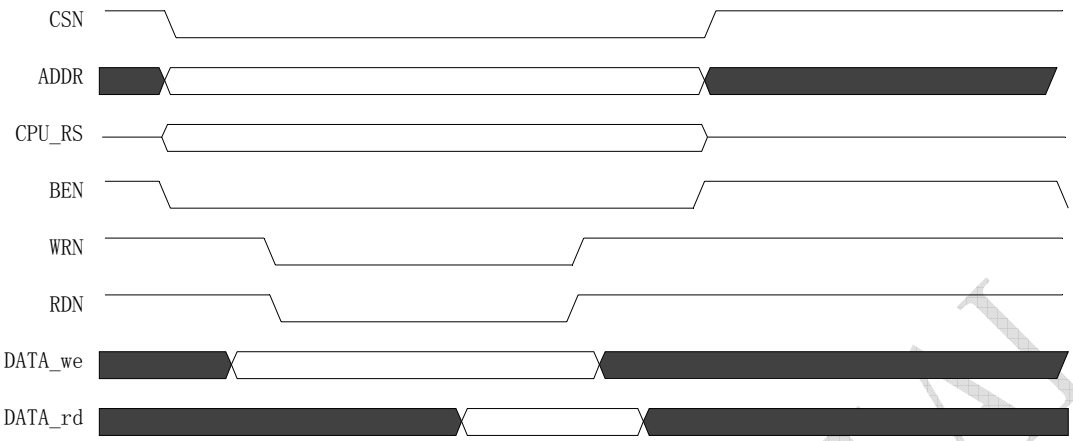
## 6.2 Multiplex 80 Type1

## 6.3 Multiplex 80 Type2



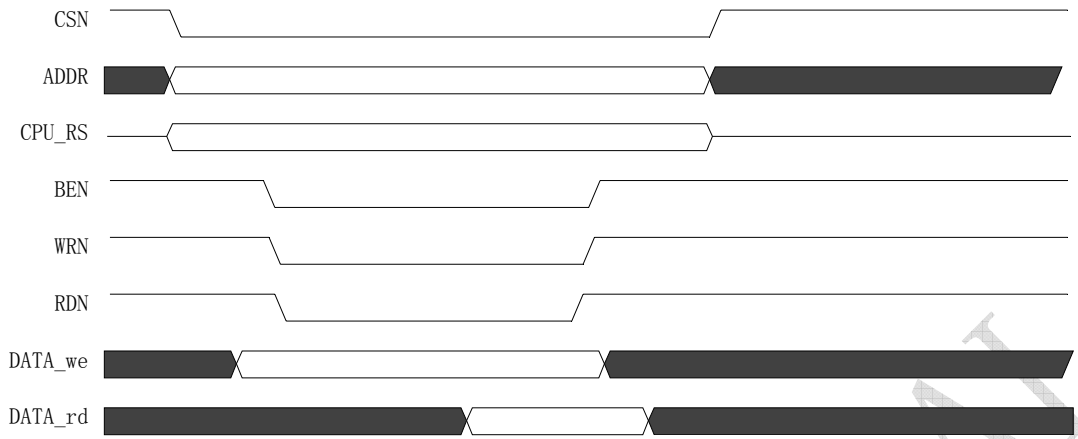

## 6.4 Multiplex 68 Type3

## 6.5 Separate Page 80 Type4




## 6.6 Separate Page 80 Type5

## 6.7 Separate Page 80 Type6




## 6.8 Separate Page 68 Type7

# 7. Operation Mode

The following operation modes are supported in VC0568 accompanied with Camera module and LCD panel:

## 7.1 Viewfinder Mode

In viewfinder mode, continuous video stream (up to 30fps) from sensor is shown on LCD panel with no frame delay. The user can adjust the zooming factor and image of different resolution will be displayed on LCD. When the user is happy with the image frame on display, he or she can push a button and capture it. Then the chip will go to the capture mode.

In viewfinder mode, the following features are supported:

- Video streaming at high frame rate (up to 30fps)
- No frame delay (What you see is what you capture!)
- Zoom in/out
- Add frame on the video
- Configurable display window

## 7.2 Capture Mode

VC0568 can capture still image, multi-shot and video clip.

When capture still image, the user first chose an appropriate frame in viewfinder mode, then he can press a capture button and the next frame from the image sensor will be captured. The JPEG compression image is stored in the internal SRAM and the host CPU can read the data. The user can choose the image size to be captured and whether there is a ‘frame’ outside the captured image or not. VC0568 have on-chip buffer for capturing high-quality still image up to 1.3M pixels in JPEG format. Thumbnail with configurable size can be generated accompanied with the JPEG image data.

When capture multi-shot, the user first push the capture button, then VC0568 will capture consecutive TBD images at TBD internal from image sensor. The images will be resized to VGA size and compressed as JPEG files along with a thumbnail version, and stored in on-chip buffer. Each image will be assigned a unique number internally for reference. The thumbnail images will be sent to LCD for display side by side. When user selects one of the thumbnail images, the corresponding VGA sized image will be sent to LCD for display at right size and bit depth. 2-D graphics functions (including special image effect) are supported in capture mode.

After the user pushes the capture button, VC0568 will capture the video stream from image sensor, until he/she pushes the stop button. The video stream will be compressed as AVI file, and then sent to baseband processor. At the same time, video frames of right size and bit-depth will be sent to LCD for display. 2-D graphics functions (including special image effect) are supported in capture mode. VC0568 will allow user to capture video in two resolutions: 320 x 240 and 160 x 120.

The captured still image, multi-shot and video clip can be sent to the host CPU or the storage card.

In capture mode, the following features are supported

- Capture still images up to 1.3Mega resolution
- Capture SIF (320x240), QSIF (160x120) and QQSIF (80x60) MJEPG video clip
- Capture still image with various resolution of thumbnail
- Capture still image with overlay
- Capture still image with alpha-blending
- Capture multi-shot up to VGA resolution

## 7.3 Display Mode

Under display mode, JPEG image or AVI saved in host memory or the storage card will be downloaded to VC0568, where it will be prepared (right size and bit depth) for LCD display. 2-D graphics functions are supported in capture mode.

In display mode, the following features are supported:

- Receive JPEG still image or MJPEG video clip from host CPU
- Decode and display on LCD with right size and color depth
- Support various image format: 4:4:4, 4:2:2, 4:1:1, 4:2:0
- Support JPEG image up to VGA resolution
- Resize the image with anti-aliasing pre-filtering
- Add frame to the image
- Add special effect to the image

## 7.4 JPEG decode mode

It is possible to use VC0568 as a JPEG decoding engine. When it is used as a JPEG decoder, the JPEG data is written to internal SRAM similar to the display mode and then decompressed by JPEG codec. But the decompressed data is sent back to the host CPU, other than LCD panel. The decoding result (YUV444/YUV422/YUV411/YUV420) is written in 8-line buffer. When data of 8 lines (YUV422/YUV411/YUV444) or 16 lines (YUV420) is decompressed, an interrupt is issued and the host CPU will read the data. Then the host

CPU will restart the decompression. Then 'Interruption-read-restart' repeats until decompression of one frame complete.

In JPEG decoder mode, the following features are supported:

- Receive JPEG image from host CPU
- Decode the JPEG image to YUV image data
- Add optional special effect to the image
- Resize the image data to specific resolution
- Send the YUV image data back to host CPU
- Support 4:4:4, 4:2:2, 4:1:1, 4:2:0
- Support JPEG image up to 1.3M resolution

## 7.5 JPEG Encode Mode

VC0568 can also be used as a JPEG encoder. At this mode, image data can be encoded into JPEG format by writing the image data in the specific registers one by one. Data of YUV422/YUV411/YUV420/YUV400 is written to the register in block sequence (8x8). The compressed JPEG data is saved in the internal SRAM and then is read by the host CPU after one frame is completed.

In JPEG encoder mode, the following features are supported:

- Receive YUV image data from host CPU
- Encode the image to JPEG format
- Send the JPEG image back to host CPU
- Support 4:2:2, 4:1:1, 4:2:0
- Support JPEG image up to 1.3M resolution

## 7.6 Through Mode

In this mode, the camera functions are disabled. The host CPU will read/write the LCD module directly. VC0568 support two ways for interfacing LCD panel in this mode: i) through registers for forwarding the index and the data to the LCD panel. Conversion from 8bit to 16bit of can be supported; ii) directly mapping the data and address from host CPU to LCD panel and there is no registers between host CPU and LCD panel, just like the host CPU interface LCD panel directly.

In through mode, the following features are supported:

- Video function is disabled
- Host CPU update LCD panel directly
- Directly pin mapping between host CPU and LCD module
- Index register for address and data for host CPU to update LCD
- Low power

## 7.7 Direct Display Mode

In this mode, the camera functions are disabled. The host CPU will writes the graphics data to the LCD panel through the on-chip graphics SRAM. 2-D graphics engine is supported at this mode. Direct data (16bpp, 24bpp and 32bpp) and indirect data (4 and 8bpp) are supported to write to the SRAM. For indirect data, a color palette table is used for converting to 16-bit direct color data.

In direct display mode, the following features are supported:

- Video function is disabled
- Host CPU reads/writes the frame buffer
- Optional BitBLT operation
- Optional 256 Raster operation
- Optional all angels line draw

# 8. Electrical Characteristics

## 8.1 Absolute Maximum Ratings

Permanent device damage may occur if absolute maximum ratings are exceeded, hence the maximum ratings must never be exceeded. Functional operation should be restricted to the conditions as detailed in recommended operating conditions. Exposure to the absolute maximum conditions for extended periods may affect device reliability.

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | $V_I$ | -0.5 | 4.6 | V |
| Output voltage | $V_O$ | -0.5 | 4.6 | V |
| Pre-driver power supply voltage | - | -0.5 | 2.5 | V |
| Post-driver power supply voltage | - | -0.5 | 4.6 | V |
| Operation temperature | $T_{OPT}$ | -40 | 125 | ℃ |
| Storage temperature | $T_{STG}$ | -65 | 150 | ℃ |

## 8.2 Recommended Operating Conditions for 3.3V IO Application

The recommended operating conditions are the recommended values for assuring normal logic operation. As long as the device is used within the recommended operating conditions, the electrical characteristics (DC and AC characteristics) described below are assured.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pre-driver supply voltage | VDD | 1.62 | 1.8 | 1.98 | V |
| I/O supply voltage | VDD33 | 2.6 | 3.3 | 3.63 | V |
| Input high voltage | $V_{IH}$ | 2.0 | - | 3.6 | V |
| Input low voltage | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Threshold point | $V_T$ | 1.46 | 1.59 | 1.75 | V |
| Schmitt trig low to high threshold point | $V_{T+}$ | 1.44 | 1.50 | 1.56 | V |
| Schmitt trig high to low threshold point | $V_{T-}$ | 0.88 | 0.94 | 0.99 | V |
| Junction temperature | $T_J$ | 0 | 25 | 125 | $^oC$ |
| Input leakage current | $I_L$ | - | - | ±10 | uA |
| Tri-state output leakage current | $I_{OZ}$ | - | - | ±10 | uA |
| Pull-up resistor | $R_{PU}$ | 50 | 65 | 100 | Kohm |
| Pull-down resistor | $R_{PD}$ | 40 | 56 | 107 | Kohm |
| Output low voltage @$I_{OL}$=4mA | $V_{OL}$ | - | - | 0.4 | V |
| Output high voltage @$I_{OH}$=4mA | $V_{OH}$ | 2.4 | - | - | V |
| Low level output current @$V_{OL}$=0.4V | $I_{OL}$ | 4.4 | 7.4 | 9.2 | mA |
| **High level output current @VOH=2.4V** | $I_{OH}$ | 5.0 | 10.2 | 15.0 | mA |

*The value of the supply voltage is the typical case.

## 8.3 Working Current

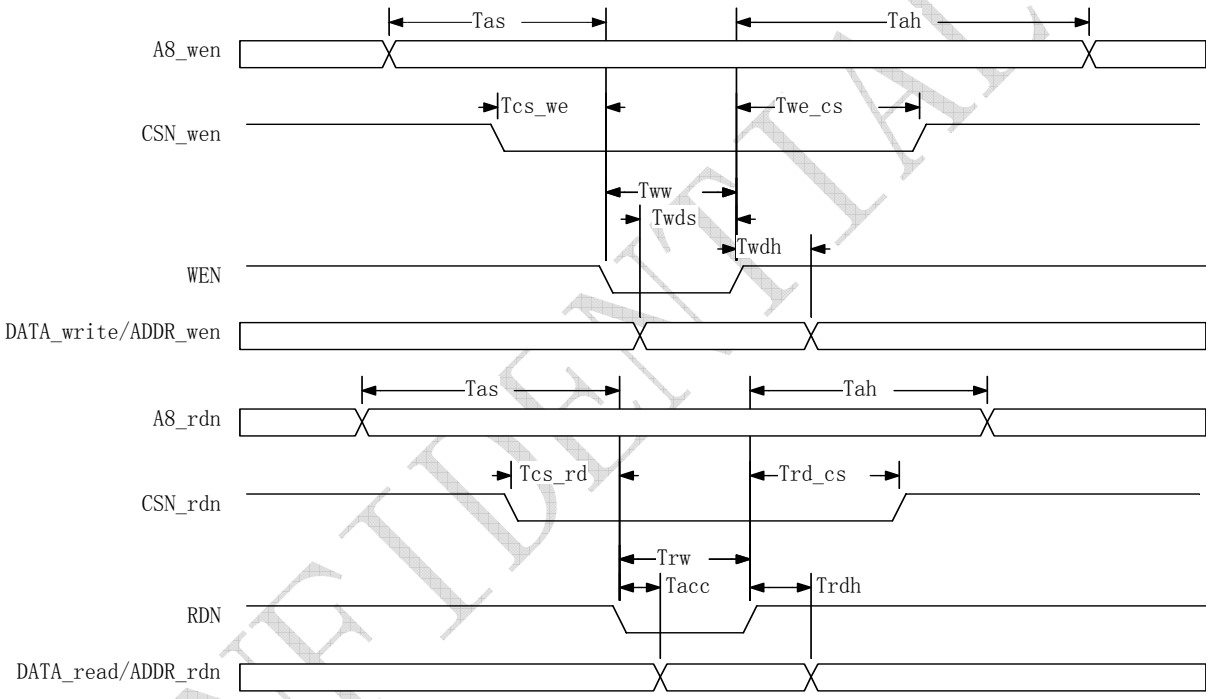
| Current / Mode style | 3.3V_IO (mA) | 1.8V (mA) | | | P (mW) |
|---|---|---|---|---|---|
| | | CORE | PLL | SUM | |
| Viewfinder Mode | 2.8 | 17.94 | 5.836 | 23.776 | 52.04 |
| Capture Mode | 2.83 | 22.15 | 5.826 | 27.976 | 59.70 |
| Display Mode | 2.85 | 10.179 | 5.832 | 16.011 | 38.22 |
| Bypass Mode | 0.173 | 0.041 | 0.003 | 0.044 | 0.39 |

## 8.4 AC Characteristics

This section describes the VC0568 AC characteristics, which consist of output delays, input setup and hold times and all the interface timing.

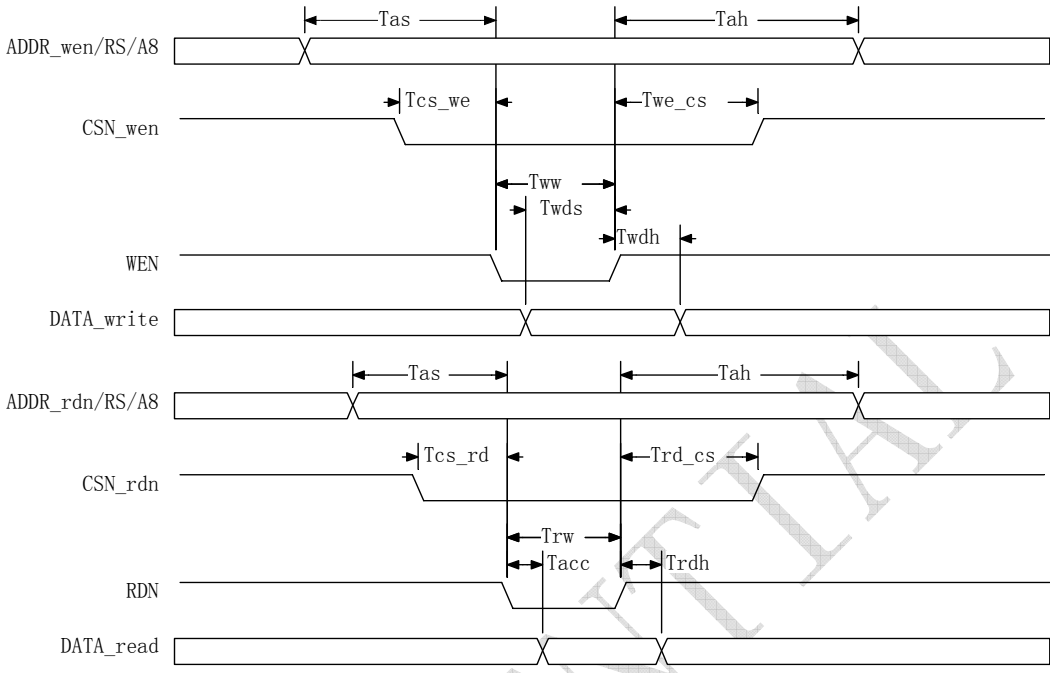
### 8.4.1 Host interface

#### 8.4.1.1 Multiplex interface characteristics



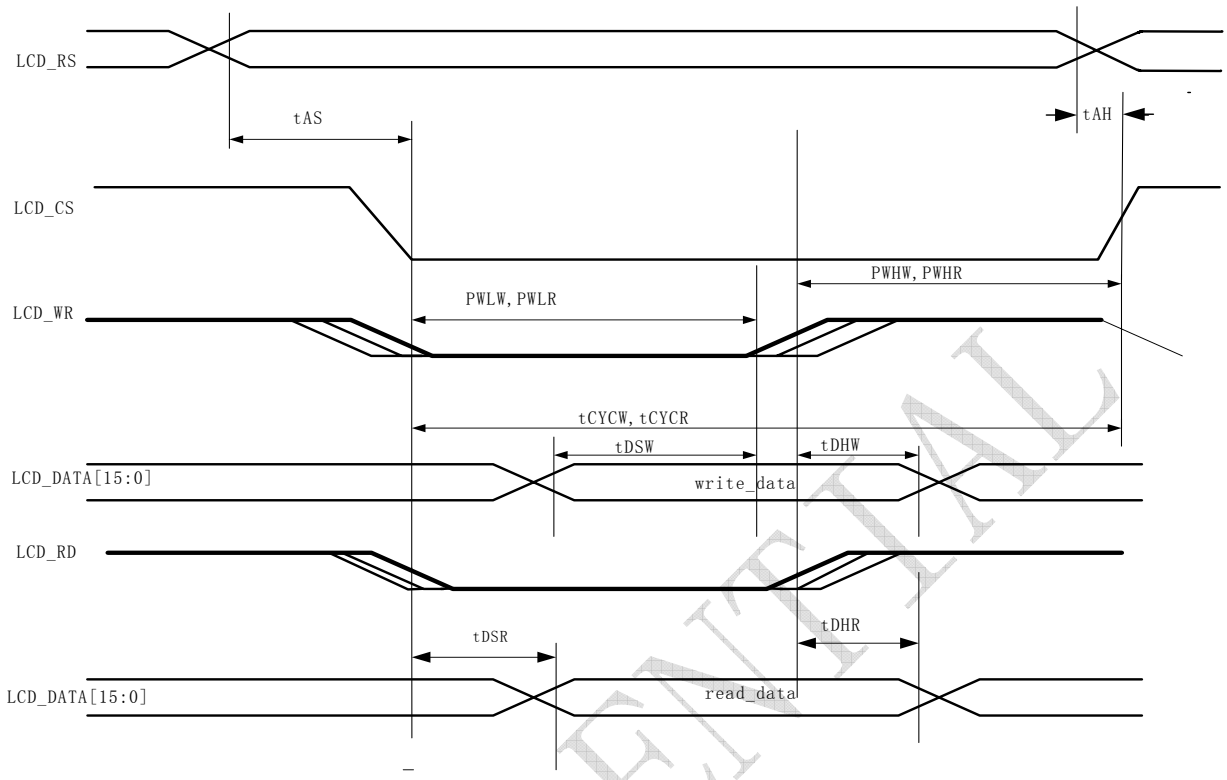

| Item | symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Address setup time | Tas | 0 | | | ns |
| Address hold time | Tah | 13.8 | 20 | | ns |
| Cs setup time at write status | Tcs_we | 0 | | | ns |
| Cs hold time at write status | Twe_cs | 0 | | | ns |
| Data setup time | Twds | 12.2 | 24 | | ns |
| Data hold time | Twdh | 8.8 | 10 | | ns |
| Write width | Tww | 120 | | | ns |
| Cs setup time at read status | Tcs_rd | 0 | | | ns |
| Cs hold time at read status | Trd_cs | 0 | | | ns |
| Read data access time | Tacc | 120 | | | ns |
| Read width | Trw | 120 | | | ns |
| Data hold time | Trdh | 2.5 | | | ns |

### 8.4.1.2 Separate page interface characteristics




| Item | symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Address setup time | Tas | 0 | | | ns |
| Address hold time | Tah | 13.8 | 20 | | ns |
| Cs setup time at write status | Tcs_we | 0 | | | ns |
| Cs hold time at write status | Twe_cs | 0 | | | ns |
| Data setup time | Twds | 12.2 | 24 | | ns |
| Data hold time | Twdh | 8.8 | 10 | | ns |
| Write width | Tww | 120 | | | ns |
| Cs setup time at read status | Tcs_rd | 0 | | | ns |
| Cs hold time at read status | Trd_cs | 0 | | | ns |
| Read data access time | Tacc | 120 | | | ns |
| Read width | Trw | 120 | | | ns |
| Data hold time | Trdh | 2.5 | | | ns |

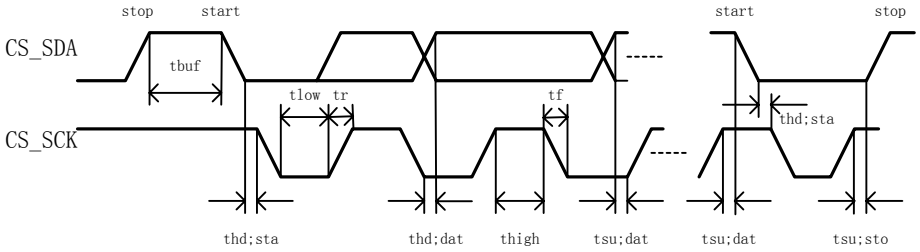
### 8.4.2 LCD panel interface




| Parameter | | sybmol | Min | Max | Unit |
|---|---|---|---|---|---|
| Bus cycle time | Write | $t_{CYCW}$ | 2 | | cycle * |
| | Read | $t_{CYCR}$ | 2 | | cycle |
| Write low-level pulse width | | $PW_{LW}$ | 1 | | cycle |
| Read low-level pulse width | | $PW_{LR}$ | 1 | | cycle |
| Write high-level pulse width | | $PW_{HW}$ | 1 | | cycle |
| Read high-level pulse width | | $PW_{HR}$ | 1 | | cycle |
| Setup time (LCD_RS to LCD_CS, LCD_WRN, LCD_RDN) | | $t_{AS}$ | 0 | | ns |
| Hold time (LCD_RS to LCD_CS) | | $t_{AH}$ | 0 | | ns |
| Write data setup time | | $t_{DSW}$ | 1 | | cycle |
| Write data hold time | | $t_{DHW}$ | 1 | | cycle |
| Read data setup time | | $t_{DSR}$ | 0 | | ns |
| Read data hold time | | $t_{DHR}$ | 0 | | ns |

* The cycle width is according to the VC0568 system clock period

### 8.4.3 Sensor Interface

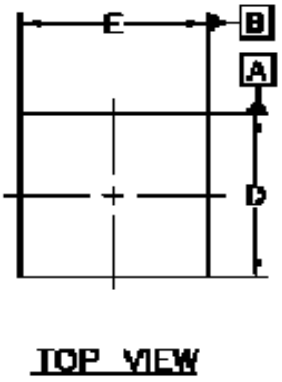



| Parameter | sybmol | Min | Max | Unit |
|---|---|---|---|---|
| CS_SCK clock frequency | $f_{sck}$ | 0 | 375 | kHz |
| Time that sensor serial bus must be free before a new transmission can start | $t_{buf}$ | 1.3 | - | us |
| Hold time for a start | $t_{hd;sta}$ | 0.6 | - | us |
| Low period of CS_SCK | $t_{low}$ | 1.3 | - | us |
| High period of CS_SCK | $t_{high}$ | 1.3 | - | us |
| Setup time for start | $t_{su;sta}$ | 0.6 | - | us |
| Data hold time | $t_{hd;dat}$ | 0 | - | us |
| Data setup time | $t_{su;dat}$ | 100 | - | ns |
| Rise time of both CS_SDA and CS_SCK | $t_r$ | - | 1 | us |
| Fall time of both CS_SDA and CS_SCK | $t_f$ | - | 300 | ns |
| Setup time for stop | $t_{su;sto}$ | 0.6 | - | us |

Because this chip don't use PCLK from sensor to sample sensor's synchronous signal and data, the output from sensor must be generate in same clock domain and have same setup and hold timing requirement.

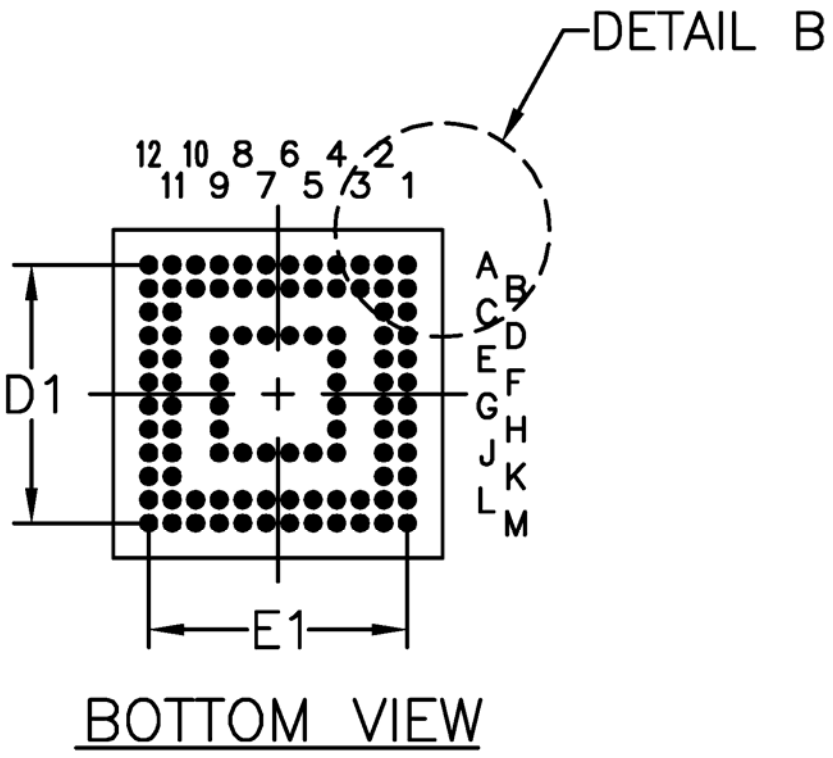
# 9. Mechanical dimensions

## 9.1 Top View



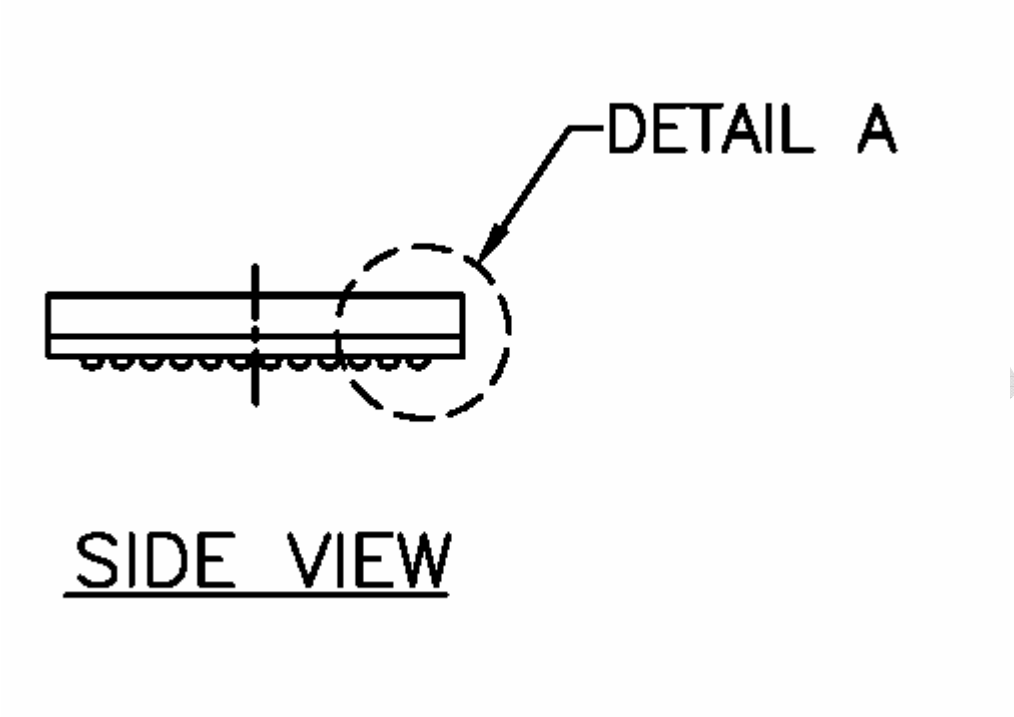

TOP VIEW

## 9.2 Bottom View

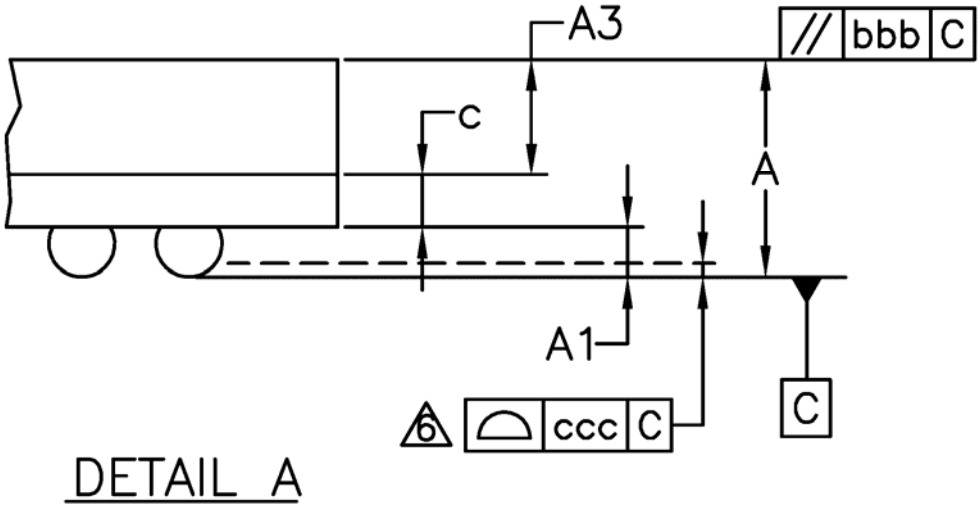



BOTTOM VIEW

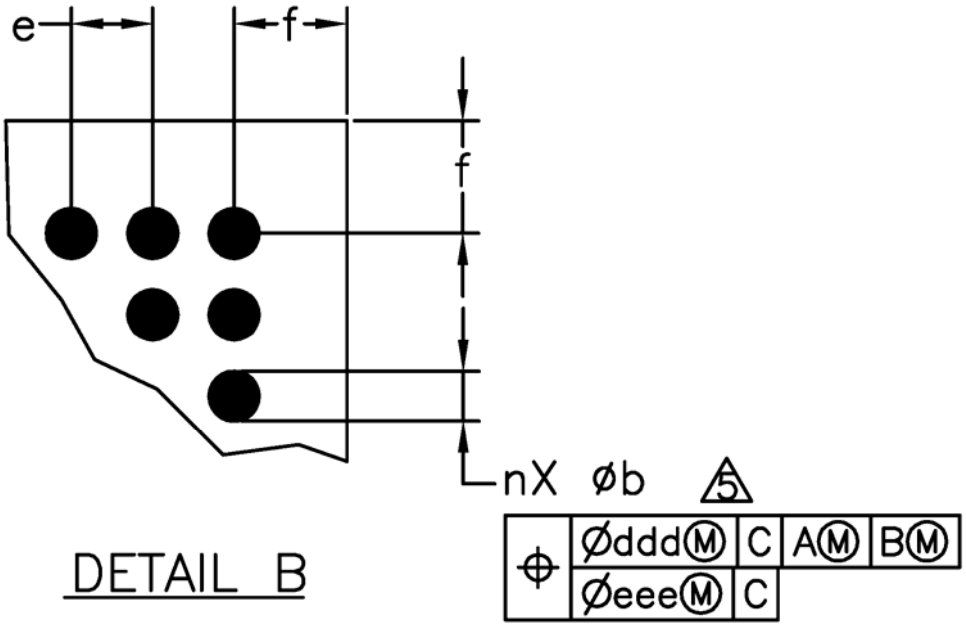
### 9.3 Side view




### 9.4 Delta A



## 9.5 Delta B



## 9.6 Dimensional Reference

| DIMENSIONAL REFERENCES | | | |
|---|---|---|---|
| REF. | MIN. | NOM. | MAX. |
| A | 0.94 | 1.09 | 1.24 |
| A1 | 0.17 | 0.22 | 0.27 |
| A3 | 0.50 | 0.55 | 0.60 |
| D | 6.80 | 7.00 | 7.20 |
| D1 | | 5.50 BSC. | |
| E | 6.80 | 7.00 | 7.20 |
| E1 | | 5.50 BSC. | |
| b | 0.25 | 0.30 | 0.35 |
| bbb | | | 0.20 |
| c | 0.27 | 0.32 | 0.37 |
| ccc | | 0.08 | |
| ddd | | | 0.15 |
| eee | | | 0.05 |
| e | | 0.50 BSC. | |
| f | 0.65 | 0.75 | 0.85 |
| M | | 12 | |
| N | | 100 | |

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. THE "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE AND SYMBOL "N" IS THE ACTUAL NUMBER OF BALLS AFTER DEPOPULATING.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. PRIMARY DATUM C IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
8. SUBSTRATE MATERIAL BASE IS BT RESIN.
9. THE OUTLINE DRAWING IS REFER TO JEDEC SPEC. MO-207 ISSUE G.
10. BALL MATRIX VARIATIONS CM-1.
11. FOR QUALIFICATION PURPOSE ONLY

## 9.7 Marking information

| | |
|---|---|
| **Marking Information** | Vimicro<br>VC0568-V33<br>100BGA-AR<br>……<br>…… |

## 10. Revision History

| Revision History | | | |
|---|---|---|---|
| **Version No.** | **Content of Revision** | **Corrector** | **Release Time** |
| 1.2 | 1.Update some register definition,<br>2.sensor data width: 8bit<br>lcd data width: 16bit<br>3.add marking information | Liujian | 4-12-2005 |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

## 11. Contact Information

Vimicro Corporation
15/F Shining Tower
No.35 Xueyuan Road
Haidian District, Beijing
P. R. China 100083
Tel: 86-10-68948888
Fax: 86-10-68944075
Web: http://www.vimicro.com

Vimicro Corporation – USA
1758 N. Shoreline
Mountain View, CA 94043
Tel: 1-650-966-1882
Fax: 1-650-966-1885

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课程网址：http://www.edatop.com/peixun/rfe/110.html

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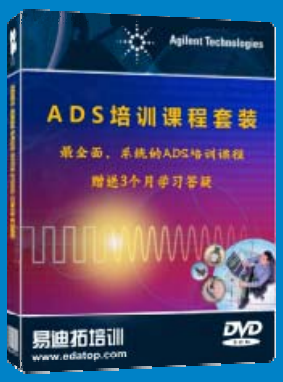


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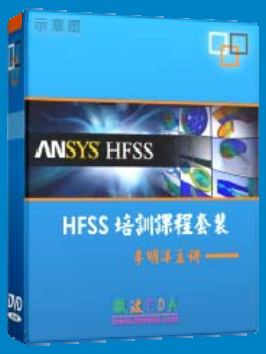
课程网址： http://www.edatop.com/peixun/ads/13.html

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## 13.56MHz NFC/RFID 线圈天线设计培训课程套装


套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

**详情浏览**：http://www.edatop.com/peixun/antenna/116.html

## 我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

## 联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com