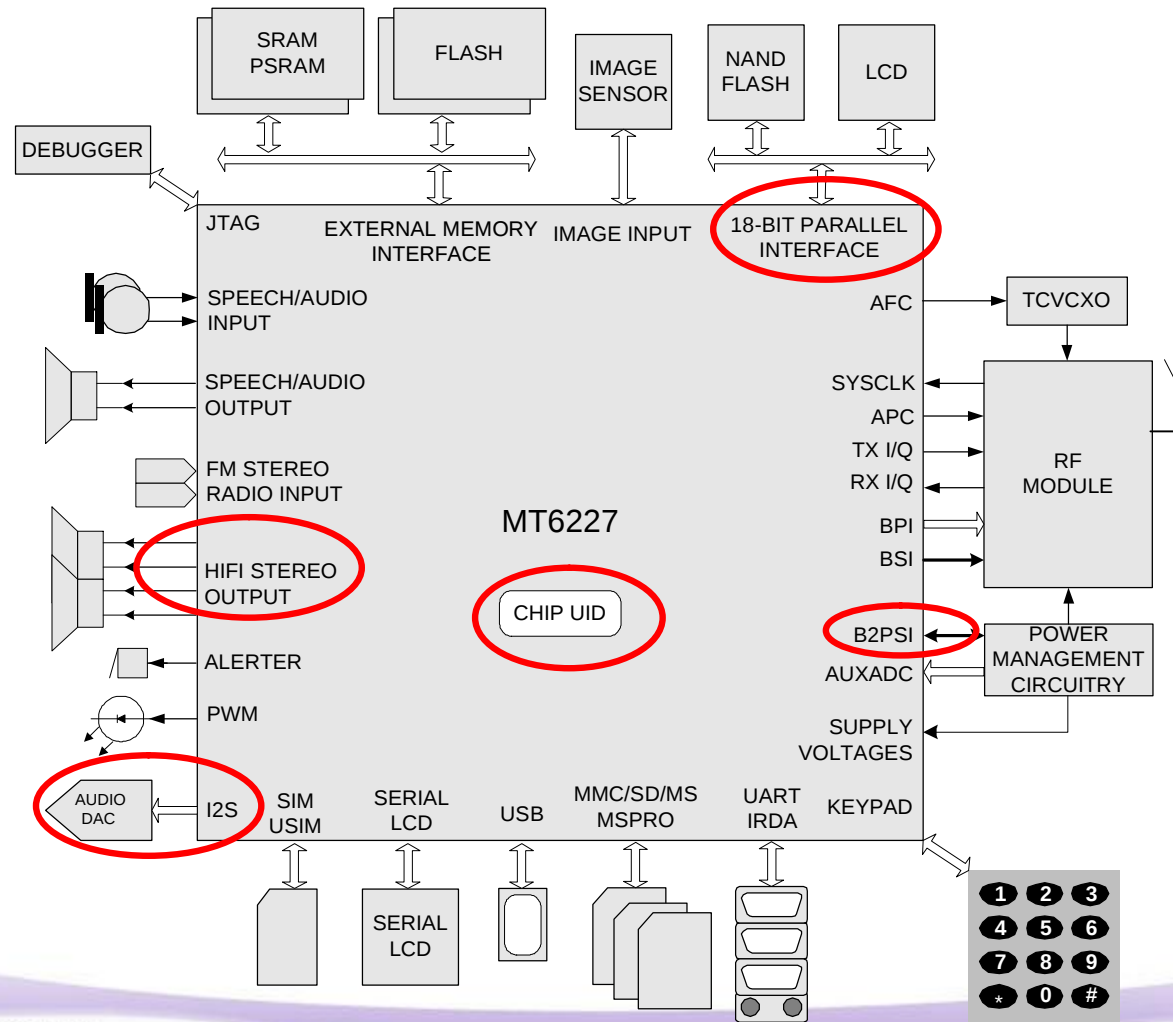


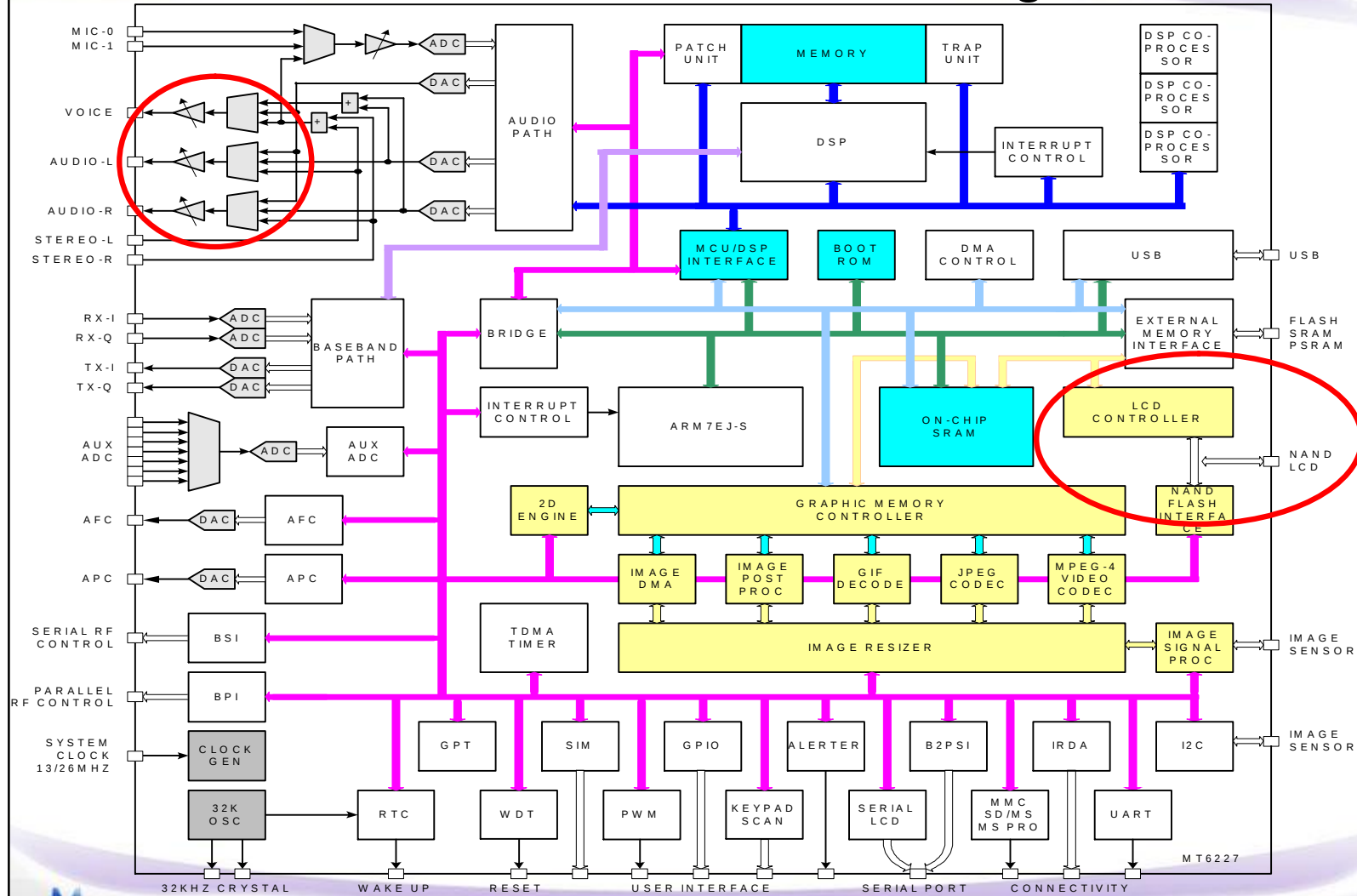
MT6226/7 and MT6228 Base Band Solution Introduction

*Ethan Lee
Media Tek
4 Jan. , 2006*

MT6226/7 Overview – Typical Application



MT6226/7 Overview – Block Diagram



MT6226/7 New Feature

- ISP
 - Capable of processing image of size up to **2M** pixels (MT6227)
 - Capable of processing image of size up to **VGA** pixels (MT6226)
 - Capable of processing image of size up to **1.3M** pixels (MT6226M)
 - Support **12MHz-based** and **13MHz-based** sensor clock
 - YUV422/RGB565 input data format
 - Sensor gamma compensation
 - Crosstalk compensation
 - Defect compensation
 - Lens shading compensation
 - Low light accumulation mode
 - **Synchronous flash light control (GPIO6)**
 - Enhanced Bayer interpolation
- JPEG encoder
 - Provide 4 quantization level for programmable compression quality
- Security engine
 - Secure key for code protection
 - Unique chip ID

MT6226/7 New Feature

- **18-bit** LCM/NAND FLASH interface
 - Support 8/9/16/18-bit LCM interface
 - Support 8/16-bit NAND FLASH interface
 - NFI supports 2 chip-select for dual-die device
- LCM controller
 - **Support gamma correction**
- Internal memory
 - Total 284KB internal RAM
- MSDC
 - Support SDIO for WiFi application
- BSI
 - Support 4-wire interface for RF calibration
- Audio
 - **Support FM recording**
 - Support EDI (**I2S**)
 - Support aacPlus decode
 - Supports AMR codec to adaptively optimize speech and audio quality.
 - HE-AAC codec is implemented to deliver CD-quality audio at low bit rates.

MT6227 Power and GPIO

Power Supply	Symbol	MT6219 Voltage	MT6227 Voltage
Core	VDDK	1.2V	1.8V
RTC	AVDD_RTC	1.2V	1.5V
General I/O	VDD33	2.8V	2.8V
Memory card I/O	VDD33_MC	2.8V	2.8V
EMI I/O	VDD33_EMI	1.8~2.8V	1.8~2.8V
Sensor I/O	VDD33_IS	2.8V	1.8~2.8V
Analog I/O	AVDD	2.8V	2.8V
USB I/O	VDD33_USB	3.3V	3.3V

Ball	Ball name	GPIO function 0	GPIO function 1	GPIO function 2
U2	GPIO0	GPIO0	DICK	DSP_GPO3
M19	GPIO1	GPIO1	BSI_RFIN	
B18	GPIO6	GPIO6	ARM_CLK	DSPLD2
K2	LPCE1B	GPIO24	LPCE1B	NCE1B
H15	URXD3	GPIO33	URXD3	EINT7
H16	UTXD3	GPIO34	UTXD3	EINT5
J18	URXD2	GPIO35	URXD2	UCTS3
J19	UTXD2	GPIO36	UTXD2	URTS3
F6	NLD17	GPIO56	NLD17	MCDA7
G6	NLD16	GPIO55	NLD16	MCD6

MT6227 Package

	MT6219	MT6227
Package	TFBGA-293	TFBGA-296

**ARM**

MT6227A
DDDD-###
LLLLL

S

MT6227A: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Lot No.
S: Special Code

MT6226/7 Overview – Platform Features

- General
- Integrated voice-band, audio-band and base-band analog front ends
- TFBGA 13mm×13mm, **296-ball**, 0.65 mm pitch package

- MCU Subsystem
- ARM7EJ-S 32-bit RISC processor
- High performance multi-layer AMBA bus
- Java hardware acceleration for fast Java-based games and applets
- Operating frequency: 26/52 MHz
- Dedicated DMA bus
- 14 DMA channels
- **284K** Bytes zero-wait-state on-chip SRAM
- On-chip boot ROM for Factory Flash Programming
- Watchdog timer for system crash recovery
- 2 sets of General Purpose Timer
- Circuit Switch Data coprocessor
- Division coprocessor

MT6226/7 Overview – Platform Features

- **External Memory Interface**
- Supports up to 8 external devices
- Supports 8-bit or 16-bit memory components with maximum size of up to 64M Bytes each
- Supports Flash and SRAM with Page Mode or Burst Mode
- Supports Pseudo SRAM
- Industry standard Parallel LCD Interface
- Supports multi-media companion chips with 8/16 bits data width
- Flexible I/O voltage of 1.8V ~ 2.8V for memory interface
- Configurable driving strength for memory interface
- **User Interfaces**
- 6-row × 7-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- SIM/USIM Controller with hardware T=0/T=1 protocol control
- 3 UARTs with hardware flow control and speed up to 921600 bps
- IrDA modulator/demodulator with hardware framer supports SIR mode of operation
- Real Time Clock (RTC) operating with a separate power supply
- General Purpose I/Os (GPIOs)
- 2 Sets of Pulse Width Modulation (PWM) Output
- Alerter Output with Enhanced PWM or PDM
- 4~10 external interrupt lines (**EINT0~7**)

MT6226/7 Overview – Platform Features

- **Connectivity**
 - Full-speed USB 1.1 Device controller
 - Multi Media Card/Secure Digital Memory Card/Memory Stick/Memory Stick Pro host controller
- **Security**
 - Supports security key for code protection
 - 56-bit unique/secret chip ID
- **Power Management**
 - Power Down Mode for analog and digital circuits
 - Processor Sleep Mode
 - Pause Mode of 32KHz clocking at Standby State
 - 7-channel Auxiliary 10-bit A/D Converter for charger and battery monitoring and photo sensing
- **Test and Debug**
 - Built-in digital and analog loop back modes for both Audio and Baseband Front-End
 - DAI port complying with GSM Rec.11.10
 - JTAG port for debugging embedded MCU

MT6226/7 Overview – MODEM Features

- **Radio Interface and Baseband Front End**
- GMSK modulator with analog I and Q channel outputs
- 10-bit D/A Converter for uplink baseband I and Q signals
- 14-bit high resolution A/D Converter for downlink baseband I and Q signals
- Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
- 10-bit D/A Converter for Automatic Power Control
- 13-bit high resolution D/A Converter for Automatic Frequency Control
- Programmable Radio RX filter
- 2 Channels bi-directional Baseband Serial Interface (BSI) with 3-wire or **4-wire** control
- 10-Pin Baseband Parallel Interface (BPI) with programmable driving strength
- Multi-band support

MT6226/7 Overview – MODEM Features

- Voice and Modem CODEC
- Dial tone generation
- Voice Memo
- Noise Reduction
- Echo Suppression / Echo Cancellation
- Advanced Sidetone Oscillation Reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- FR error concealment
- GSM channel coding, equalization and A5/1 and A5/2 ciphering
- GPRS GEA1 and GEA2 ciphering
- Programmable GSM/GPRS Modem
- Packet Switched Data with CS1/CS2/CS3/CS4 coding schemes
- GSM Circuit Switch Data
- GPRS Class 12

MT6226/7 Overview – MODEM Features

- **Voice Interface and Voice Front End**
- Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control (AGC) mechanism
- Voice power amplifier with programmable gain
- 2nd order Sigma-Delta A/D Converter for voice uplink path
- D/A Converter for voice downlink path
- Supports half-duplex hands-free operation
- Compliant with GSM 03.50

MT6226/7 Overview – Multi-Media Features

- LCD/NAND Flash Interface
- **18**-bit Parallel Interface supports 8/16 bit NAND flash and 8/9/16/18 bit Parallel LCD
 - 8 bit: NLD0~NLD7
 - 9 bit: NLD0~NLD8
 - 16 bit: NLD0~NLD15
 - 18 bit: NLD0~NLD17
- 8/16 bit NAND Flash Controller with 1-bit ECC correction for mass storages
- 2 Chip selects available for high-density NAND flash device
- Serial LCD Interface with 8/9 bit format support
- LCD Controller
- Hardware accelerated display
- Supports simultaneous connection to up to 2 parallel LCD and 1 serial LCD modules
- Supports format: RGB332, RGB444, RGB565, RGB666, **RGB888**
- Supports LCD panel maximum resolution up to 800x600 at 16bpp
- Supports hardware display rotation
- Capable of combining display memories with up to **4** blending layers
- **Accelerated Gamma correction with programmable gamma table.**

MT6226/7 Overview – Multi-Media Features

- **Image Signal Processor**
- 8/10 bit Bayer format image input
- YUV422 format image input
- Capable of processing image of size up to **2M** pixels. (MT6227)
- Capable of processing image of size up to **VGA** pixels. (MT6226)
- Capable of processing image of size up to **1.3M** pixels (MT6226M)
- Lens shading compensation
- Defect pixel correction
- **Synchronous** flash light control
- Optical black correction
- Color Correction Matrix
- Gamma Correction
- Automatic Exposure Control
- **Automatic focus control**
- Automatic White Balance Control
- Edge Enhancement Support
- Flexible I/O voltage of **1.8V ~ 2.8V**

MT6226/7 Overview – Multi-Media Features

- **JPEG Decoder**
- ISO/IEC 10918-1 JPEG Baseline and Progressive modes
- Supports all possible YUV formats, including grayscale format
- Supports all DC/AC Huffman table parsing
- Supports all quantization table parsing
- Supports restart interval
- Supports SOS, DHT, DQT and DRI marker parsing
- IEEE Std 1180-1990 IDCT Standard Compliant
- Supports progressive image processing to minimize storage space requirement
- Supports reload-able DMA for VLD stream
- **JPEG Encoder**
- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 Compliance
- Supports YUV422 and grayscale formats
- Standard DC and AC Huffman tables
- Provides 14 levels of encode quality

MT6226/7 Overview – Multi-Media Features

- **Image Data Processing**
- High throughput hardware scalar capable of tailoring image to arbitrary size
- Horizontal scaling in averaging method
- Vertical scaling in bilinear method
- Simultaneous scaling for MPEG-4 encode and LCD display
- YUV and RGB color space conversion
- Pixel format transform
- Boundary padding
- Accelerated Pixel-based luminance/chrominance processing: hue/saturation/intensity/color adjustment, Gamma correction and grayscale/invert/sepia-tone effects
- Accelerated Programmable Spatial Filtering : Linear filter, Non-linear filter and Multi-pass artistic effects
- Hardware accelerated image editing
- **2D Accelerator**
- Rectangle fill
- BitBlt: multi-BitBlt without transform, 7 rotate, mirror (transparent) BitBlt
- Alpha blending
- Line drawing: normal line, dotted line
- Font caching: normal font, Italic font
- Supports 16-bpp RGB565 and 8-bpp index color modes with one color palette inside
- Command queue with 32 levels

MT6226/7 Overview – Multi-Media Features

- MPEG-4/H.263 CODEC
- Hardware Video CODEC
- ISO/IEC 14496-2 simple profile:
- decode @ level 0/1/2/3
- encode @ level 0
- Supported visual tools for decoder: I-VOP, P-VOP, AC/DC prediction, 4-MV, Unrestricted MV, Error Resilience, Short Header
- Error Resilience for decoder: Slice Resynchronization, Data Partitioning, Reversible VLC
- Supported visual tools for encoder: I-VOP, P-VOP, Half-pel, DC prediction, Unrestricted MV, Reversible VLC, Short Header
- Supports encoding motion vector of range up to $-64/+63.5$ pixels
- ITU-T H.263 profile 0 @ level 10
- AAC/HE-AAC/AMR audio decode support
- AMR audio encode support

MT6226/7 Overview – Multi-Media Features

- Audio CODEC
- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set of 128 instruments and 47 sets of percussions
- PCM Playback and Record
- Digital Audio Playback
- High resolution D/A Converters for Stereo Audio playback
- Stereo analog input for stereo audio source
- Analog mixers for Stereo Audio
- HE-AAC decode support
- Audio Interface and Audio Front End
- Supports I2S interface
- High resolution D/A Converters for Stereo Audio playback
- Stereo analog input for stereo audio source
- Analog multiplexer for Stereo Audio
- Stereo to Mono Conversion
- FM radio recording

MT6226/7 Compare to MT6219 (1/2)

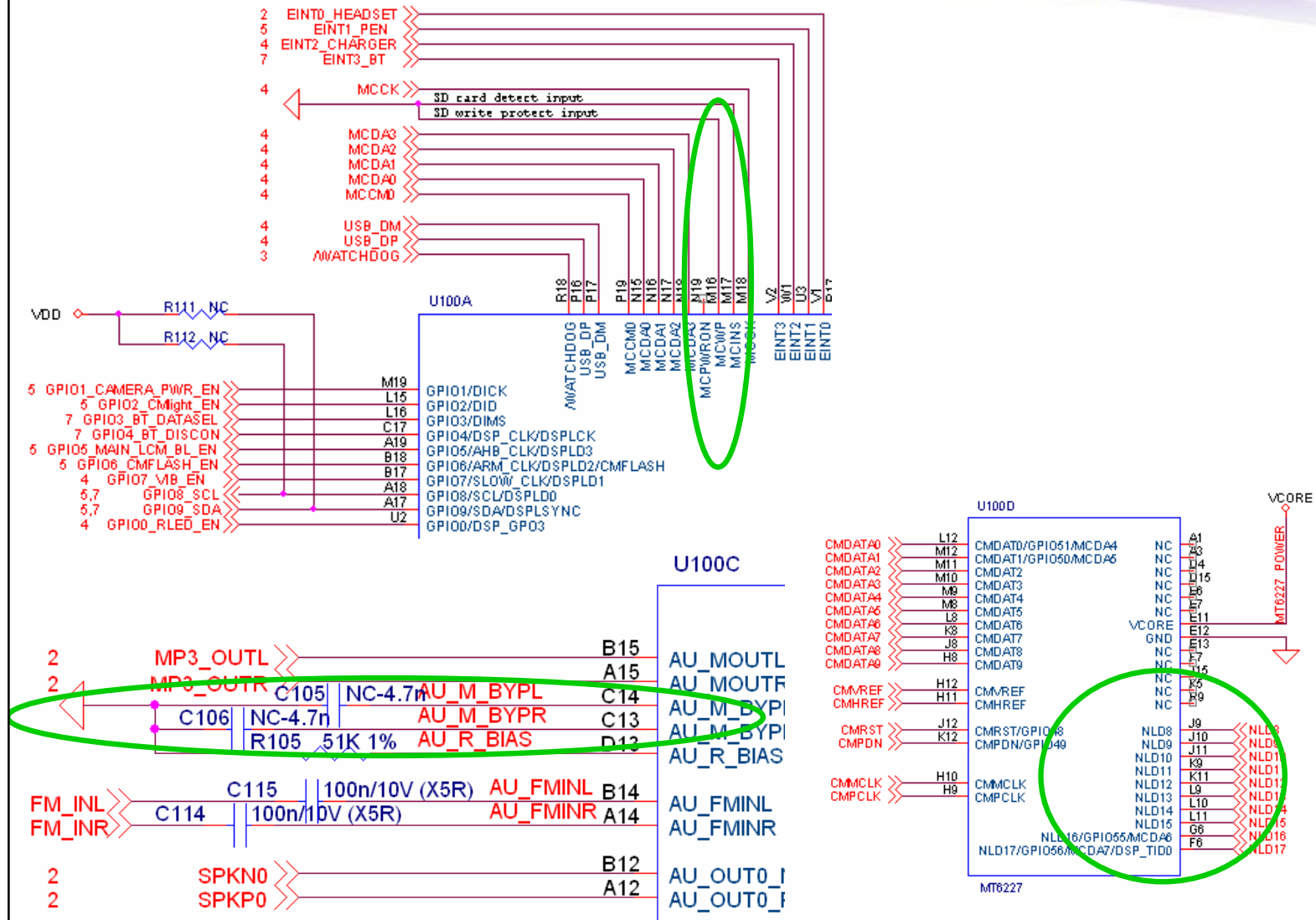
PIN	MT6227	MT6219	Need Modified Portion from MT6219 change to MT6227
A3	NC	VSS33	N/A
C13	AU_M_BYPR	AU_OUT1_P	MT6227->NC, don't add capacito, or it will generate pop noise (*No audio channel 1 in MT6227)
D4	NC	VDD33	N/A
D5	PLL_OUT	VSS33	MT6227->NC ; MT6219-> GND
D13	AU_RBIAS	AU_OUT1_N	Add 51K OHM (1%) to GND. (*No audio channel 1 in MT6227)
D15	NC	ESDM_CK	N/A
E6	NC	VDD33	N/A
E7	NC	VSS33	N/A
E11	VCORE	VDD33	MT6227->Vcore ; MT6219-> VDD
E13	NC	VDD33	N/A
F6	NLD17	MPLL_OUT	N/A
F7	NC	DPLL_OUT	N/A
G6	NLD16	UPLL_OUT	N/A
M15	VDD33_MC	NC	Connect to VDD
R11	EWAIT	NC	N/A
J9	NLD8	N/A	Must add ball in MT6227 footprint
J10	NLD9	N/A	Must add ball in MT6227 footprint
J11	NLD10	N/A	Must add ball in MT6227 footprint
K9	NLD11	N/A	Must add ball in MT6227 footprint
K11	NLD12	N/A	Must add ball in MT6227 footprint
L9	NLD13	N/A	Must add ball in MT6227 footprint
L10	NLD14	N/A	Must add ball in MT6227 footprint
L11	NLD15	N/A	Must add ball in MT6227 footprint
M16	MCWP	MCPWRON	MT6227->MCWP ; MT6219->MCPWRON
M17	MCINS	MCWP	MT6227->MCINS ; MT6219->MCWP
M18	MCCK	MCINS	MT6227->MCCK ; MT6219->MCINS
N19	MCPWRON	MCCK	MT6227->MCPWRON ; MT6219->MCCK
E15	VDD33_IS	VDD33	

MT6227 : VOCRE is 1.8V, VRTC is 1.5V

MT6219 : VCORE is 1.2V, VRTC is 1.2V

MT6226/7 Compare to MT6219 (2/2)

Confidential **B** 機密

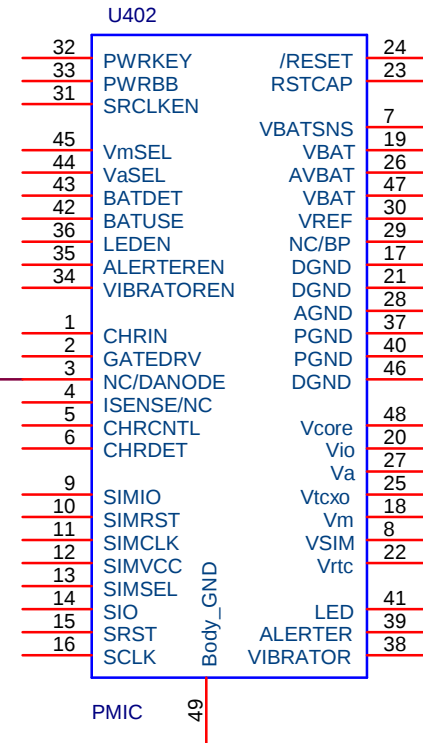


MT6226/7 Reference Design

For MT6226/7, PMIC **PIN 3** connects to VBAT
(pull high is better than floating)

MT6227: R449 NC
MT6219: R449 00HM

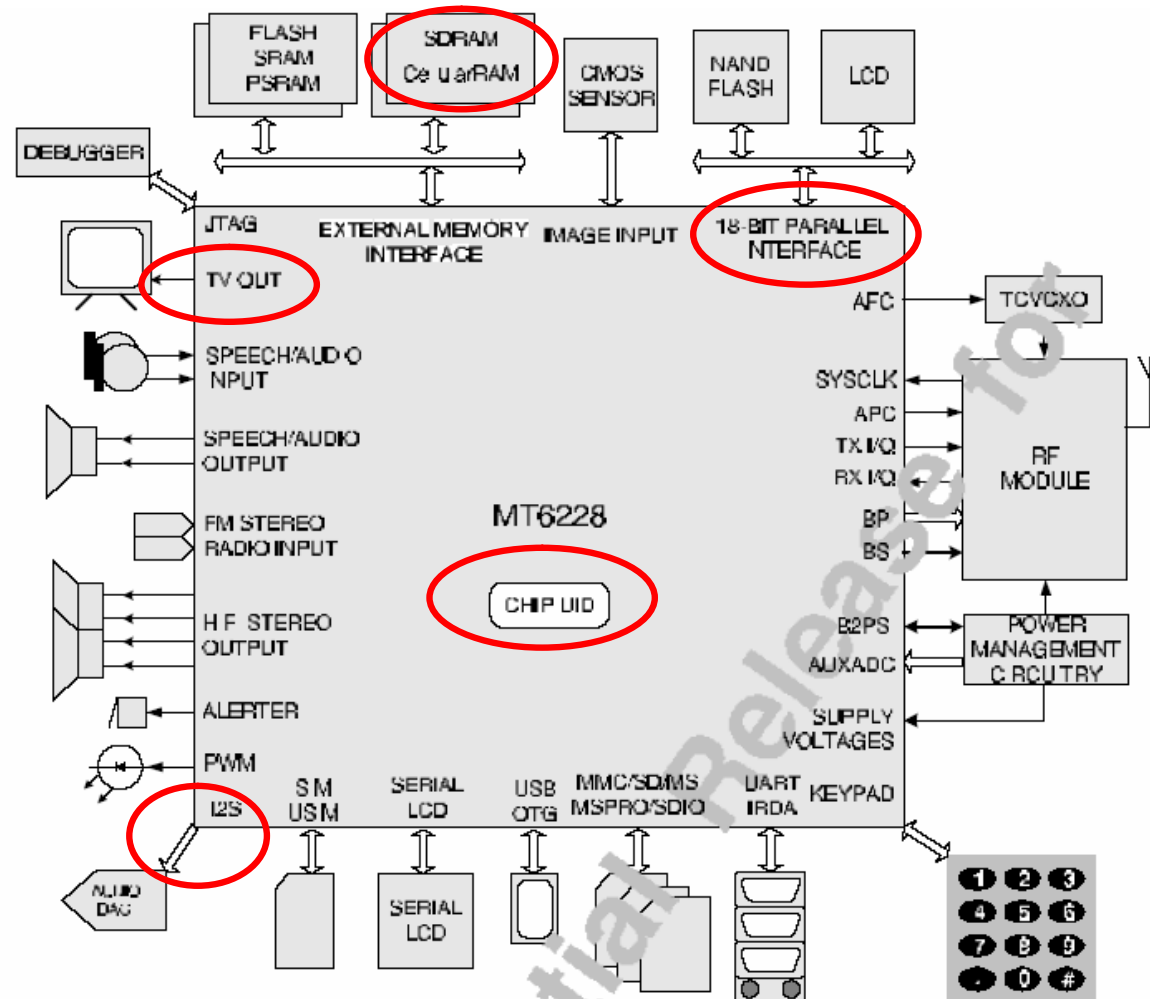
R449



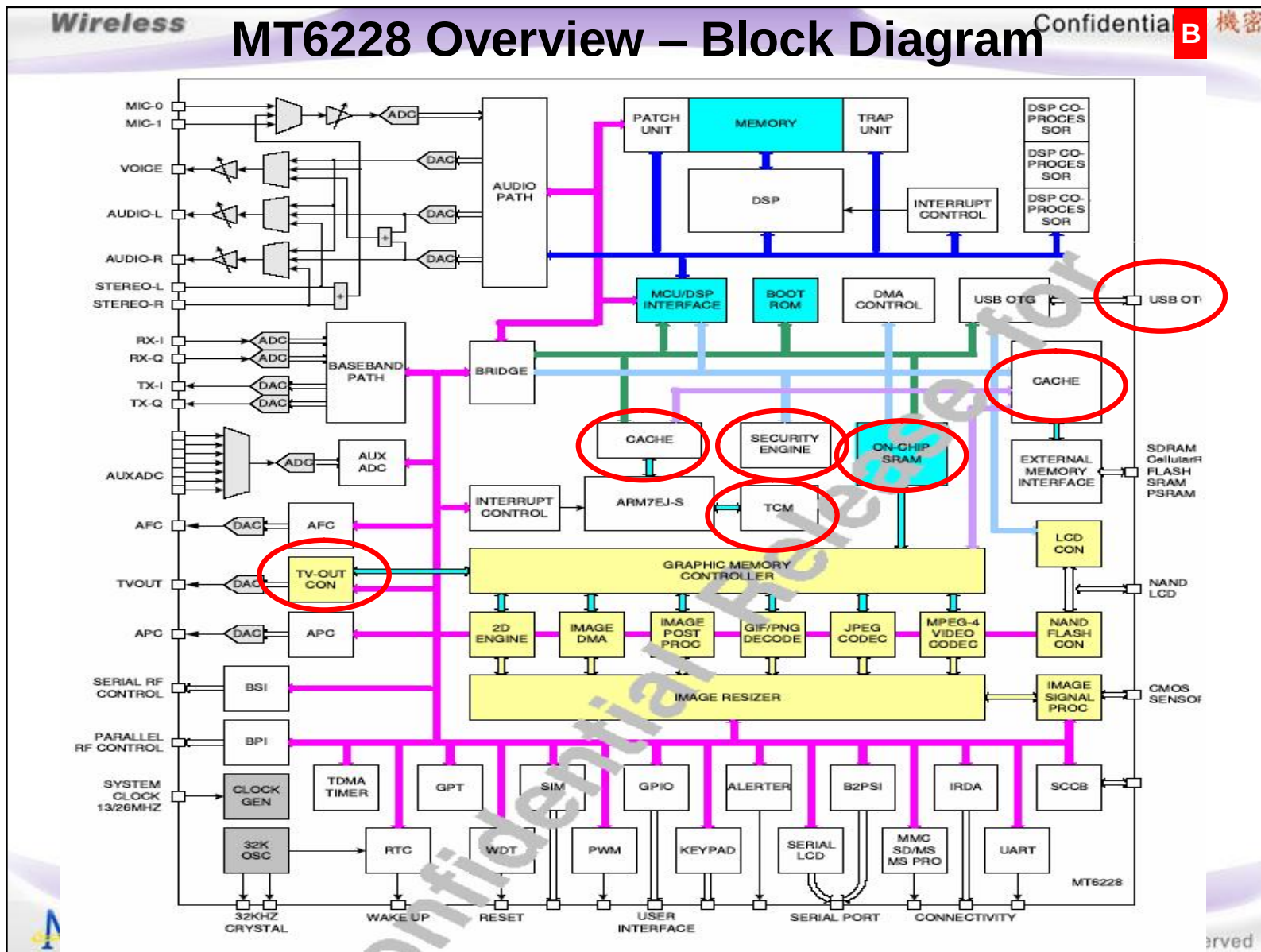
1 GPIO6_CMFLASH_EN >>

Flash Light control pin: its timing sync with the camera capture

MT6228 Overview – Typical Application



MT6228 Overview – Block Diagram



- **General**
- Integrated voice-band, audio-band and base-band analog front ends
- TFBGA 13mm×13mm, 314-ball, 0.65 mm pitch package
- **MCU Subsystem**
- ARM7EJ-S 32-bit RISC processor
- High performance multi-layer AMBA bus
- Java hardware acceleration for fast Java-based games and applets
- Operating frequency: 26/52/**104** MHz
- Dedicated DMA bus
- 14 DMA channels
- **1M bits** zero-wait-state on-chip SRAM
- **1M bits MCU dedicated Tightly Coupled memory (TCM) – High Performance**
- **256K bits CODE cache – High Performance**
- **64K bits DATA cache – High Performance**
- On-chip boot ROM for Factory Flash Programming
- Watchdog timer for system crash recovery
- **3** sets of General Purpose Timer
- Circuit Switch Data coprocessor
- Division coprocessor
- **PPP Framer coprocessor**

- **External Memory Interface**
- Supports up to 4 external devices
- Supports 8-bit or 16-bit memory components with maximum size of up to 64M Bytes each
- **Support Mobile RAM and Cellular RAM**
- Supports Flash and SRAM with Page Mode or Burst Mode
- Supports Pseudo SRAM
- Industry standard Parallel LCD Interface
- Supports multi-media companion chips with 8/16 bits data width
- Flexible I/O voltage of 1.8V ~ 2.8V for memory interface
- Configurable driving strength for memory interface
- **User Interfaces**
- 6-row × 7-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- SIM/USIM Controller with hardware T=0/T=1 protocol control
- Real Time Clock (RTC) operating with a separate power supply
- General Purpose I/Os (GPIOs)
- 2 Sets of Pulse Width Modulation (PWM) Output
- Alerter Output with Enhanced PWM or PDM
- 8 external interrupt lines (**EINT0~3**)

- **Connectivity**
- 3 UARTs with hardware flow control and speed up to 921600 bps
- IrDA modulator/demodulator with hardware framer supports SIR/**MIR/FIR** operating speeds
 - SIR: 9600~115200bps; MIR: 567000~1152000bps; FIR: 4Mbps
- Full-speed USB 1.1.
- Multi Media Card/Secure Digital Memory Card/Memory Stick/Memory Stick Pro host controller
- Support SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for Audio application
- **Security**
- **Cipher: support AES, DES/3DES**
- **Hash: support MD5, SHA-1**
- **Support security key and 27 bit chip unique ID**
- **Power Management**
- Power Down Mode for analog and digital circuits
- Processor Sleep Mode
- Pause Mode of 32KHz clocking at Standby State
- 7-channel Auxiliary 10-bit A/D Converter for charger and battery monitoring and photo sensing
- **Test and Debug**
- Built-in digital and analog loop back modes for both Audio and Baseband Front-End
- DAI port complying with GSM Rec.11.10
- JTAG port for debugging embedded MCU

- **Radio Interface and Baseband Front End**
- GMSK modulator with analog I and Q channel outputs
- 10-bit D/A Converter for uplink baseband I and Q signals
- 14-bit high resolution A/D Converter for downlink baseband I and Q signals
- Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
- 10-bit D/A Converter for Automatic Power Control
- 13-bit high resolution D/A Converter for Automatic Frequency Control
- Programmable Radio RX filter
- 2 Channels bi-directional Baseband Serial Interface (BSI) with 3-wire or 4-wire control
- 10-Pin Baseband Parallel Interface (BPI) with programmable driving strength
- Multi-band support

- Voice and Modem CODEC
- Dial tone generation
- Voice Memo
- Noise Reduction
- Echo Suppression / Echo Cancellation
- Advanced Sidetone Oscillation Reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1 and A5/2 ciphering
- GPRS GEA1 and GEA2 ciphering
- Programmable GSM/GPRS Modem
- Packet Switched Data with CS1/CS2/CS3/CS4 coding schemes
- GSM Circuit Switch Data
- GPRS Class 12

MT6228 Overview – MODEM Features

- Voice Interface and Voice Front End
- Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control (AGC) mechanism
- Voice power amplifier with programmable gain
- 2nd order Sigma-Delta A/D Converter for voice uplink path
- D/A Converter for voice downlink path
- Supports half-duplex hands-free operation
- Compliant with GSM 03.50

MT6228 Overview – Multi-Media Features

- LCD/NAND Flash Interface
- Dedicated Parallel Interface supports 3 external devices with 8/16 bit NAND flash interface, **8/9/16/18 bit Parallel interface**, and Serial interface for LCM
- Built-in NAND Flash Controller with 1-bit ECC correction for mass storages
- LCD Controller
- Hardware accelerated display
- Supports simultaneous connection to up to **3** parallel LCD and **2** serial LCD modules
- Supports LCD format: RGB332, RGB444, RGB565, RGB666, RGB888
- Supports LCD module with maximum resolution up to 800x600 at **24bpp**
- Per pixel alpha channel
- **True color engine**
- Supports hardware display rotation
- Capable of combining display memories with up to **6** blending layers
- **Accelerated Gamma correction with programmable gamma table.**

MT6228 Overview – Multi-Media Features

- **Image Signal Processor**
- 8/10 bit Bayer format image input
- Capable of processing image of size up to **3M** pixels
- Color Correction Matrix
- Gamma Correction
- Automatic Exposure (AE) Control
- Automatic White Balance (AWB) Control
- Programmable AE/AWB windows
- Edge Enhancement Support
- Histogram equalization logic
- Horizontal and vertical sync information on separate pins
- Shading compensation
- Defect Pixel compensation
- **Graphic Compression**
- GIF Decoder
- **PNG** Decoder

MT6228 Overview – Multi-Media Features

- **JPEG Decoder**
- ISO/IEC 10918-1 JPEG Baseline and Progressive modes
- Supports all possible YUV formats, including grayscale format
- Supports all DC/AC Huffman table parsing
- Supports all quantization table parsing
- Supports restart interval
- Supports SOS, DHT, DQT and DRI marker parsing
- IEEE Std 1180-1990 IDCT Standard Compliant
- Supports progressive image processing to minimize storage space requirement
- Supports reload-able DMA for VLD stream

- **JPEG Encoder**
- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 Compliance
- Supports YUV422 and YUV420 grayscale formats
- **Support JFIF (JPEG File Inter exchange Format)**
- Standard DC and AC Huffman tables
- Provides 14 levels of encode quality
- Support continuous shooting

MT6228 Overview – Multi-Media Features

- **Image Data Processing**
- Support Digital Zoom
- Supports RGB888/565, YUV444 image processing
- High throughput hardware scalar. Capable of tailoring an image to an arbitrary size
- Horizontal scaling in averaging method
- Vertical scaling in bilinear method
- **Simultaneous scaling for MPEG-4 encode and LCD display**
- YUV and RGB color space conversion
- Pixel format transform
- Boundary padding
- Pixel processing: hue/saturation/intensity/color adjustment, Gamma correction and grayscale/invert/sepia-tone effects
- Programmable Spatial Filtering: Linear filter, Non-linear filter and Multi-pass artistic effects
- Hardware accelerated image editing
- Photo frame capability
- RGB thumbnail data output

MT6228 Overview – Multi-Media Features

- **MPEG-4/H.263 CODEC**
- Hardware Video CODEC
- ISO/IEC 14496-2 simple profile:
- decode @ level 0/1/2/3
- encode @ level 0
- Supported visual tools for decoder: I-VOP, P-VOP, AC/DC prediction, 4-MV, Unrestricted MV, Error Resilience, Short Header
- Error Resilience for decoder: Slice Resynchronization, Data Partitioning, Reversible VLC
- Supported visual tools for encoder: I-VOP, P-VOP, Half-pel, DC prediction, Unrestricted MV, Reversible VLC, Short Header
- Supports encoding motion vector of range up to -64/+63.5 pixels
- ITU-T H.263 profile 0 @ level 10
- **Max decode speed is VGA@15fps**
- **Max encode speed is CIF@15fps**
- **Support VGA mode encoding**
- **Horizontal and vertical de-blocking filter in video playback**
- **Encoder resync marker and HEC**
- AAC/HE-AAC/AMR/WB-AMR audio decode support
- AMR/WB-AMR audio encode support

MT6228 Overview – Multi-Media Features

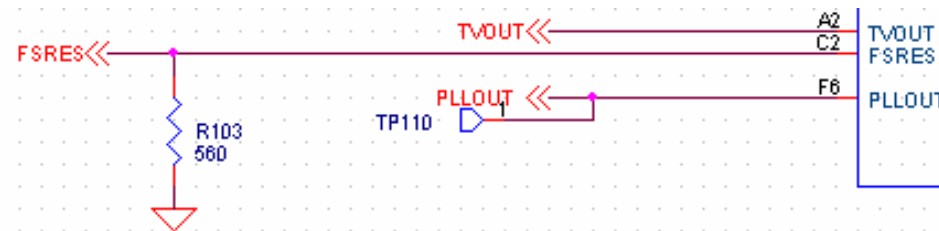
- **TV-OUT**
- Support NTSC/PAL formats (interlaced mode)
- 10 bit video DAC with 2x over-sampling
- Supports one composite video output

- **2D Accelerator**
- Support 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565, and 8-bpp index color modes
- Support SVG Tiny
- Rectangle gradient fill
- BitBlt: multi-BitBlt with 7 rotate, 16 binary ROP
- Alpha blending with 7 rotation
- Line drawing: normal line, dotted line, anti-aliasing
- Circle drawing
- Bezier curve drawing
- Triangle flat fill
- Font caching: normal font, Italic font
- Command queue with max depth 2047

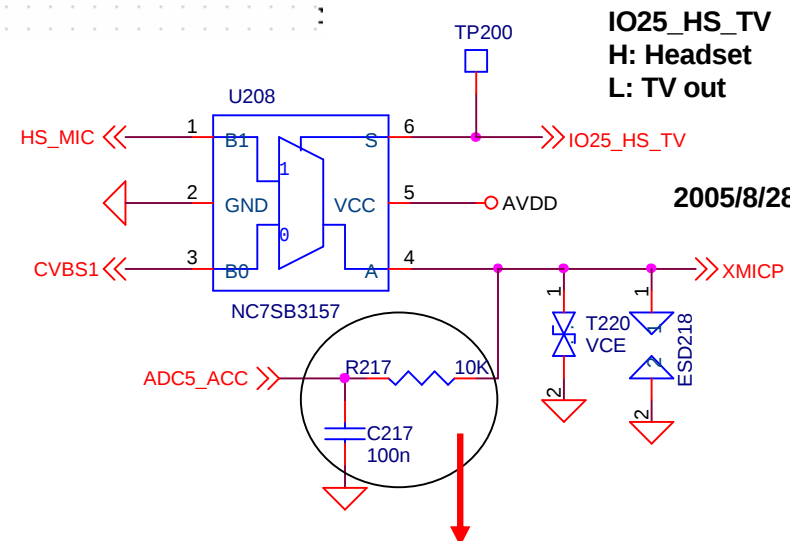
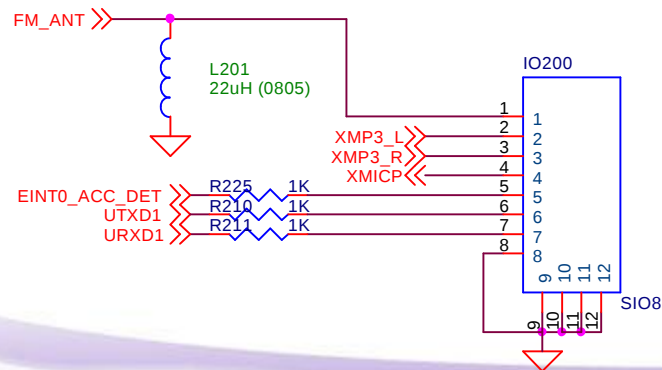
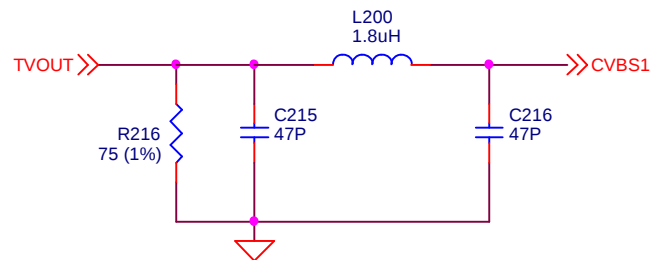
MT6228 Overview – Multi-Media Features

- **Audio CODEC**
 - Wavetable synthesis with up to 64 tones
 - Advanced wavetable synthesizer capable of generating simulated stereo
 - Wavetable including GM full set of 128 instruments and 47 sets of percussions
 - PCM Playback and Record
 - Digital Audio Playback
 - Support HE-AAC codec decode
 - Support AAC codec decode
- **Audio Interface and Audio Front End**
 - **Supports I2S interface**
 - High resolution D/A Converters for Stereo Audio playback
 - Stereo analog input for stereo audio source
 - Analog multiplexer for Stereo Audio
 - Stereo to Mono Conversion

MT6228 Reference Design



TV OUT VIEDO I/F



For TVOUT voltage detection

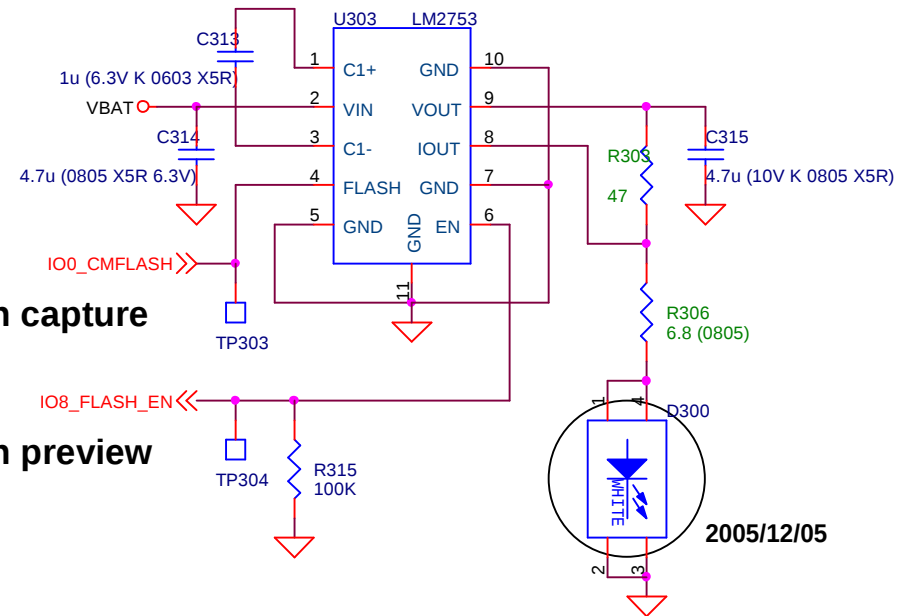
2005/8/28

MT6228 Reference Design

Flash Light

Step 2: Turn on Flash driver when capture

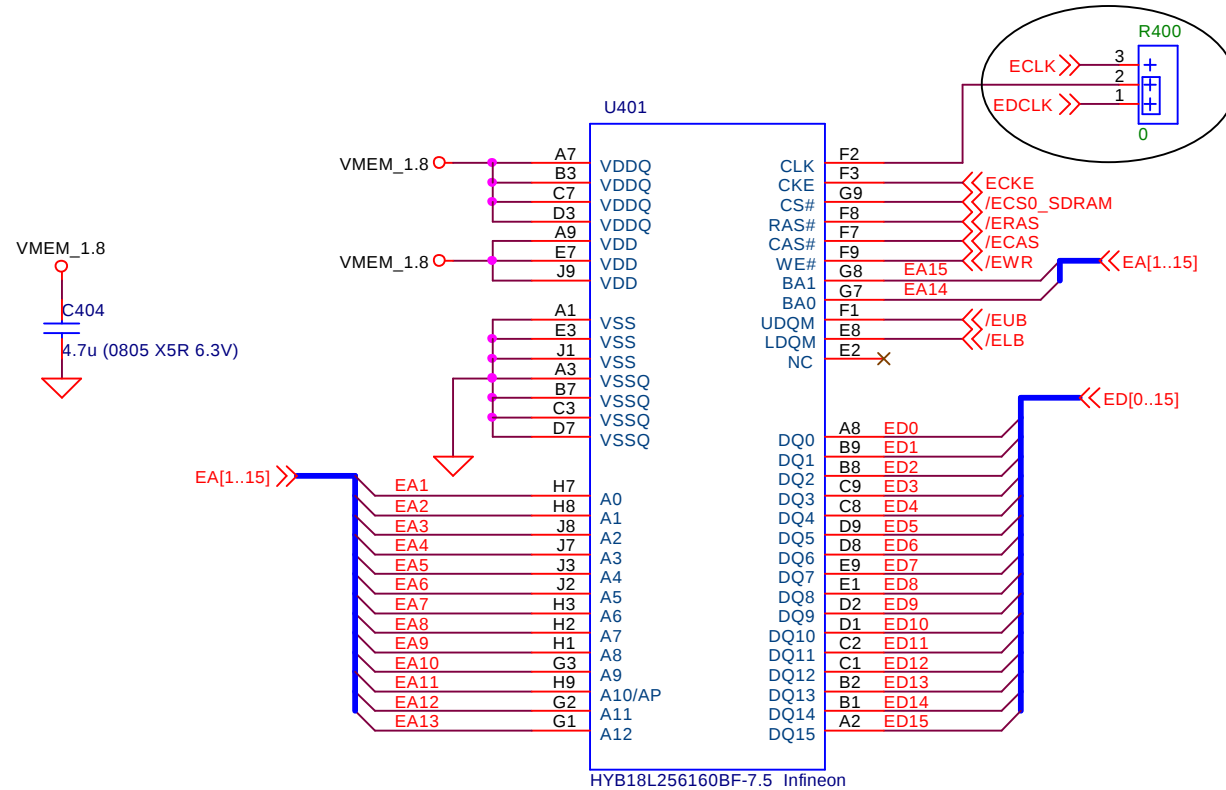
Step 1: Turn on Flash driver when preview



MT6228 Reference Design

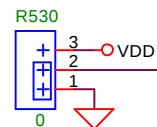
• SDRAM

2005/12/05

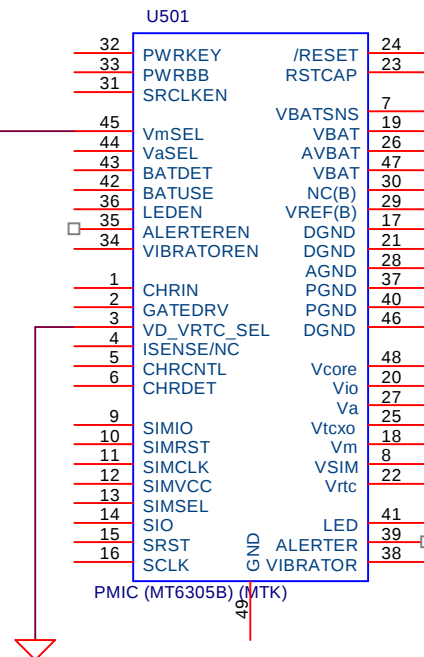


MT6228 Reference Design

VmSEL pin connect to GND
SDRAM power 1.8V



MT6228 VCORE and VRTC are 1.2V
PMIC pin3 (VD_VRTC_SEL) Low



Thank You!

MT6228 Micro-Controller Unit Subsystem

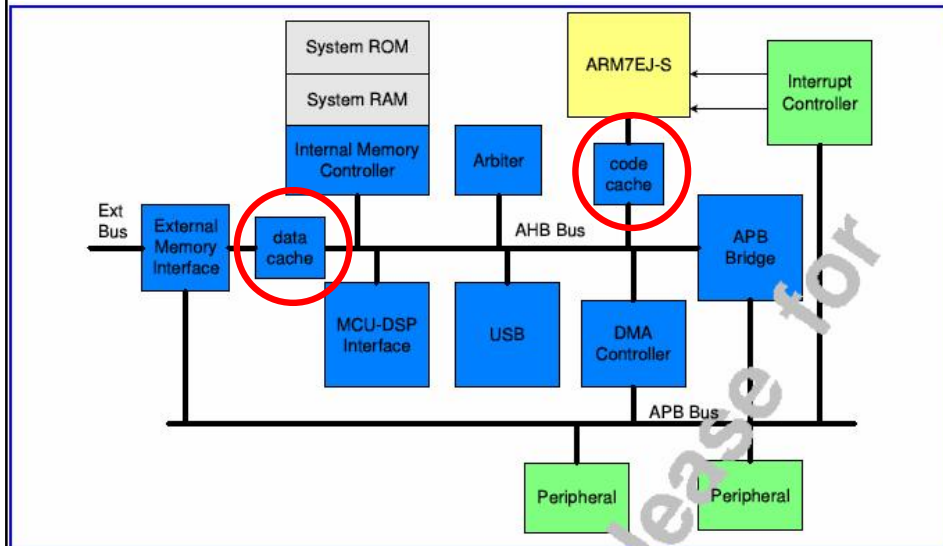
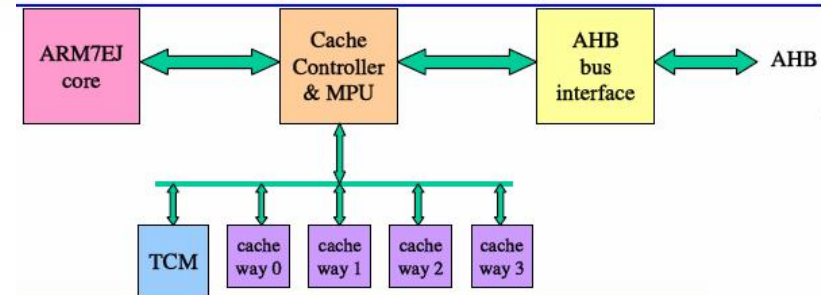


Figure 5 Block Diagram of the Micro-Controller Unit Subsystem in MT6228



- All processor transactions go to code cache first.
- If the requested content is found in TCM or in cache, no bus transaction is required
- If the code cache hit rate is high enough, bus traffic and MCU can be effectively.

MT6228 Boot Sequence

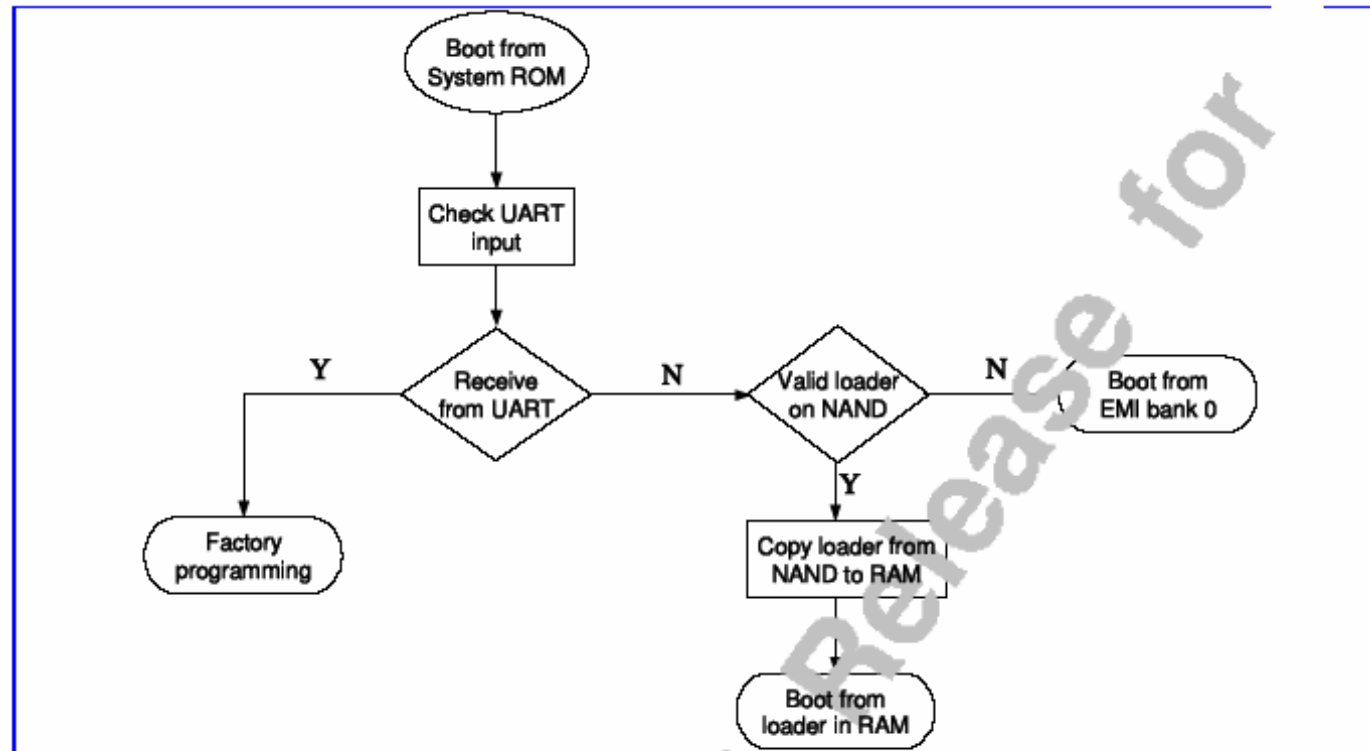


Figure 8 Boot sequence

- Memory Re-mapping Mechanism
- NAND Booting sequence

MT6228 TVOUT

- Support **NTSC/PAL** interlaced TV format.
- It includes two components: a TV controller and a TV encoder.

TV controller:

1. Fetch the TV frame buffer.

- In video playback mode: the source is from the video codec buffer in YUV420 format.
- In image playback mode: the source is in RGB565 format. Still images can be displayed.

2. Scale the frame size to fit the TV size.

- In **NTSC** mode, the ideal display area is **720(W)x480(H)**. Field update rate is **59.94** frames per second (fps).
- In **PAL** mode, the idea display area is **720(W)x576(H)**. Field update rate is **50** fps.
- The controller support an arbitrary image size up to 640 pixels in height and 480 pixels in width.

TV encoder:

- It receives a YCbCr stream from the video scaler and encodes the stream into NTSC/PAL signal.

MT6228 TVOUT

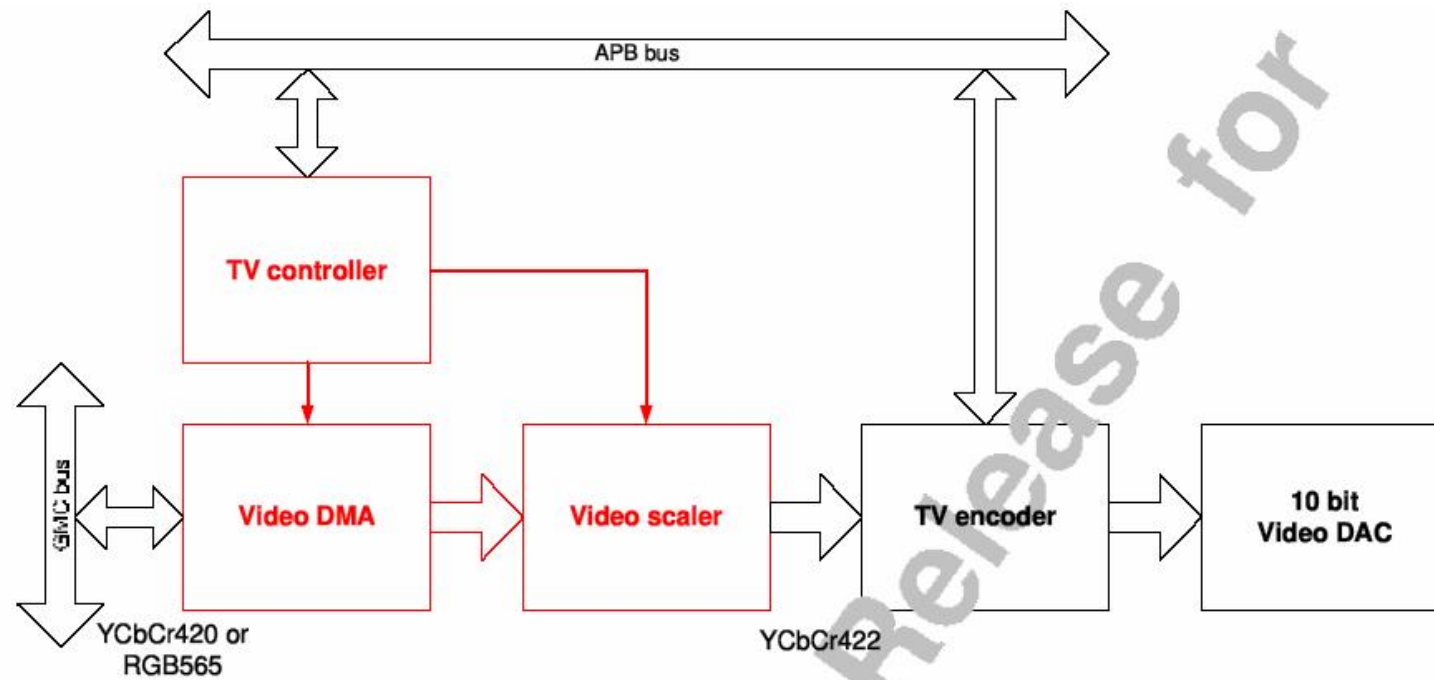


Figure 36 Block Diagram of the TV Encoder

MT6228 DAI, PCM and EDI Pin Sharing

- Beside the shared pins, the EDI interface can also use other dedicated pins. With the dedicated pin (**GPIO4,5,6**), PCM and EDI interfaced can operate at the same time.

PIN NAME	DAI	PCM	EDI
DAI_CLK (OUTPUT)	DAI_CLK	PCM_CLK	EDI_CLK
DAI_TX (OUTPUT)	DAI_TX	PCM_OUT	EDI_DAT
DAI_RX (INPUT)	DAI_RX	PCM_IN	
BT_SYNC (OUTPUT)	-	PCM_SYNC	EDI_WS

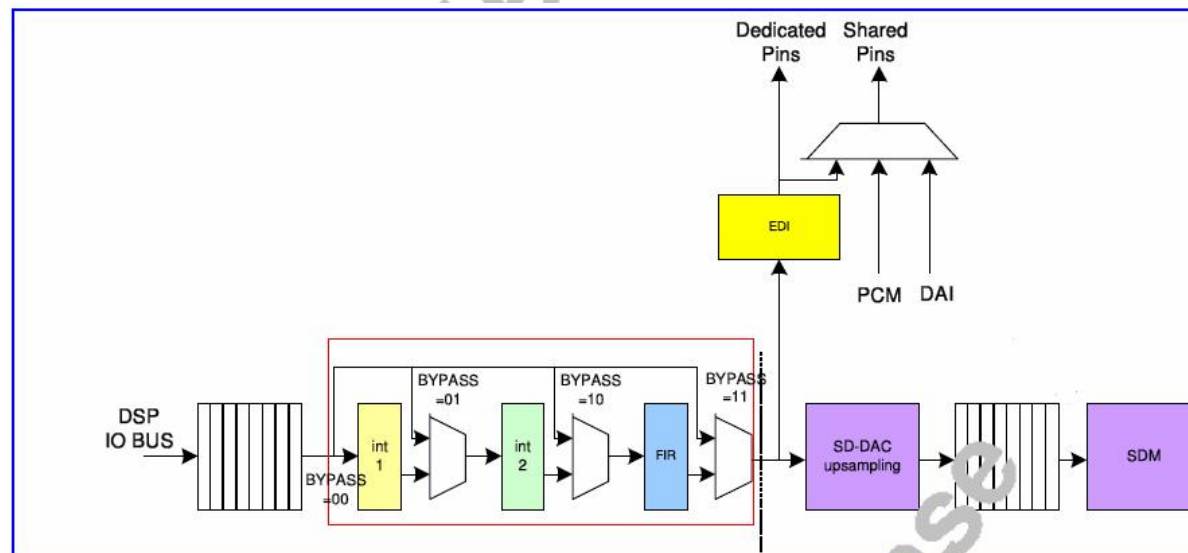


Figure 43 DAI, PCM, EDI interfaces

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