SN74LV8153
SERIAL-TO-PARALLEL INTERFACE

SCLS555 – JUNE 2004

DESCRIPTION

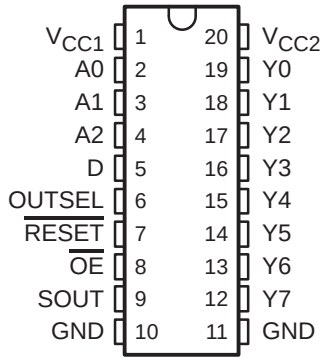
The SN74LV8153 is a serial-to-parallel data converter. It accepts serial input data and outputs 8-bit parallel data.

The automatic data-rate detection feature of the SN74LV8153 eliminates the need for an external oscillator and helps with cost and board real-estate savings.

The OUTSEL pin is used to choose between open collector and push-pull outputs. The open-collector option is suitable when this device is used in applications such as LED interface, where high drive current is required. SOUT is the output that acknowledges reception of the serial data.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC1} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

N OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS				OUTPUT Yn	OUTPUT STRUCTURE
OUTSEL	$\overline{RESET}$	$\overline{OE}$	Dn		
L	H	L	H	L	Open collector
L	H	L	L	H	
L	X	H	X	H	
L	L	X	X	H	
H	H	L	H	H	Push-pull
H	H	L	L	L	
H	X	H	X	Z	
H	L	L	X	L	

In the open-collector mode (OUTSEL = L), the outputs are inverted, e.g., Y1 = l, when D1 = H

FEATURES

- **Single-Wire Serial Data Input**
- **Compatible With UART Serial-Data Format**
- **Up to Eight Devices (64-Bit Parallel) Can Share the Same Bus by Using Different Combinations of A0, A1, A2**
- **Up to 40 mA Current Drive in Open-Collector Mode for Driving LEDs**
- **Outputs Can be Configured as Open-Collector or Push-Pull**
- **Internal Oscillator and Counter for Automatic Data-Rate Detection**
- **Output Levels Are Referenced to V_{CC2} and Can Be Configured From 3 V to 12 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

SUMMARY OF RECOMMENDED OPERATING CONDITIONS

PARAMETER	
V_{CC1}	3 V to 5.5 V
V_{CC2}	3 V to 13.2 V
I_{OL}	40 mA @ V_{CC2} = 4.5 V (open-collector mode)
I_{OH}	−24 mA @ V_{CC2} = 12 V (push-pull mode)
Maximum Data Rate	24 Kbps

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube	SN74LV8153N	SN74LV8153N
	TSSOP − PW	Tube	SN74LV8153PW	LV8153
		Tape and reel	SN74LV8153PWR	

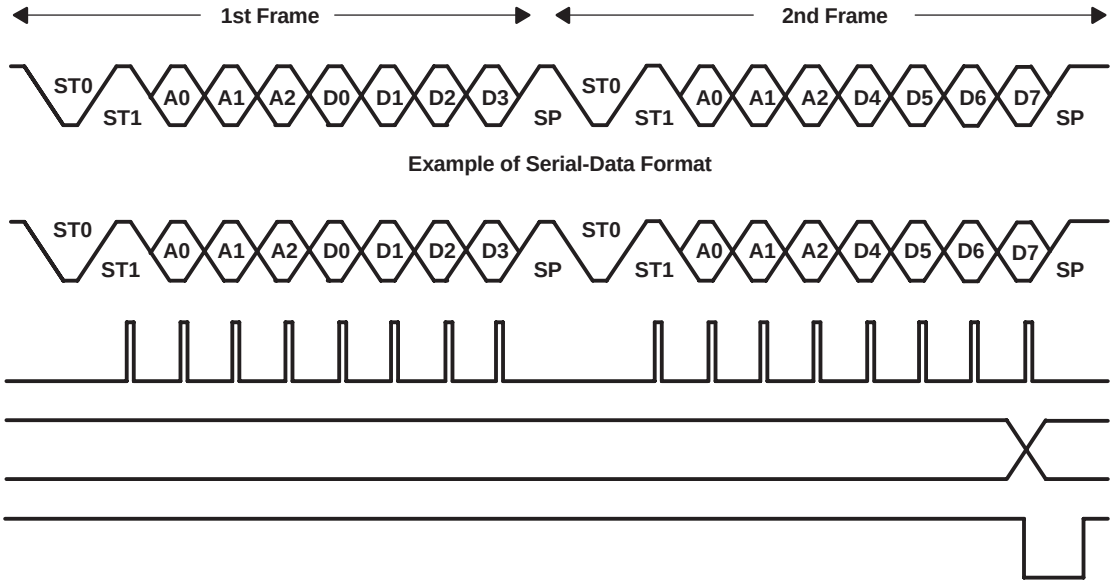
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PIN DESCRIPTION

PIN #	PIN NAME	I/O	PIN FUNCTION
1	V_{CC1}		Power-supply pin (all inputs and outputs except for Y0-Y7)
2-4	A0, A1, A2	In	The address pins are used to program the address of the device and allow up to eight devices to share the same bus.
5	D	In	Serial data input
6	OUTSEL	In	Choose between open-collector and push-pull type outputs (Y0-Y7).
7	$\overline{\text{RESET}}$	In	Initialize register status
8	$\overline{\text{OE}}$	In	Force Y0-Y7 to Hi-Z
9	SOUT	Out	Outputs a pulse when latch data is changed. Supplied by V_{CC1}.
12-19	Y0-Y7	Out	Push-pull or open collector parallel data outputs. Supplied by V_{CC2}.
20	V_{CC2}		Power-supply pin for outputs (Y0-Y7). V_{CC2} can range from 3 V to 13.2 V.

data transmission protocol

- The serial data should be sent as 2START-3ADDRESS-4DATA-1STOP. Two consecutive serial-data frames transmit 8 bits of data. The first frame includes the lower four bits of data (D0-D3), and the second frame includes the upper four bits (D4-D7).
- The three address bits (in the consecutive frame) must be the same as those in the first frame; otherwise, the data will be dropped.
- The order of the two start bits must be 0, then 1 in any frame; otherwise, the data rate will not be detected correctly. The period between the falling edge of the first start bit (ST0) and the rising edge of the second start bit (ST1) is measured to generate an internal-clock synchronized data stream.

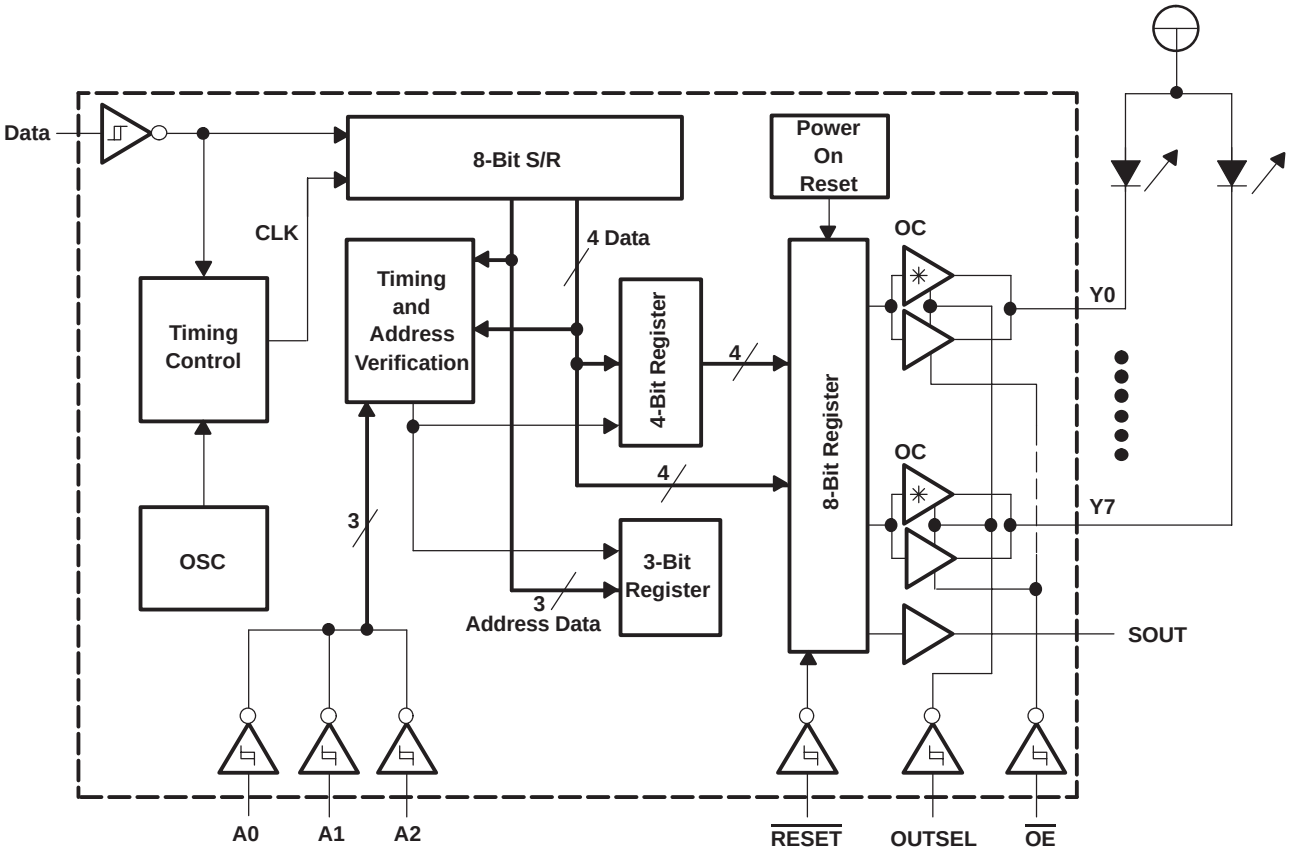


Example of Serial-Data Format

Timing Chart

(1) Internal clock cannot be observed.
(2) D0 is LSB and D7 is MSB. The data stream should be LSB first.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)(1)

Supply voltage range, V_{CC1} . . . . . −0.5 V to 7 V
Supply voltage range, V_{CC2} . . . . . −0.5 V to 14.5 V
Input voltage range, V_I(2) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or low state, V_O (SOUT)(2)(3) . . . . −0.5 V to V_{CC1} + 0.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (SOUT)(2) . . . . . −0.5 V to 7 V
Voltage range, applied to any output in the high or low state, V_O (Y0-Y7)(2)(3) . . . . −0.5 V to V_{CC2} + 0.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (Y0-Y7)(2) . . . . . −0.5 V to 14.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . 25 mA
Continuous current, I_O (OUTSEL = L, Y0-Y7 = L) . . . . . 60 mA
Package thermal impedance, θ_{JA}(4): N package . . . . . 69°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(1)The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(2)The value of V_{CC} is provided in the recommended operating operating condition table.
(3)The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions(1)

				V_{CC1}	V_{CC2}	MIN	MAX	UNIT
V_{CC1}	Supply voltage					3	5.5	V
V_{CC2}	Supply voltage					3	13.2	V
V_{IH}	High-level input voltage			3 V	3 V	$V_{CC} \times 0.7$		V
				4.5 V	4.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage			3 V	3 V		$V_{CC} \times 0.3$	V
				4.5 V	4.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage					0	5.5	V
V_O	Output voltage			4.5 V	4.5 V	0	5.5	V
					12 V	0	13.2	
I_{OH}	High-level output current	Yn	OUTSEL = H	3 V	3 V		−2	mA
				4.5 V	4.5 V		−8	
				4.5 V	12 V		−24	
		SOUT		3 V	3 V		−4	mA
				4.5 V	4.5 V		−8	
I_{OL}	Low-level output current	Yn	OUTSEL = H	3 V	3 V		2	mA
				4.5 V	4.5 V		8	
			OUTSEL = L	3 V	3 V		20	
				4.5 V	4.5 V		40	
		SOUT		3 V	3 V		4	
				4.5 V	4.5 V		8	
T_A	Operating free-air temperature					−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC1}	V_{CC2}	MIN	TYP	MAX	UNIT
V_{T+} Positive-going input threshold voltage		All inputs		3.3 V	3.3 V			2.31	V
				5 V	5 V			3.5	
V_{T-} Negative-going input threshold voltage		All inputs		3.3 V	3.3 V	0.99			V
				5 V	5 V	1.5			
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		All inputs		3.3 V	3.3 V	0.33		1.32	V
				5 V	5 V	0.5		2	
V_{OH}	Yn	I_{OH} = −2 mA		3 V	3 V	2.38			V
		I_{OH} = −8 mA		4.5 V	4.5 V	3.8			
		I_{OH} = −24 mA		4.5 V	12 V	11			
	SOUT	I_{OH} = −4 mA		3 V	3 V	2.38			
		I_{OH} = −8 mA		4.5 V	4.5 V	3.8			
V_{OL}	Yn	I_{OL} = 2 mA (OUTSEL = H)		3 V	3 V			0.44	V
		I_{OL} = 8 mA (OUTSEL = H)		4.5 V	4.5 V			0.44	
		I_{OL} = 40 mA (OUTSEL = L)		4.5 V	4.5 V			0.5	
	SOUT	I_{OL} = 4 mA		3 V	3 V			0.44	
		I_{OL} = 8 mA		4.5 V	4.5 V			0.44	
I_I		V_I = 5.5 V or GND		0 to 5.5 V				±1	µA
I_{OZ}		$V_O = V_{CC}$ or GND (OUTSEL = H)		5.5 V	5.5 V			±5	µA
I_{OH}		V_O = 12 V (OUTSEL = L)		5.5 V	5.5 V			5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	OUTSEL = H	5.5 V	5.5 V			5	mA
			OUTSEL = L					20	
I_{off} (except SOUT)		V_I or V_O = 0 to 5.5 V, V_{CC} = 0		0	0			±50	µA
C_i		$V_I = V_{CC}$ or GND		5 V	5 V		5		pF

switching characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	D7	Y	C_L = 50 pF		Pw/2	(1)			ns
	D7	SOUT			Pw/2	(1)			
	$\overline{RESET}$	Y						200	
	$\overline{OE}$(2)	Y						200	
t_{en}	$\overline{OE}$(3)	Y						200	ns
t_{dis}	$\overline{OE}$(3)	Y						200	ns
t_w		SOUT			Pw	(4)			ns
Data rate							2	24	Kbps

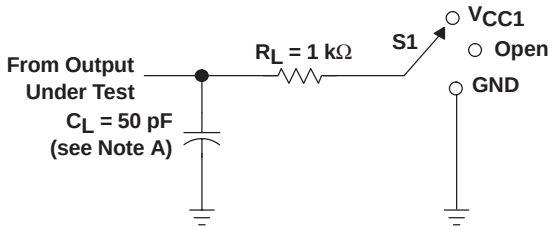
(1) The t_{pd} is dependent on the data pulse width (Pw), and Y outputs are changed after one-half of Pw, because the internal clock is synchronized at the middle of the data pulse. Not tested, but specified by design.
(2) When outputs are open collector (OUTSEL = L)
(3) When outputs are push-pull (OUTSEL = H)
(4) SOUT goes low when the data is received correctly and maintains a low level for one data-pulse period. Not tested, but specified by design.

switching characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	D7	Y	$C_L = 50\ pF$		Pw/2	(1)			ns
	D7	SOUT			Pw/2	(1)			
	$\overline{RESET}$	Y						150	
	$\overline{OE}$(2)	Y						150	
t_{en}	$\overline{OE}$(3)	Y						150	ns
t_{dis}	$\overline{OE}$(3)	Y						150	ns
t_w		SOUT			Pw	(4)			ns
Data rate							2	24	Kbps

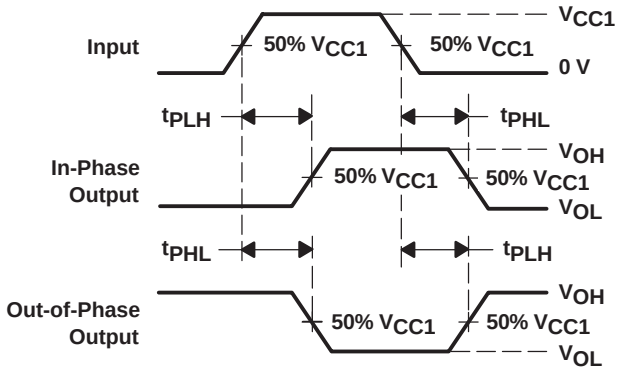
(1) The t_{pd} is dependent on the data pulse width (Pw), and Y outputs are changed after one-half of Pw, because the internal clock is synchronized at the middle of the data pulse. Not tested, but specified by design.
(2) When outputs are open collector (OUTSEL = L)
(3) When outputs are push-pull (OUTSEL = H)
(4) SOUT goes low when the data is received correctly and maintains a low level for one data-pulse period. Not tested, but specified by design.

PARAMETER MEASUREMENT INFORMATION
(PUSH-PULL OUTPUT)

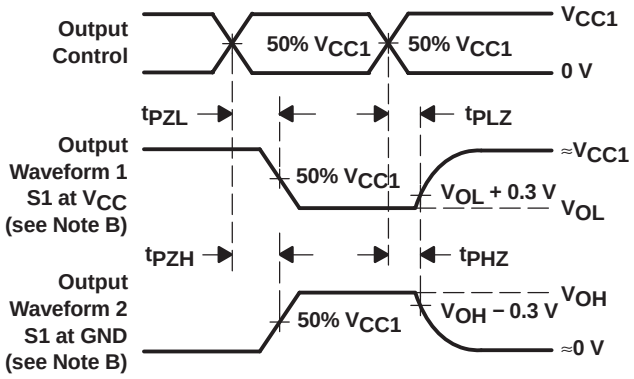


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC1}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

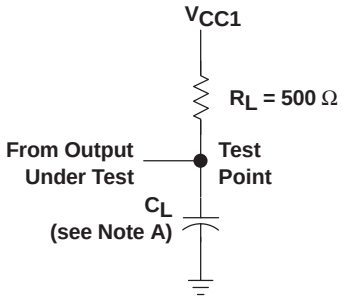


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

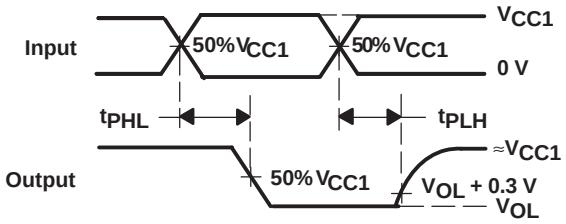
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: Z_O = 50 Ω, $t_r \le 3$ ns, $t_f \le 3$ ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
(OPEN-COLLECTOR OUTPUT)



LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤
C. The outputs are measured one at a time, with one input transition per measurement.
D. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LV8153N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV8153NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV8153PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

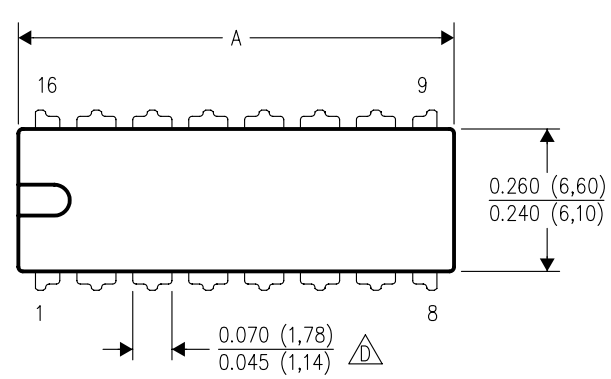
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

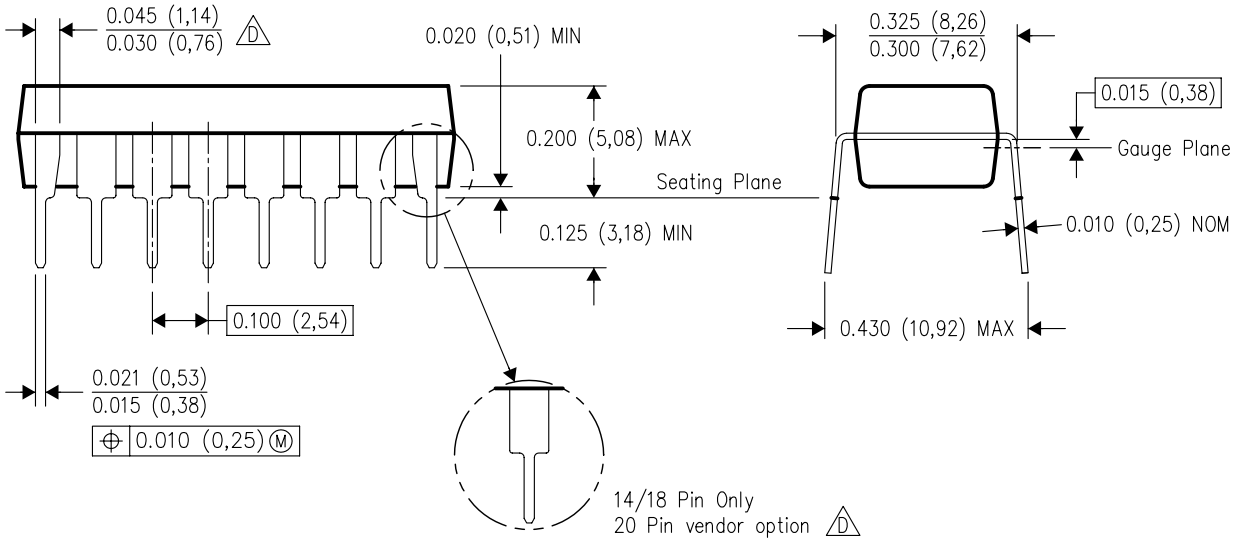
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

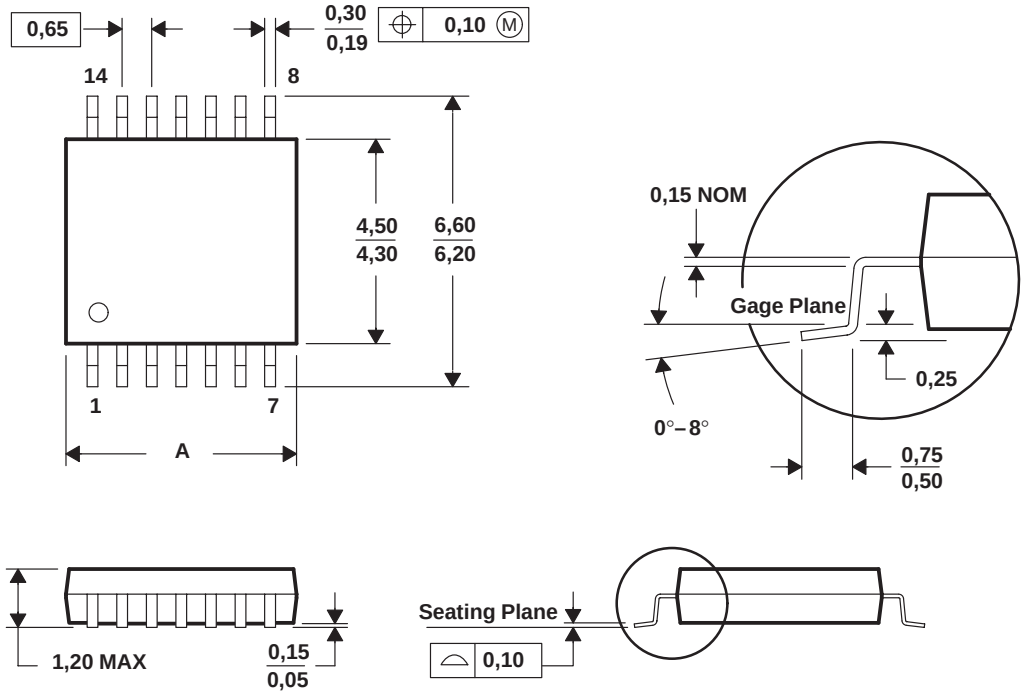


4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

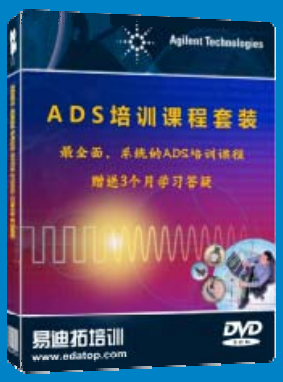
易迪拓培训课程列表：http://www.edatop.com/peixun/rfe/129.html

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

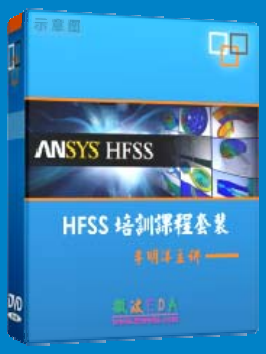
课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装



该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html



HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com