

Technical Note

Oscillation Circuit Design Guide

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SEIKO EPSON CORP.

QD Division Technical Support

NKTN-OCDG-IC RB

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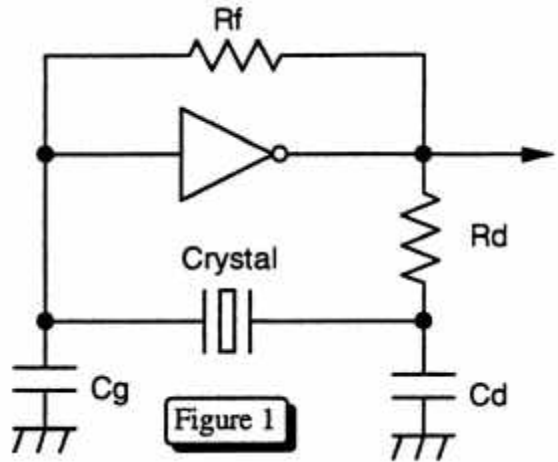
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1. Purpose and Scope

SEIKO EPSON CORP. offers an oscillation circuit evaluation service. If you can provide a few circuit boards, we will evaluate the circuit parameters and characteristics. Then we will give you the recommended parameters. However, sometimes some customers cannot give us the boards. In this case, circuit evaluation will have to be done by the customer. This guide is a reference for customers when designing and/or evaluating circuits. Basically, the crystal oscillation circuit is constructed as in Figure 1. The circuit parameters depend on the many characteristics including the specification of the IC and the oscillation frequency. In order to find the best parameters, please measure the actual circuit. This document explains the procedure and technique for circuit evaluation.



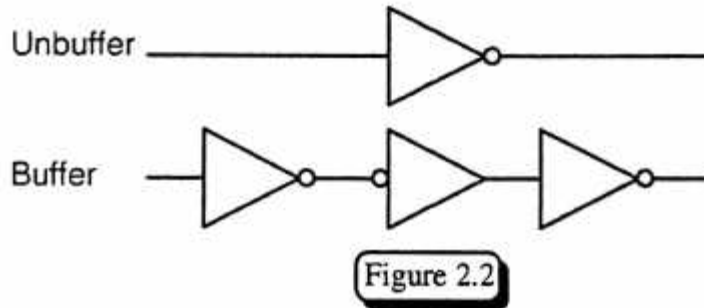
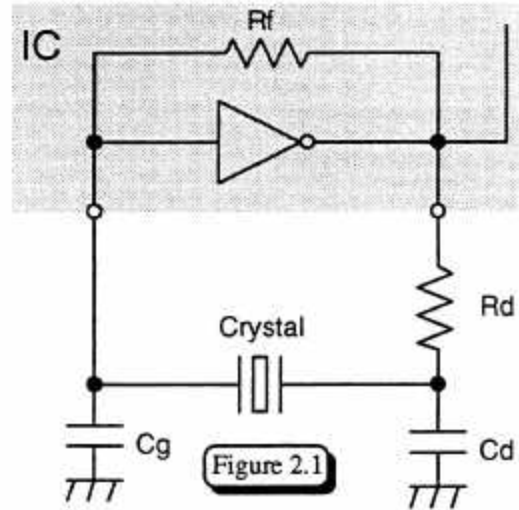
2. Methods for improving design

There are many techniques for designing good oscillation circuit. This section outlines some techniques.

2.1. Confirmation of the oscillation circuit and construction of the IC

It is necessary to confirm the IC construction before starting to design the oscillation circuit. When using a regular HC - MOS (High speed C - MOS) inverter gate such as the 74HCU04 the circuit will need all external parts. However, if the IC has built in resistors and/or capacitors, it is only necessary to add those parts not contained in the IC. (see Figure 2.1)

In addition to choosing an inverter gate, the gate must be the UNBUFFERED type. Please see Figure 2.2. The unbuffered type inverter is constructed of only one inverter, on the other hand, the buffer type has three inverter in a gate inside it although it is referred to by only one symbol.



The buffer inverter makes a reverse phase three times internally, therefore the output waveform will have some distortion. Also, the buffer has more gain than the unbuffer, causing a higher drive level.

2.2. Determining the preliminary values

There is no general value for the oscillation circuit because the value must be changed due to the IC characteristics, printed pattern layout, oscillation frequency, etc. In the case of a regular inverter, such as the TC74HCU04P, the following parameters will generally assure suitable operation. If the IC has some built-in device, please choose each parameter close to the following values:

Preliminary Parameters	Rf [MW]	Rd[kW]	Cg [pF]	Cd[pF]
20 to 60 [KHz]	20	500	10	10
60 to 165 [KHz]	10	300	10	10
5.5 to 24 [MHz]	1	0.5	10	10

A more exact value will be found with actual data from the circuit evaluation.

2.3. Useful board design for the evaluation

There are some parts positions that are useful for the evaluation even for parts that will not be used. Figure 2.3 shows five (5) positions A, B, C, D1 and D2 which will be used for additional devices during the evaluation. The following explains the purpose of these positions:

- A: Used for putting a resistor in series with the crystal. With this, measurement of oscillation allowance will be easy.
- B: Used for putting a resistor in series to increase Rf if the device has a built - in Rf
- C: Used for putting a resistor in series to increase Rd if the device has a built - in Rd.
- D1, D2: Used for putting capacitors in parallel to increase Cg and Cd if the device has them.

The printed patterns for these are shown bellow the circuit. For A, B and C the line should continue through and will be cut when the resistors are added.

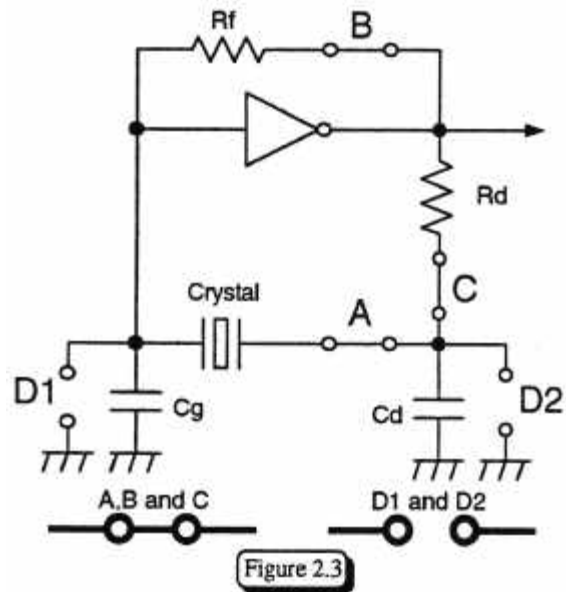


Figure 2.3

2.4. Characteristics of each parameter of the oscillation circuit

The circuit parameters which referred to Figure 1 have the characteristics as follows:

- Rf: Used for a bias for the inverter closed loop. If the value is small, it will cause an overtone oscillation due to the small phase difference between the inverter input and output.
- Ri: Used to bias the crystal. Generally, a small Rd will cause a high drive level. Cg, Cd: It is a basic part of the closed loop on the crystal side. Generally, a large capacitance will cause a high drive level. Please try to keep the same value for Cg and Cd. This is ideal for stable operation.

3. Circuit evaluation

The results of the circuit evaluation will decide the circuit parameters and characteristics for suitable operation.

3.1. Deciding the best parameters

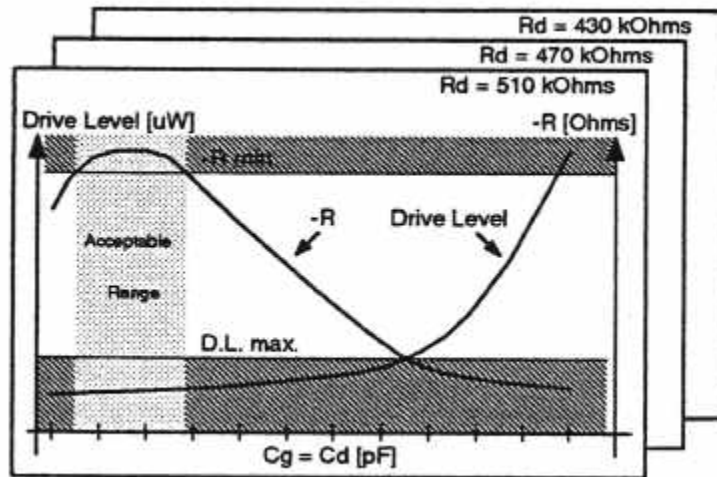
To decide the best parameters, please use the following guidelines:

- i. Drive Level: Must be below 1μW (20kHz to 165kHz)
Must be below 300μW. 100μW Typ. (5.5MHz to 24MHz)
- ii. Oscillation Allowance: At least 5 times CL maximum value
(Negative Resistance) (ex., if the crystal is C - 002RX, in this case at least -250kΩ)
In the case when CL is low, the required oscillation allowance is at least twice Re*1 (Effective Resistance). Three (3) times Re is recommended.
Re*1 : The Re (Effective Resistance) can be calculated by the following formula:

$$Re = R_1 \left[1 + \frac{C_0}{C_L} \right]^2 [\Omega]$$

- iii. Oscillation start up voltage: It must start up with in 2.5V if the Vdd=5.0V.
- iv. Oscillation start up time: Within 3 seconds (20kHz to 165kHz)
(General standard value) Within 4m seconds (5.5MHz to 24MHz)
- v. Oscillation frequency: The value must be matched to the intended circuit frequency.

The characteristics iii., iv. and v. can be measured while checking i. and ii. So, to decide the parameter's accuracy always use i. (drive level) and ii. (oscillation allowance). Using graphed data will help for confirmation of characteristics. Use drive level and oscillation allowance as Y axes, Cg and Cd as X axis. According to the graph, there is a range of suitable characteristics. Please choose a common value of capacitance for the parts within the acceptable range.



3.2. Deciding the CL value

CL means Load Capacitance; that is the capacitance of the circuit (the capacitance of a circuit between the two terminals of a crystal). The CL is specified by the circuit. Please do not specify the values that may cause a shift in frequency. The relationship between CL and frequency is shown in Figure 3.1: When the CL required is 'a' pF, the crystal will oscillate within a fine tolerance under an 'a'pF CL circuit. If the actual CL is low, the frequency will be high and if the CL is high, the frequency will be low. Therefore in order to get an accurate frequency, the CL value for the crystal device and circuit must match.

Again, the CL value of the Crystal device means 'a crystal for a XXpF CL circuit'. It is as important as the frequency. However it is impossible to measure the actual CL.

Therefore, an approximate value is calculated using the following formula:

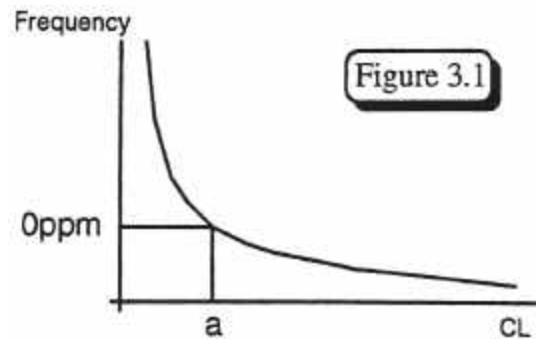
$$C_L @ \frac{C_G \cdot C_D}{C_G + C_D} + C_s [pF]$$

The Cs (Stray Capacitance) is usually 2pF if the board is a dual surface board. If using a multi-layer board, the value will be higher. For example, if both Cg and Cd are 10pF, the CL will be 7pF, as the Cs is 2pF.

Next, confirm the CL accuracy using a crystal with a Known CL. If there is still a difference in frequency, there are the following ways to correct it:

- i. Change Cg and Cd
- ii. Use a different CL crystal

Please evaluate all the parameters if the circuit board has been modified. The value usually changes even if the circuit is the same. We recommend that the easiest way to confirm the values, is to confirm the actual oscillation frequency with SEIKO EPSON's sample parts which have data attached.



4. Measurement procedure

4.1. Measurement of the Drive Level

The procedure of measuring the drive level is to measure the current which runs through the crystal. Then calculate with Ohm's formula as follows:

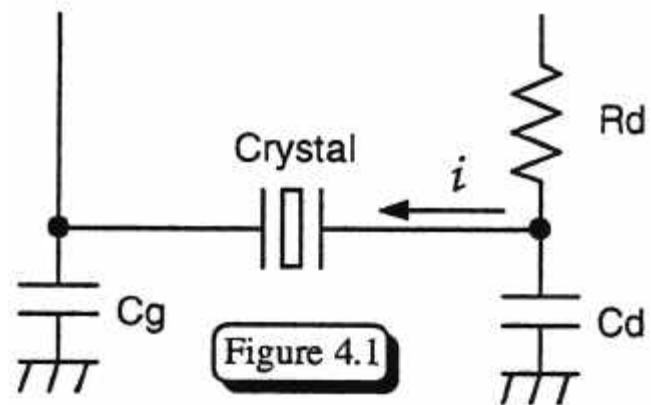
$$P(D.L.) = i^2 R [W]$$

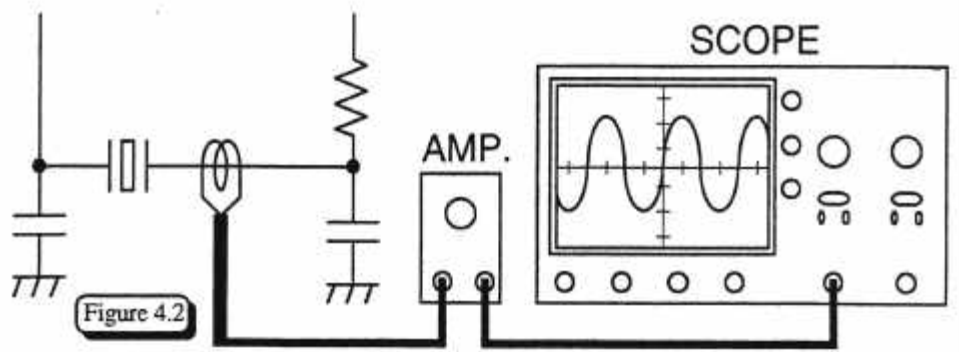
'i' must be the actual value and 'R' must be the specified CI maximum. The way to measure 'i' is different for AT crystals and Tuning fork crystals.

4.1.1. Measurement of the Drive Level for AT crystals

In order to measure the current as accurately as possible, use a current probe and an oscilloscope.

The current probe is similar to the CT (Current Transformer) which measures a current that runs through a lead using a magnetic flux according to the right screw rule. The signal goes to the oscilloscope via an amplifier. The current can be read from the scope.



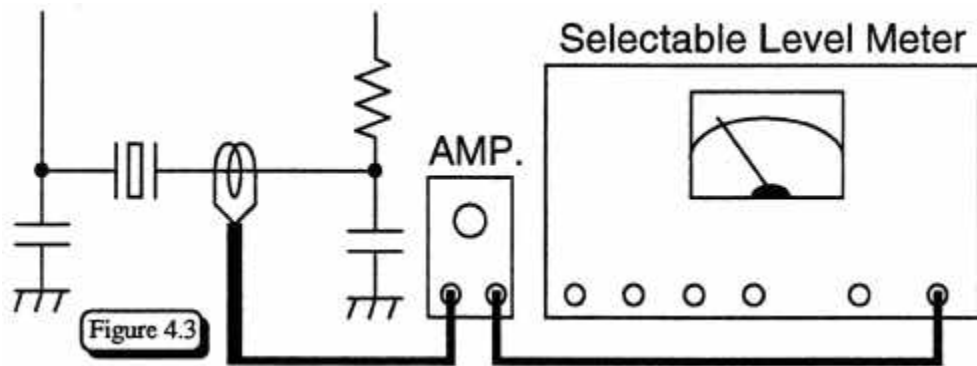


Read the current value from peak to peak, then calculate the effective value using the following formula:

$$i = \frac{i_{p-p}}{2\sqrt{2}} \text{ [A]}$$

4.1.2. Measurement of the Drive Level for Tuning Fork crystals

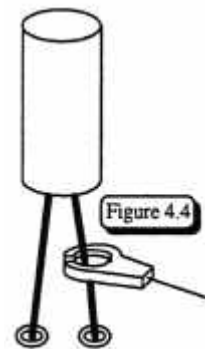
In the case of the tuning fork - type crystal (20kHz to 165kHz), the drive level is very small (1μW maximum). If the CI value is 50kΩ, the current that runs through the crystal is approximate 4.5μA. This current cannot be read by an oscilloscope as in the procedure of 4.1.1. due to being too small. Hence, a special instrument must be used for measuring the current: the selectable level meter.



Use the current probe as in the AT crystal procedure, then read the current from the meter.

4.1.3. How to use a current probe

Please use the current probe as shown in Figure 4.4. The leads are necessary in order to measure the current, so please use a cylinder type part even if the part is surface - mounted. Actual characteristics will not change between a cylinder - type part and surface - mounted part.



4.2. Measurement of the oscillation Allowance

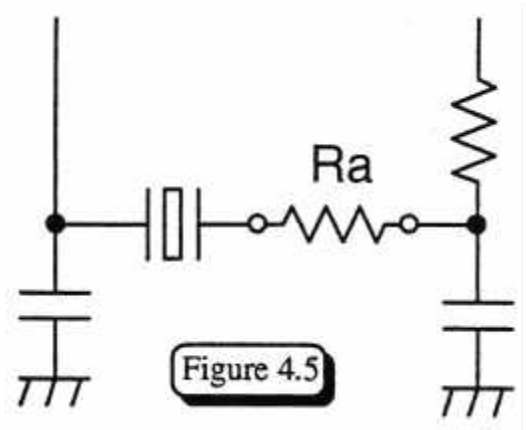
The procedure of measuring the oscillation allowance is to place a resistance in series beside the crystal.

With this additional resistance, the amount of CI necessary for creating oscillation can be measured. That means the 'allowance' for oscillation. The oscillation allowance is indicated by the value of the additional resistance (ref., Negative resistance has the same meaning as oscillation allowance).

Basically, the oscillation allowance required is at least five (5) times the CI maximum. To prepare the Ra for evaluation, please use as many resistors as possible from more than 5 times CI (up to 10 times CI if possible).

Cut off the power to the circuit and add resistors beginning with a low value, becoming progressively higher. Monitor the wave form with the oscilloscope; the circuit has allowance if it oscillates. Continue this procedure, gradually increasing the resistance. The circuit will show no oscillation at an Ra condition. It means

the limit of the allowance is under the condition necessary for oscillation. So the previous resistance is the value of allowance. That is to say, the circuit oscillated when the Ra was 470kΩ, it did not oscillate when the Ra was 510kΩ. In this case, 470kΩ (actually -470kΩ) is the oscillation allowance.



4.3. Actual data sampling

Provided an unusual value for RF is not chosen among the parameters for the oscillation circuit (Rf, Rd, Cg and Cd), the circuit will work even if these are small variations in the values. Actually data sampling is done with varying Rd, Cg and Cd. The best parameter will be confirmed by using a graph described on 3.1. which uses Cg and Cd for the X axis and drive level and oscillation allowance for the Y axes. So, data should be collected using various values for Cg and Cd applied to several Rd conditions. For the capacitance of Cg and Cd choose as many as possible from 5pF to 50pF. We recommend that you use a data chart as follows:

Cd=Cg	Drive Level	Ra Max. (Oscillation Allowance)	Comment
5pF			
6pF			
7pF			
8pF			
9pF			
10pF			
12pF			
:			
47pF			
50pF			

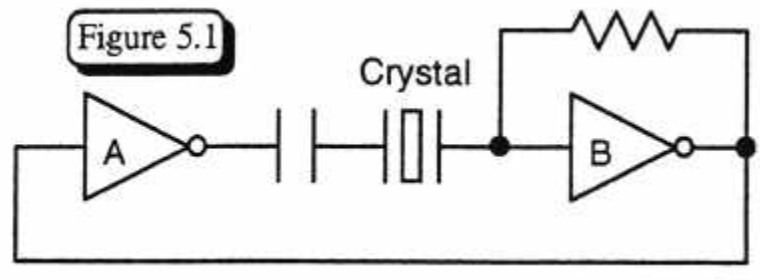
The main things to concentrate on are drive level and oscillation allowance. The other item is a comment concerning with any problem with oscillation start up time, etc. When data sampling is finished, find the range which shows acceptable characteristics by producing a graph.

5. Other circuits and frequencies

This document described the parallel resonance oscillation circuit using a C-MOS inverter device, the crystal is both tuning fork and fundamental AT crystal type. This section will explain the other circuits and frequencies.

5.1. Series resonance circuit with C-MOS inverter

Usually, the series resonance circuit with a C-MOS inverter device is constructed as in the following figure:

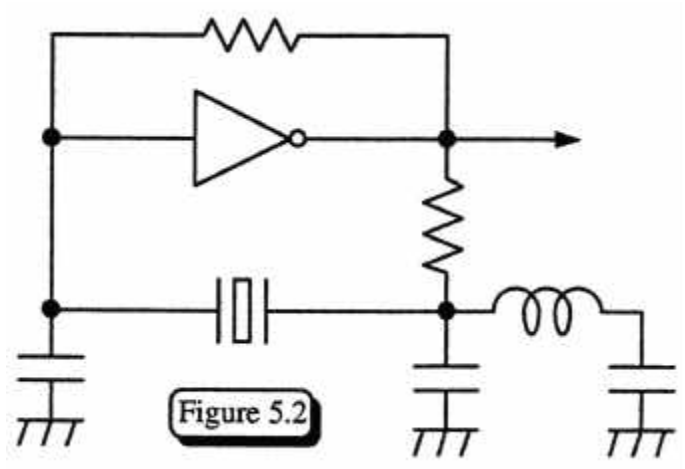


This circuit gives a 5V swing level to the crystal. Hence, usually this circuit supplies a high drive level to the crystal.

Also, there is one more problem in this circuit; that is, when the probe is attached to the input terminal of the 'B' inverter in order to monitor the wave form, a short current passes through the probe due to the probe's input capacitance. The short current creates shock in the crystal and it may damage the crystal. Therefore it might be difficult to evaluate the circuit and we do not recommend the use of this circuit

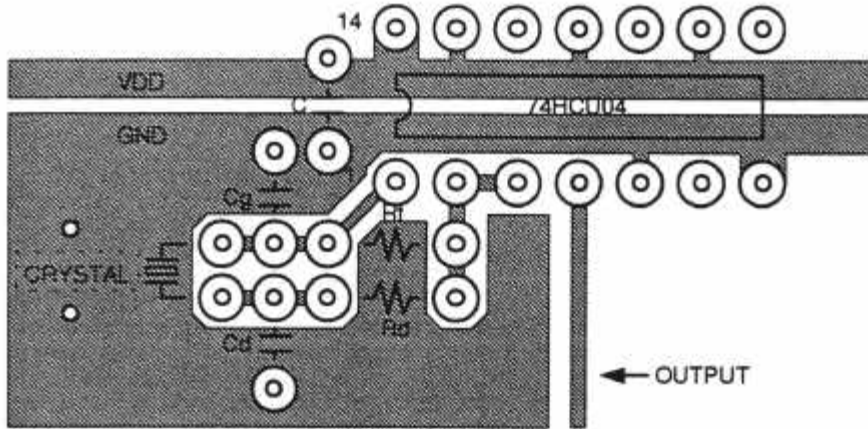
5.2. Overtone oscillator circuit for AT crystals

The general circuit for the overtone oscillation with an AT crystal is as follows: However the construction of the circuit and parameters may be changed due to the IC characteristics, frequency, pattern layout on the board, etc. It is usually difficult to keep sufficient oscillation allowance (especially in the case of a high frequency circuit due to be frequency being close to the device's speed limit). The basic way to measure the drive level and oscillation allowance is the same as in the fundamental circuit but, we recommend that this circuit is evaluated by SEIKO EPSON Corp.

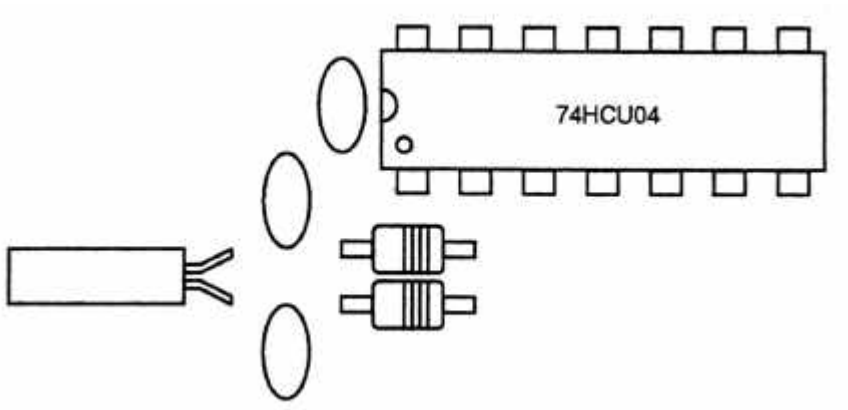


Appendix A. Oscillation Circuit Example

- i. Through hole parts.
Print Pattern Layout:

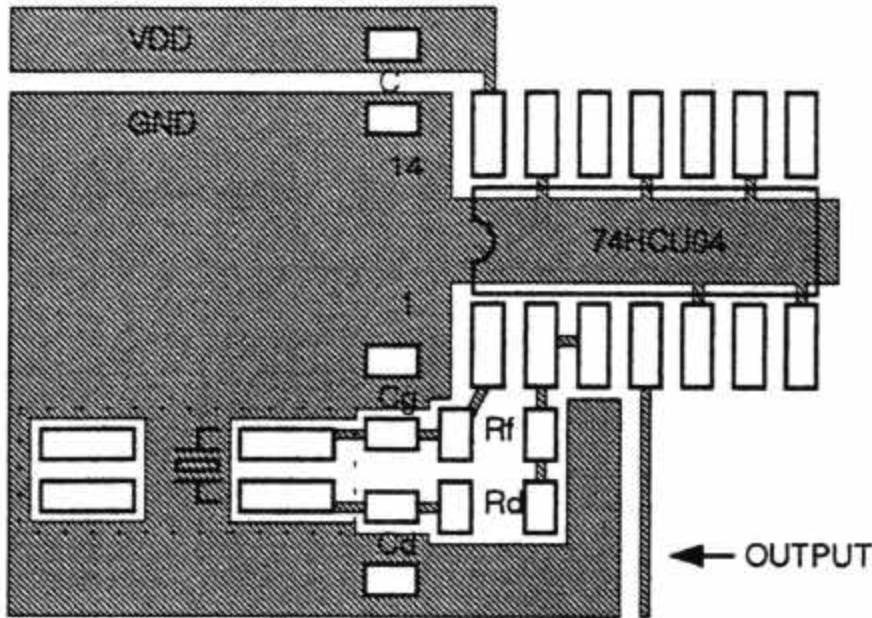


Parts layout :

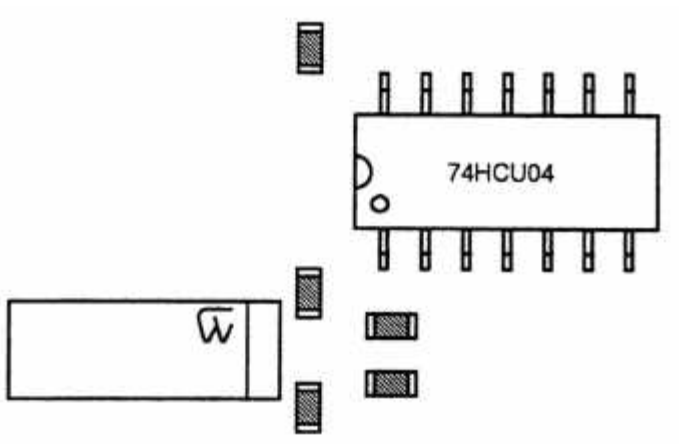


Note : The above drawing is not to scale.

- ii. Surface mount parts.
Print Pattern Layout :



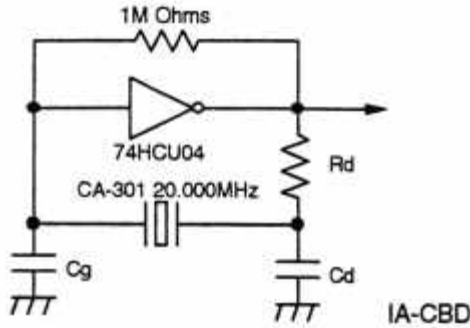
Parts Layout :



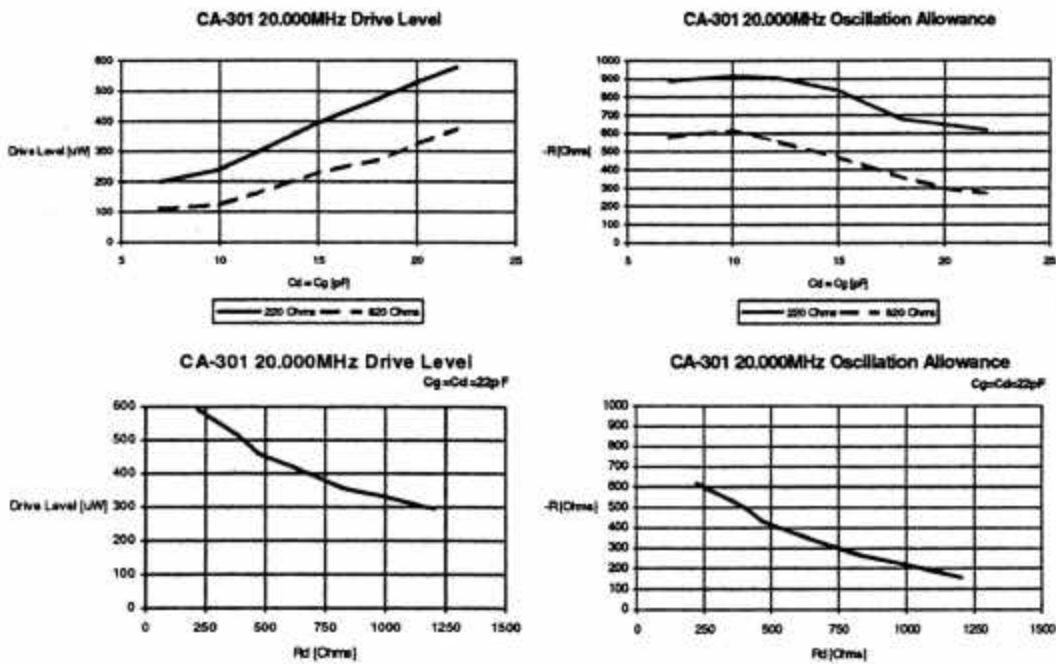
Note : The above drawing is not to scale.

Appendix B. Example of the Drive Level, Oscillation Allowance Characteristics

Circuit



The following charts indicate the characteristics of the drive level and oscillation allowance:



In the upper two graphs, the data are measured on two R_d conditions, R_d = 220Ω and 820Ω. The characteristics are taken with changing C_g and C_d from 7pF through 22pF. The CA - 301 has a specified C_I value of 40Ω maximum at 20.000MHz. Hence the oscillation allowance must be at least -200Ω. In this case, the highest oscillation allowance is C_g=C_d=10pF each and the graph shows enough oscillation allowance. In this point, the drive level shows approximately 240µW on 220Ω R_d and 120µW on 820Ω R_d. According to these data a recommended condition is;

$$R_d = 820\Omega \quad C_g \text{ and } C_d = 10pF$$

The lower two graphs show the characteristics of the drive level and oscillation allowance against R_d variation. These data are measured on 22pF C_g and C_d. The larger R_d can reduce the drive level. However, it also reduces oscillation allowance.

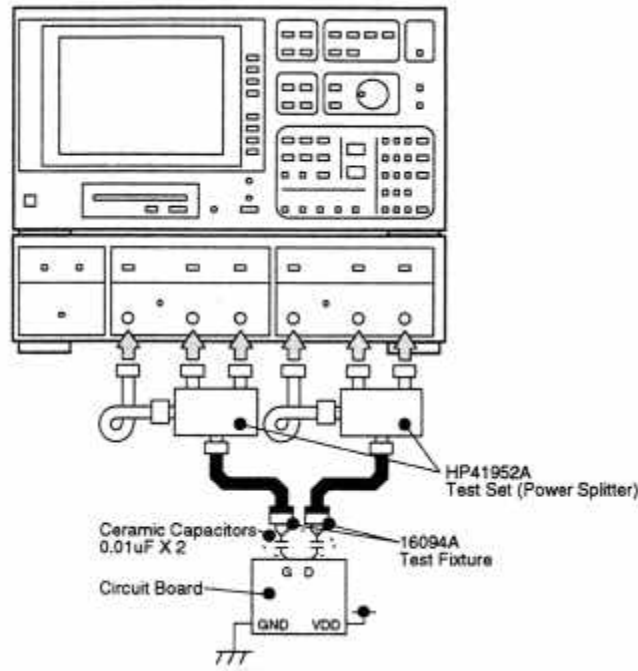
NOTE

The purpose of these data is to see the general characteristics of the relation of Drive level and oscillation allowance against R_d, C_g and C_d variation. The values are only for reference and you may find differences in actual test conditions. Because, the values will be affected by the circuit construction and difference in board design.

Appendix C. Measurement of Negative Resistance using the S - Parameter

In order to confirm the matching of the circuit to the required oscillation mode to inhibit unnecessary oscillation modes, we recommend measuring the negative resistance using the S - Parameter. The following shows the general system configuration for measuring the negative resistance using the S - Parameter:

HP 4195A Network/Spectrum Analyzer

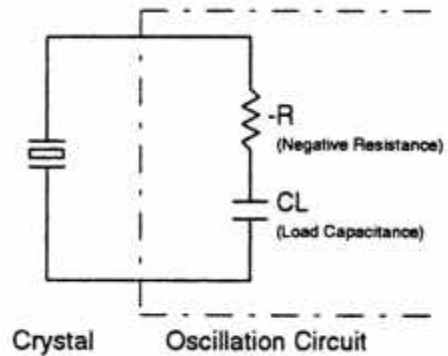


(This figure referred from HP 4915A Maintenance Manual Fig 3-5)

The equivalent parameter of the oscillation circuit is as follows:

This procedure measures the negative resistance and CL using a network analyzer. To connect the network analyzer, remove the crystal from the board, then connect the test fixture to the board.

The network analyzer measures each parameter; -R and the CL which is converted to reactance (Xc). The CL can be calculated from Xc by the following formula;



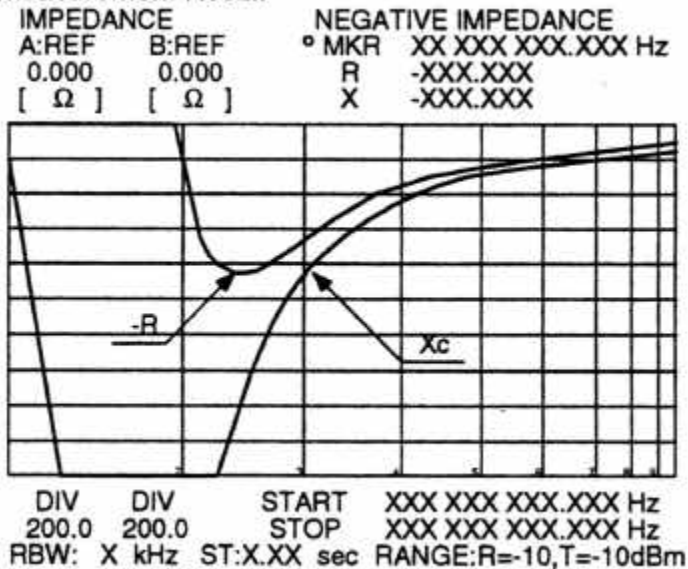
The measurement program example is mentioned on next page. Using this procedure, you will achieve a result as shown in the example on the next page.

Example of Measurement Program

```

100 CMT "NEGATIVE IMPEADANCE"
110 DISP "START FREQUENCY"
120 START=10E6
130 DISP "STOP FREQUENCY"
140 STOP=100E6
150 SWT2
160 RBW=3 KHz
170 !***S PARA
180 FNC4;SPI3
190 DISP "S11"
200 SWTRG
210 E=MA;F=MB
220 FNC5;GPP3
230 DISP "S21"
240 SWTRG
250 I=MA;J=MB
260 FNC6;GPP3
270 DISP "S12"
280 SWTRG
290 G=MA;H=MB
300 FNC7;SPI3;DPB1
310 DISP "S22"
320 SWTRG
330 RA=MA;RB=MB
340 !
350 !****N Z CAL
360 BEEP
370 DISP "CSL"
380 WAIT 1
390 DSP1
400 <RC,RD>=<(1,0>+<E,F>)*<(1,0>-<RA,RB>)+<(1,0>+<RA,RB>)*<(1,0>-<E,F>)>
410 <RE,RD>=<RC,RD>-<2,0>*<G,H>-<2,0>*<I,J>+<2,0>*<G,H>*I,J>
420 <RE,RF>=<RE,RF>/(<(1,0>-<E,F>)*<(1,0>-<RA,RB>-<G,H>*I,J>)>
430 FNC3;IMP2;DPB1
440 A=RE*50;B=RF*50
450 SCL1;DIV=200;REF=0
460 SCL2;DIV=200;REF=0
470 END
    
```

Example of the Measurement Result



Appendix D. Example of the Evaluation Equipment

For AT Crystal			
Scope	Oscillo-Scope	2465B	Tektronics
Probe	AC Current Probe	P6022	Tektronics
Amp.	Current Probe Amplifier	Type 134	Tektronics
For Tuning Fork Crystal			
Selectable Level Meter		ML422A	Anritsu
Probe	DC.AC Current Probe	A6302	Tektronics
Amp.	Current Probe Amplifier	AM503	Tektronics
	Power Rack	TM501A	Tektronics
Using S-Parameter			
Network/Spectrum Analyzer		HP4195A	Hewlett Packard
Power Splitter	Test Set	HP51952A	Hewlett Packard
Test Fixture		16094A	Hewlett Packard

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易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立,致力并专注于微波、射频、天线设计研发人才的培养;我们于 2006 年整合合并微波 EDA 网(www.mweda.com),现已发展成为国内最大的微波射频和天线设计人才培养基地,成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程,广受客户好评;并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书,帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司,以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训课程列表: <http://www.edatop.com/peixun/rfe/129.html>



射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材;旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习,能够让学员完全达到和胜任一个合格的射频工程师的要求...

课程网址: <http://www.edatop.com/peixun/rfe/110.html>

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 ADS 培训教程,共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解,并多结合设计实例,由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS,迅速提升个人技术能力,把 ADS 真正应用到实际研发工作中去,成为 ADS 设计专家...



课程网址: <http://www.edatop.com/peixun/ads/13.html>



HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程,是迄今国内最全面、最专业的 HFSS 培训教程套装,可以帮助您从零开始,全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装,更可超值赠送 3 个月免费学习答疑,随时解答您学习过程中遇到的棘手问题,让您的 HFSS 学习更加轻松顺畅...

课程网址: <http://www.edatop.com/peixun/hfss/11.html>

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出,是最全面、系统、专业的 CST 微波工作室培训课程套装,所有课程都由经验丰富的专家授课,视频教学,可以帮助您从零开始,全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装,还可超值赠送 3 个月免费学习答疑...

课程网址: <http://www.edatop.com/peixun/cst/24.html>



HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书,课程从基础讲起,内容由浅入深,理论介绍和实际操作讲解相结合,全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程,可以帮助您快速学习掌握如何使用 HFSS 设计天线,让天线设计不再难...

课程网址: <http://www.edatop.com/peixun/hfss/122.html>

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程,培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合,全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作,同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习,可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试...

详情浏览: <http://www.edatop.com/peixun/antenna/116.html>



我们的课程优势:

- ※ 成立于 2004 年,10 多年丰富的行业经验,
- ※ 一直致力并专注于微波射频和天线设计工程师的培养,更了解该行业对人才的要求
- ※ 经验丰富的一线资深工程师讲授,结合实际工程案例,直观、实用、易学

联系我们:

- ※ 易迪拓培训官网: <http://www.edatop.com>
- ※ 微波 EDA 网: <http://www.mweda.com>
- ※ 官方淘宝店: <http://shop36920890.taobao.com>