# QCP1701 Mobile Multimedia Processor

Product Brief

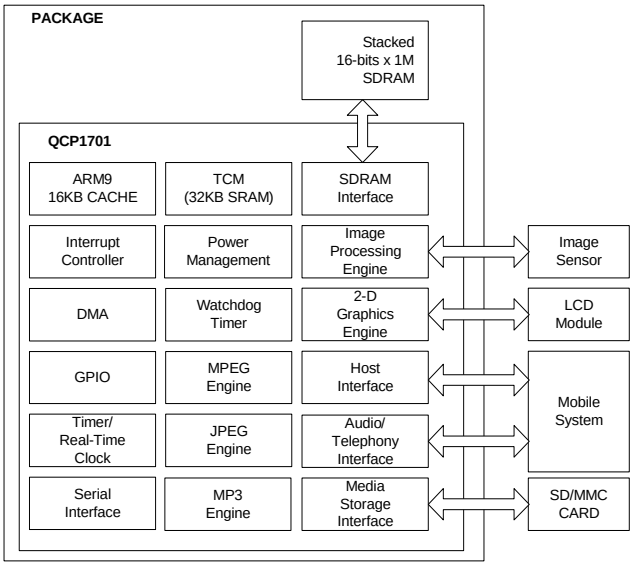

## Overview

QCP1701 is a high performance and low power multimedia processor, especially designed for handheld devices such as mobile phones and PDAs. The QCP1701 integrates a 32-bit ARM processor, hardware-accelerated video/image codecs, speech/audio firmware codecs, peripheral interfaces, a real-time operation system, and firmware applications into one single chip. With ultra low power feature, the QCP1701 enables users to enjoy multimedia applications anytime anywhere.

In order to give the users outstanding multimedia capabilities and take into consideration of the requirement of low power consumption in handsets at the same time, the core features of QCP1701 are hard-wired, including MPEG-4 video codec, image processing engine, JPEG codec, 2D graphics engine, and MP3 player to bring the users unprecedented multimedia experience. Additionally, for audio and speech applications, QCP1701 provides optimized firmware solutions as well, including AMR encoding/decoding, MP3 decoding, and AAC decoding for Hi-Fi sound.

The peripheral interfaces of QCP1701 make your integration job smoothly without extra cost for mobile host, image sensor, LCD module, SD/MMC card, USB interface, and audio device, and so on. Through the application programming interface (API) of QCP1701, firmware applications such as audio/video (A/V) recorder, A/V player, camera and viewer functions, and a file system are provided.

## QCP1701 Block Diagram




## Features

- **Processor**
  - 32-bit ARM9 RISC processor
  - 8KB I-cache and 8KB D-cache
  - Embedded 16KB I-SRAM and 16KB D-SRAM
  - Programmable CPU operating frequency up to 72MHz

- **Video Codec**
  - Scalable resolutions from 16x16 to 352x288 @ 30 fps
  - MPEG-4 Simple Profile @ L0-3 from 64 to 384 Kbps
  - Supports I and P pictures
  - H.263 Profile 0
  - Programmable group of VOP
  - CBR and VBR rate control
  - Fast forward and reverse
  - Error resilience and concealment tools include resynchronization marker, data partitioning, header extension code, and RVLC

- **Image Codec**
  - Supports Resolution Up to 2M Pixels JPEG Codec
  - Auto exposure
    - Automatic / manual mode
    - Matrix metering, spot metering and center-weighted metering
    - Flicker-free
    - Adjustable ISO / shutter combinations
    - Last-second exposure compensation/mitigation
    - Multi-frame jumbo operation
  - Auto white balance
    - Automatic / manual mode
    - Preset mode
  - Sensor compensation function
    - Defective pixel correction
    - Vignetting compensation
  - Color adjustment function
    - Adjustable color correction matrix
    - Color space conversion
    - Saturation control
    - Skin-tone correction
  - Image enhancement function
    - Contrast adjustment
    - Edge Enhancement
    - Gamma correction
    - Digital zoom (1x-8x, 32 steps)
  - Special effects ( Black/white, Sepia, False color, Negative, Posterization, Solarization, Emboss, Sketch)

- **Audio Codec**
  - Low Power MPEG Layer III (MP3) Decoder (<10mA)
  - Enhanced aacPlus decoder
  - MIDI synthesizer
  - Mono and stereo channel configurations
  - 3GPP AMR codec

- **2D Graphics**
  - BitBlt for Image size below 240x320
  - Sprites
  - Color transparency

- Rectangle fill
- Clipping (for RGB image only)
- 90 degree rotation, mirror, scaling
- Eight display layers with Z-order and multiple source format (RGB565, RGB666, YUV422/ YUV420)
- Alpha-blending for the top display layer
- On-screen display (OSD)

♦ **LCD Interface**
- Support various LCD modules (LCM) with RAM integrated
- Resolution up to 240RGBx320 (QVGA)
- Support dual-glasses LCM
- Support both i80 and M68 CPU IF
- Programmable polarity of all control signals to support various LCM
- GPIO-like memory map interface for initialization with CPU IF
- Input format 16-bit (65K colors)/18-bit (260K colors)

♦ **Camera Interface**
- Programmable input format (RGB444 and YUV422)
- Support master-type CMOS sensors, such as OmniVision series
- Support resolution up to UXGA

♦ **Host interface**
- LCD-interface-like host interface
- 16-bit CPU interface
- 18-bit LCD bypass interface

♦ **Audio Interface**
- I2S
- ADI DSP audio interface
- Master/slave clock to external audio codec chips
- Audio sample rates (8K/11.025K/12K /16K/22.05K/24K/ 32K/44.1K/48K Hz)

♦ **External memory card interface**
- MMC
- SD and miniSD
- NAND Flash

♦ **USB**
- 2.0 Full speed
- Block and isochronous transfer
- PC storage
- PC cam

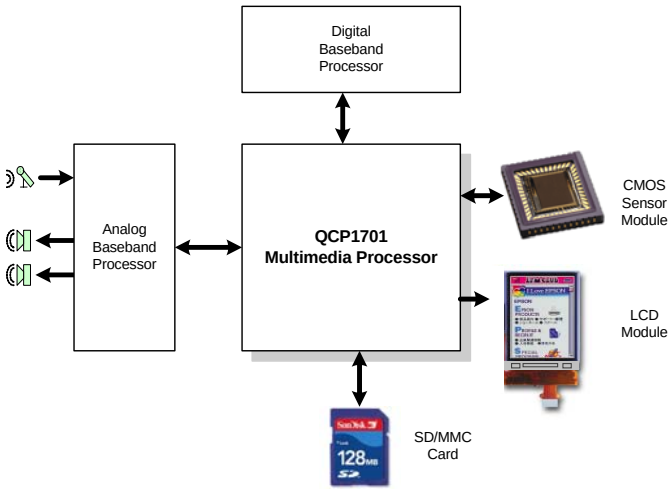
♦ **GPIO**
- GPIO pins
- Support interrupt function in each GPIO

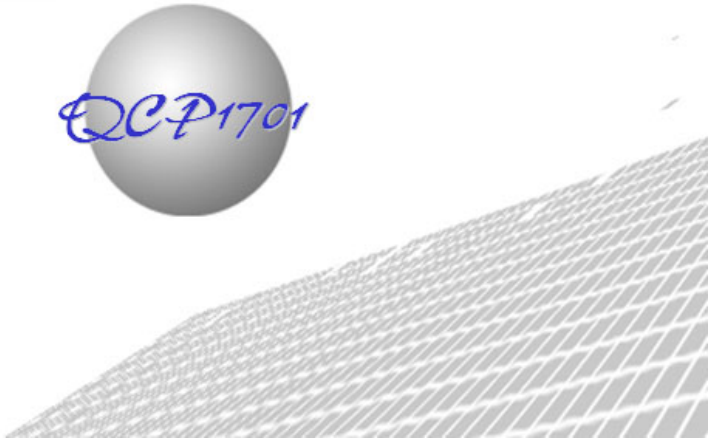
♦ **Clock**
- Internal PLL driven by a single external reference clock 13MHz and 26MHz
- Provide clocks to drive external audio codec chips
- PLL bypass mode available

♦ **Power Save**
- Programmable partial clock power saving
- Bypass mode to allow the host access LCM and audio codec directly

♦ **Package and Power**
- JTAG for ARM software debug and boundary scan
- 1.2 voltage for core die and 2.8 voltage for IO and SDRAM
- 144 pins lead-free TFBGA package (9x9 mm size)

## Application Block Diagram



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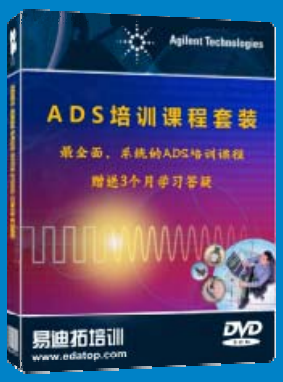


该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

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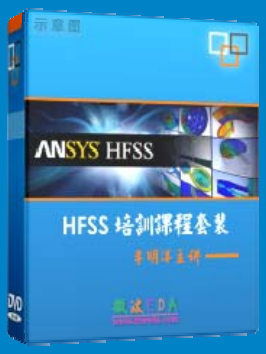


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该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

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※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

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