130-mW DIRECTPATH STEREO HEADPHONE DRIVER

DESCRIPTION

The SN4911 is stereo headphone drivers designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The SN4911 is ideal for small portable electronics where size and cost are critical design parameters.

The SN4911 is capable of driving 130 mW into a 32-Ω load at 4.5V. It has a fixed gain of –1.5 V/V. The SN4911 has independent shutdown control for the right and left audio channels.

The SN4911 is available in a 2.06mm×2.06mm WCSP and 4 mm ×4 mm Thin QFN packages.

FEATURES

- Space Saving Packages，4 mm ×4 mm QFN-20 and 16 ball WCSP
- Ground-Referenced Outputs Eliminate DC-Bias Voltages on Headphone Ground Pin
  - No Output DC-Blocking Capacitors
  - Reduced Board Area
  - Reduced Component Cost
  - Improved THD+N Performance
  - No Degradation of Low-Frequency Response Due to Output Capacitors
- Independent Right and Left Channel Shutdown Control
- Short-Circuit and Thermal Protection
- Pop Reduction Circuitry

APPLICATIONS

- CD / MP3 Players
- Smart Phones
- Cellular Phones
- PDAs

Typical Application Circuit

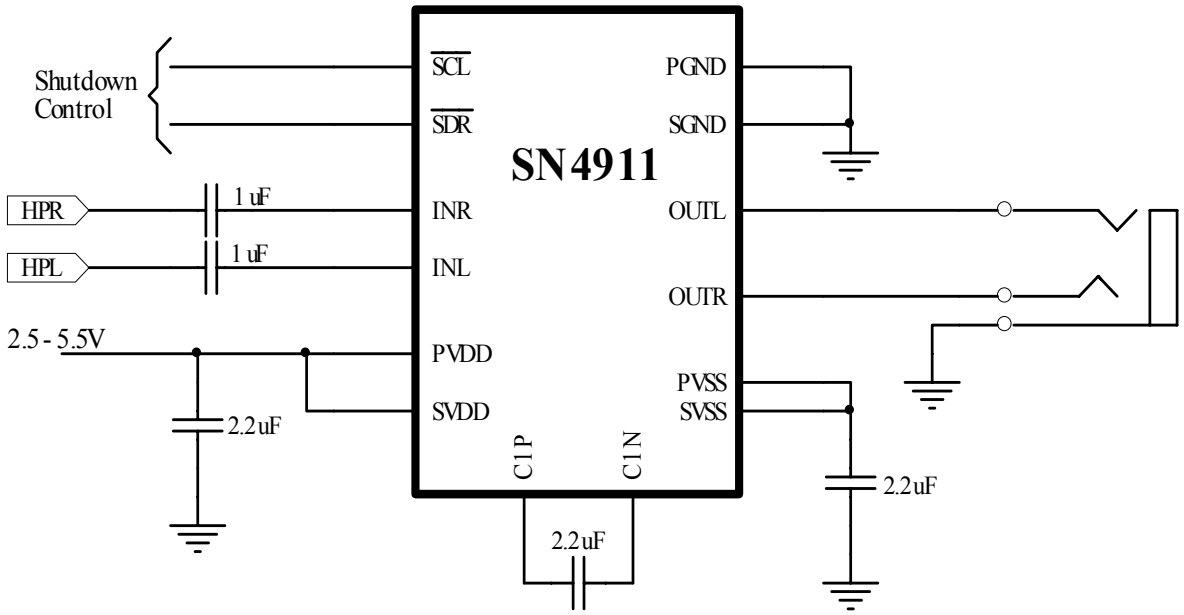
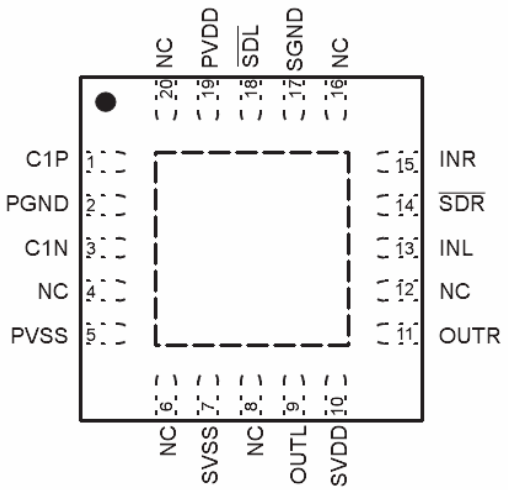
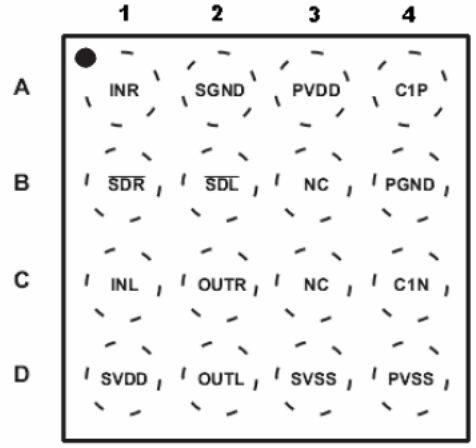


Figure1

Pin Configurations

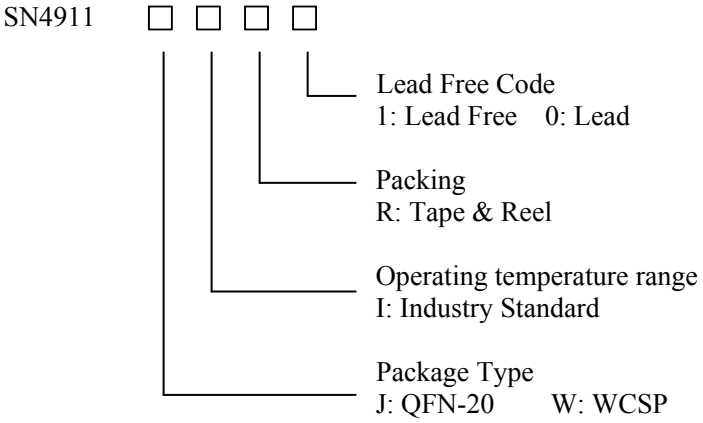
Part Number	QFN-20	16ball WCSP
Pin Configurations		

Pin Description

TERMINAL			I/O	DESCRIPTION
NAME	QFN	WCSP		
C1P	1	A4	I/O	Charge pump flying capacitor positive terminal
PGND	2	B4	I	Power ground, connect to ground.
C1N	3	C4	I/O	Charge pump flying capacitor negative terminal
NC	4, 6, 8, 12, 16, 20	B3, C3		No connection
PVSS	5	D4	O	Output from charge pump.
SVSS	7	D3	I	Amplifier negative supply, connect to PVSS via star connection.
OUTL	9	D2	O	Left audio channel output signal
SVDD	10	D1	I	Amplifier positive supply, connect to PVDD via star connection.
OUTR	11	C2	O	Right audio channel output signal
INL	13	C1	I	Left audio channel input signal
SDR	14	B1	I	Right channel shutdown, active low logic.
INR	15	A1	I	Right audio channel input signal
SGND	17	A2	I	Signal ground, connect to ground.
SDL	18	B2	I	Left channel shutdown, active low logic.
PVDD	19	A3	I	Supply voltage, connect to positive supply.
Exposed Pad		-		Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
SN4911JIR1	QFN-20	xxxx 4911	-40 °C to 85°C
SN4911WIR1	16ball WCSP	Bxxx	-40 °C to 85°C



Absolute Maximum Ratings

- Supply voltage, ---------- -0.3V to 5.5V
- Input voltage ---------- -0.3 V to V_{DD} +0.3V
- Storage temperature ---------- -65°C to 85°C
- Operating Junction Temperature range---------- -40°C to 150°C
- Operating free-air Temperature range---------- -40°C to 85°C

Recommended Operating Conditions

Symbol	Parameter	SN4911		Unit
		Min	Max.	
SVDD PVDD	Supply voltage	2.5	5.5	V
V_{IH}	High level input voltage	1.5		V
V_{IL}	Low level input voltage		0.5	V

Electrical Characteristics

T_A=25℃.

Symbol	Parameter	Conditions	SN4911			Unit
			Min	Typ	Max.	
$\|V_{OS}\|$	Output Offset Voltage			6		mV
V_{OH}	High-level output voltage	V_{DD} = 3 V, 32Ω load	2.4			V
V_{OL}	Low -level output voltage	V_{DD} = 3 V, 32Ω load			–1.7	V
I_{DD}	Supply Current	V_{DD} = 3 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = V_{DD}		6.0	8.0	mA
		V_{DD} = 5 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = V_{DD}		8.5	10.5	
		Shutdown mode, V_{DD} = 2.5 V to 5.5 V			1	μA

OPERATING CHARACTERISTICS

VDD = 3 V , TA = 25°C, RL = 32 Ω (unless otherwise noted)

Symbol	Parameter	CONDITIONS	SN4911			UNIT
			MIN	TYP	MAX	
P_O	Output power (Outputs In Phase)	THD = 1%, V_{DD} = 3 V, f = 1 kHz		62		mW
		THD = 1%, V_{DD} = 4.5 V, f = 1 kHz		130		
THD+N	Total harmonic distortion plus noise	P_O = 25 mW, f = 1 kHz		0.027%		
		P_O = 25 mW, f = 20 kHz		0.012%		
	Crosstallk	P_O = 20 mW, f = 1 kHz		–96		dB
PSRR	Power Supply Rejection Ratio	200-mVpp ripple, f = 217 Hz		–80		dB
		200-mVpp ripple, f = 1 kHz		–68		
		200-mVpp ripple, f = 20 kHz		–41		
Av	Closed-loop voltage gain		-1.45	–1.5	–1.55	V/V
ΔAv	Gain matching			1%		
	Slew rate			2.2		V/μs
	Maximum capacitive load			400		pF
Vn	Noise output voltage			10		μVRMS
fosc	Charge pump switching frequency		280	320	420	kHz
	Start-up time from shutdown			450		μs
	Input impedance		12	15	18	kΩ
SNR	Signal-to-noise ratio	Po = 40 mW (THD+N = 0.1%)		100		dB
	Thermal shutdown	Threshold	150		170	°C
		Hysteresis		15		°C

Typical Operating Characters C(pump)=C(PVSS)=2.2uF, Cin=1uF(unless otherwise noted)
Curve Color: In Phase(Cyan)、180° Out of Phase(Magenta)、AC to input GND(Yellow)、Input Floating(Blue)

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

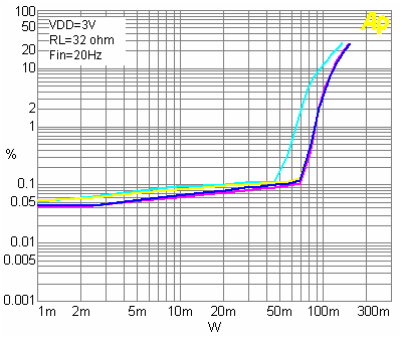


Figure2

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

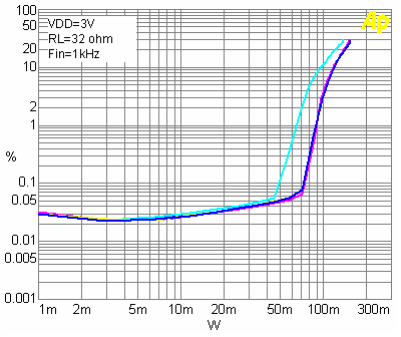


Figure3

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

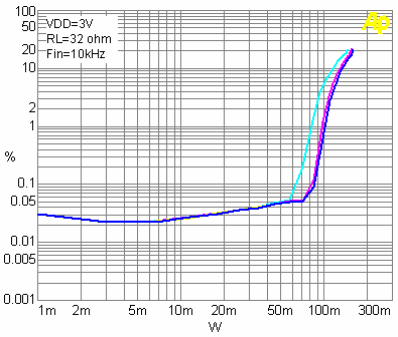


Figure4

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

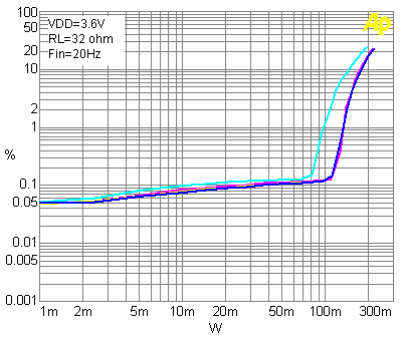


Figure5

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

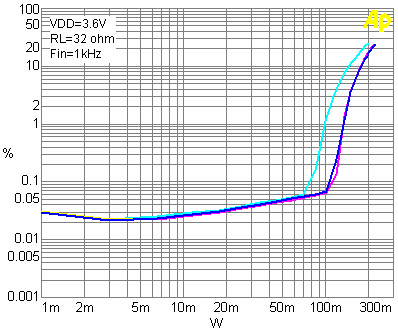


Figure6

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

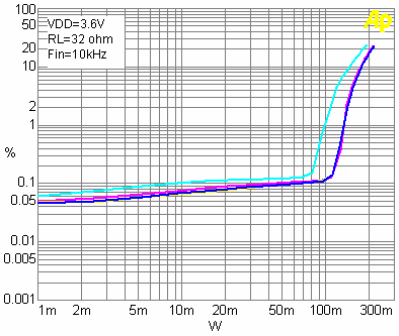


Figure7

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

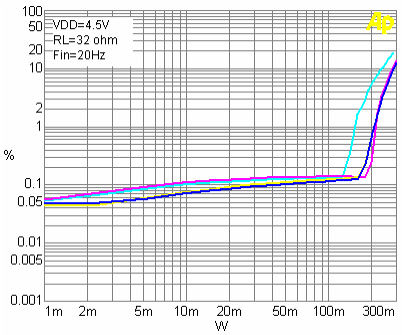


Figure8

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

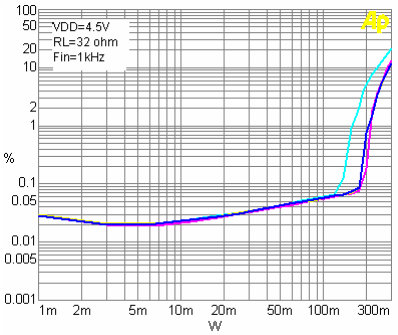


Figure9

TOTAL HARMONIC DISTORTION +Noise Vs OUTPUT POWER

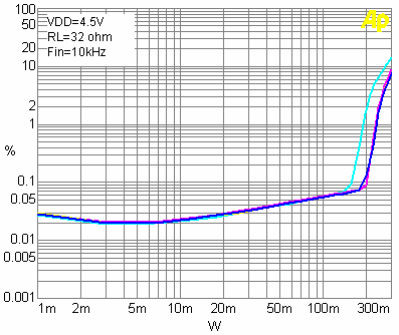


Figure10

THD+N vs. Freq
VDD=3V, RL=32 ohm

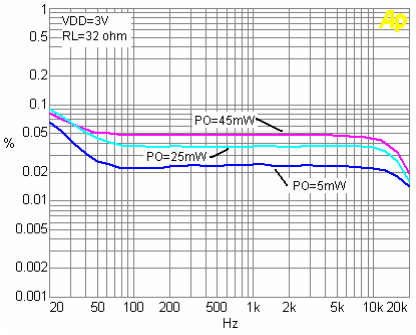


Figure11

THD+N vs. Freq
VDD=3.6V, RL=32 ohm

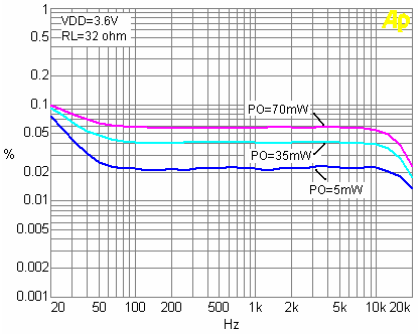


Figure12

THD+N vs. Freq
VDD=4.5V, RL=32 ohm

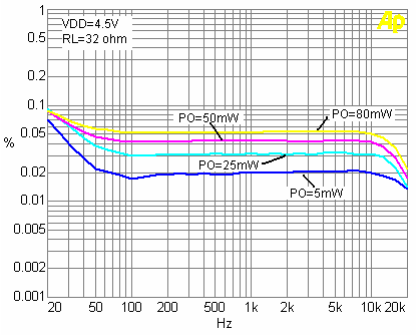


Figure13

PSRR vs. Freq
200mVpp ripple, Input floating

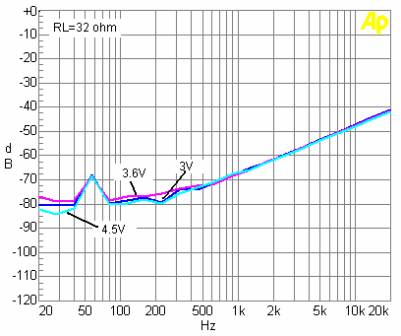


Figure14

CROSSTALK vs. Freq

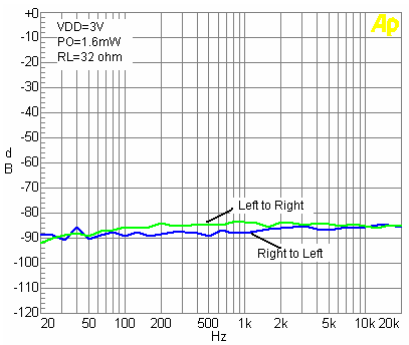


Figure15

CROSSTALK vs. Freq

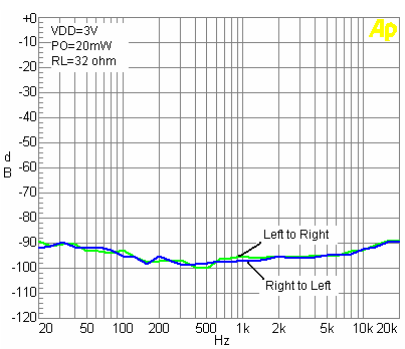


Figure16

OUTPUT SPECTRUM

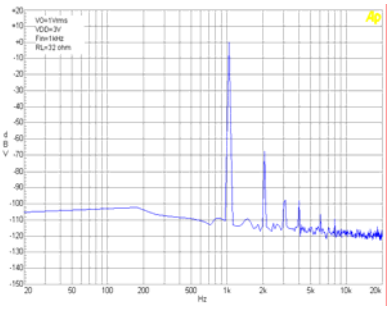


Figure17

Gain and Phase v.s Freq

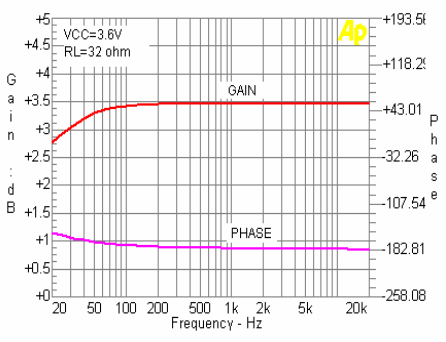


Figure18

Gain and Phase v.s Freq

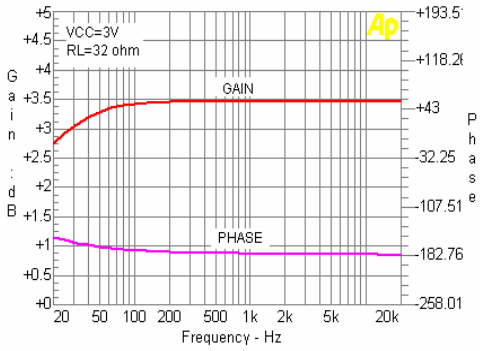


Figure19

Application Information

Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely clipped, and large amounts of dc current rush through the headphones, potentially damaging them. The top drawing in illustrates the conventional headphone amplifier connection to the headphone jack and output signal.

DC blocking capacitors are often large in value. The headphone speakers (typical resistive value of 32Ω) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (C_O), and the cutoff frequency (f_C).

$$f_c = \frac{1}{2\pi R_L C_O} \quad (1)$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \quad (2)$$

If f_C is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area; stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

Two different headphone amplifier applications are available that allow for the removal of the output dc blocking capacitors. The Capless amplifier architecture is implemented in the same manner as the conventional amplifier with the exception of the headphone jack shield pin. This amplifier provides a reference voltage, which is connected to the headphone jack shield pin. This is the voltage on which the audio output signals are centered. This voltage reference is half of the amplifier power supply to allow symmetrical swing of the output voltages. Do not connect the shield to any GND reference or large currents will result. The scenario can happen if, for example, an accessory other than a floating GND headphone is plugged into the headphone connector. See the second block diagram and waveform in Figure 21.

The SN4911 operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The SN4911 requires no output dc blocking capacitors, and does not place any voltage on the sleeve. The bottom block diagram and waveform of illustrate the ground-referenced headphone architecture.

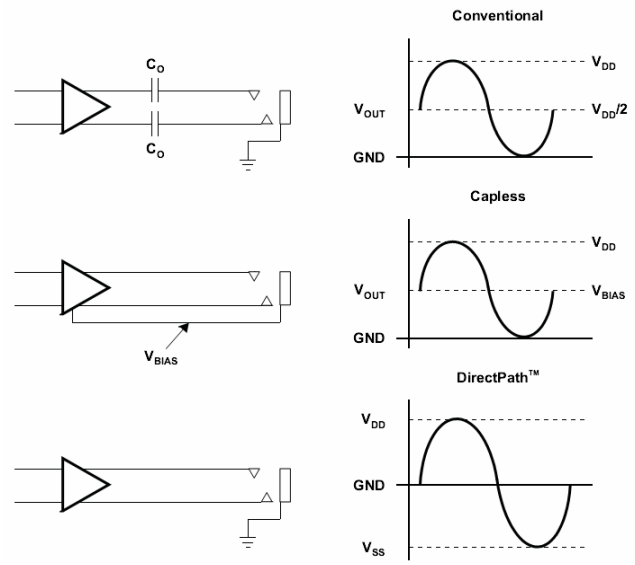


Figure 21. Amplifier application

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the SN4911. These capacitors block the DC portion of the audio source and allow the SN4911 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input impedance of the SN4911. The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input impedance of the SN4911. Because the gains of both the SN4911 is fixed, the input impedance remains a constant value. Using the input impedance value from the operating characteristics table, the frequency and/or capacitance can be determined when one of the two values is given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \quad (3)$$

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 2.2µF is typical. Capacitor values that are smaller than 2.2µF can be used, but the maximum output power is reduced and the device may not operate to specifications.

Decoupling Capacitors

The SN4911 require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 2.2μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the SN4911 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Layout Recommendations

Exposed Pad on SN4911 Package Option

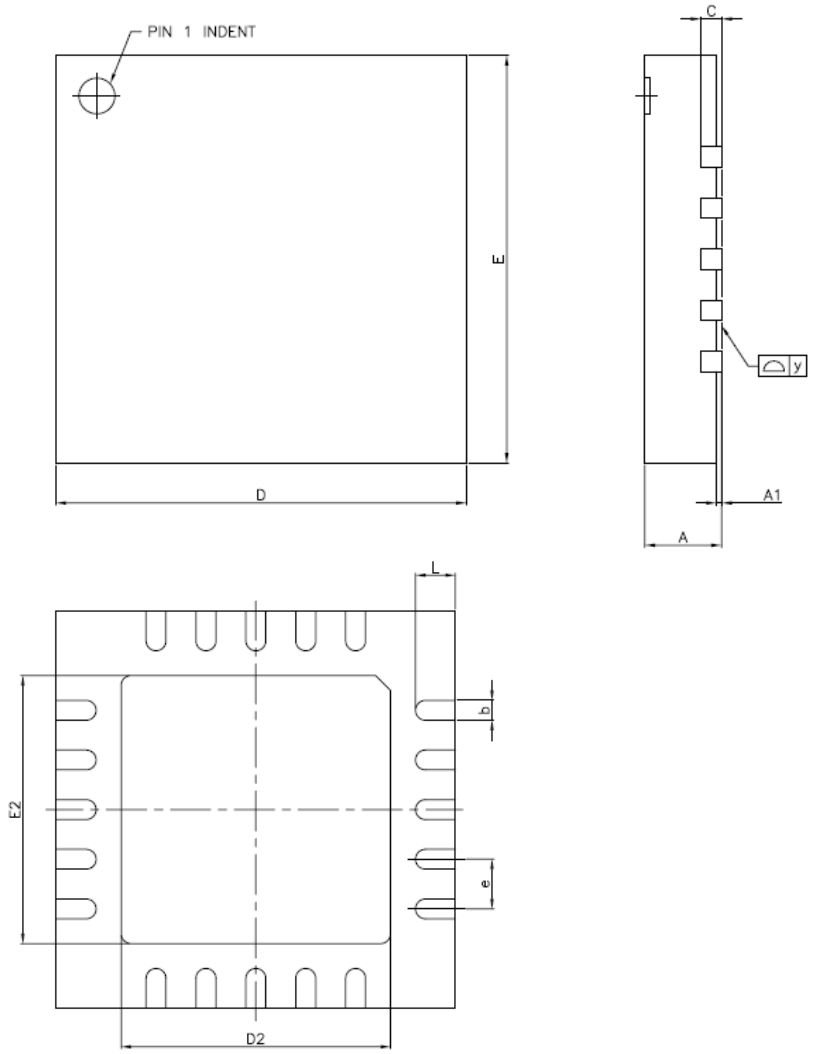
The exposed metal pad on the SN4911JIR1 package must be soldered down to a pad on the PCB in order to maintain reliability. The pad on the PCB should be allowed to float and not be connected to ground or power.

SGND and PGND Connections

The SGND and PGND pins of the SN4911 must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.

Packaging Information

QFN-20

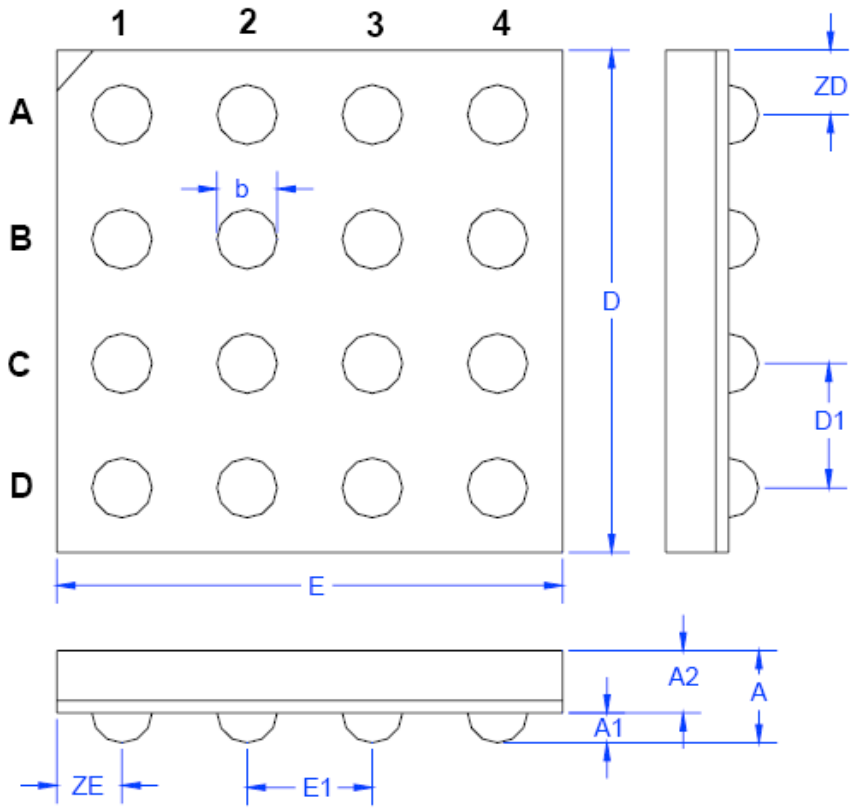


NOTE

The thermal #1 identifier is a laser marked feature

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
C	——	0.20 REF.	——
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075

16 Ball-WCSP



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.575	0.625	0.675
A1	0.215	0.24	0.265
A2	——	0.4	——
b	0.29	0.32	0.35
E	2.04	2.06	2.10
D	2.04	2.06	2.10
D1	0.50		
E1	0.50		
ZD	0.28		
ZE	0.28		

射 频 和 天 线 设 计 培 训 课 程 推 荐

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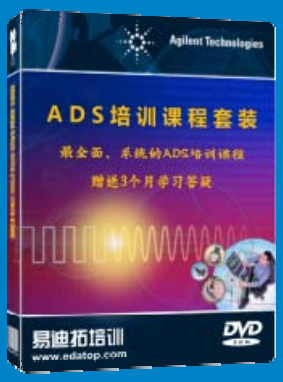
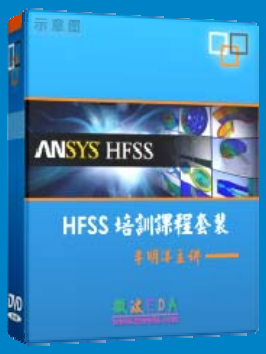


该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html



HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com