

CMOS RF Power Amplifiers: Nonlinear, Linear, Linearized

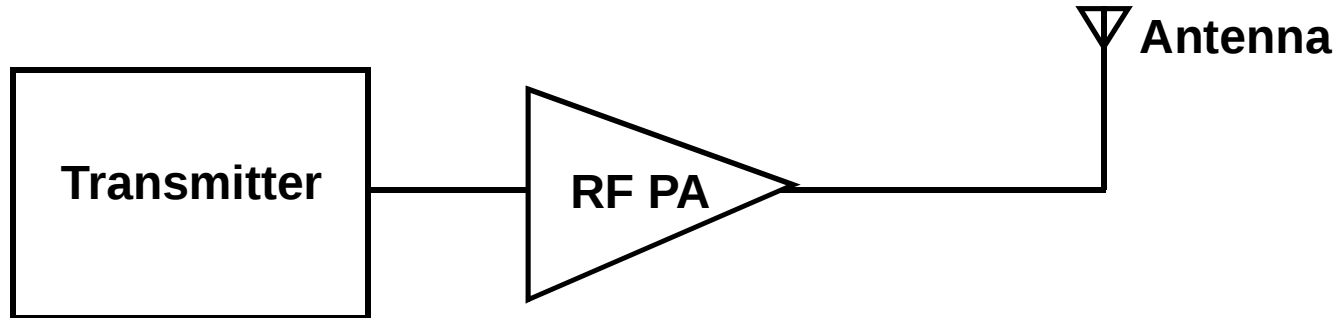
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Outline

- **Introduction**
- **Nonlinear Power Amplification**
- **Linear Power Amplification**
- **Linearization using Envelope Elimination and Restoration**
- **Conclusion**

RF Power Amplification

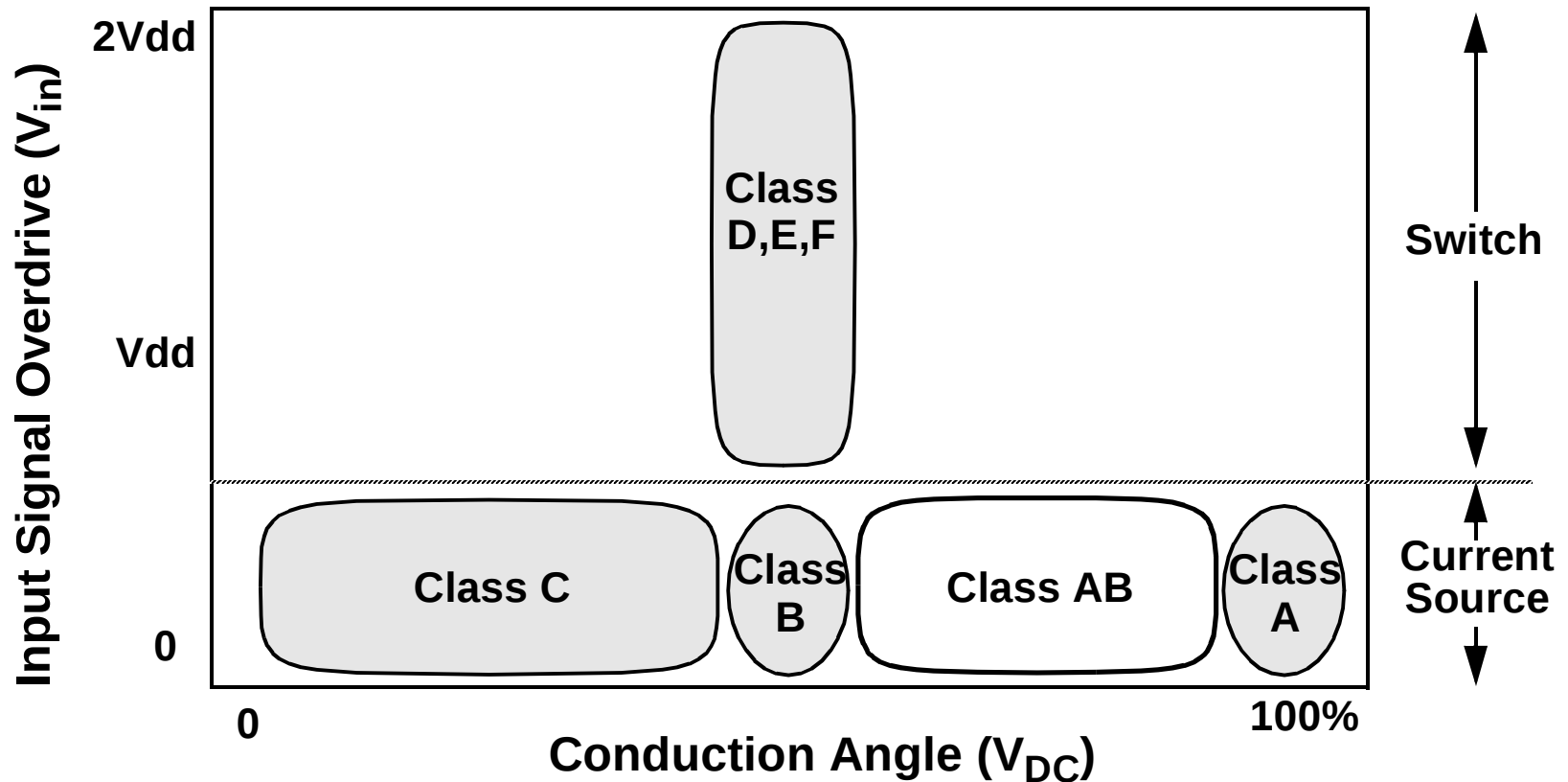


- **Purpose:** Delivers “narrow-band” RF power to a 50-ohm antenna
- **Performance:** Output Power
Efficiency
Linearity

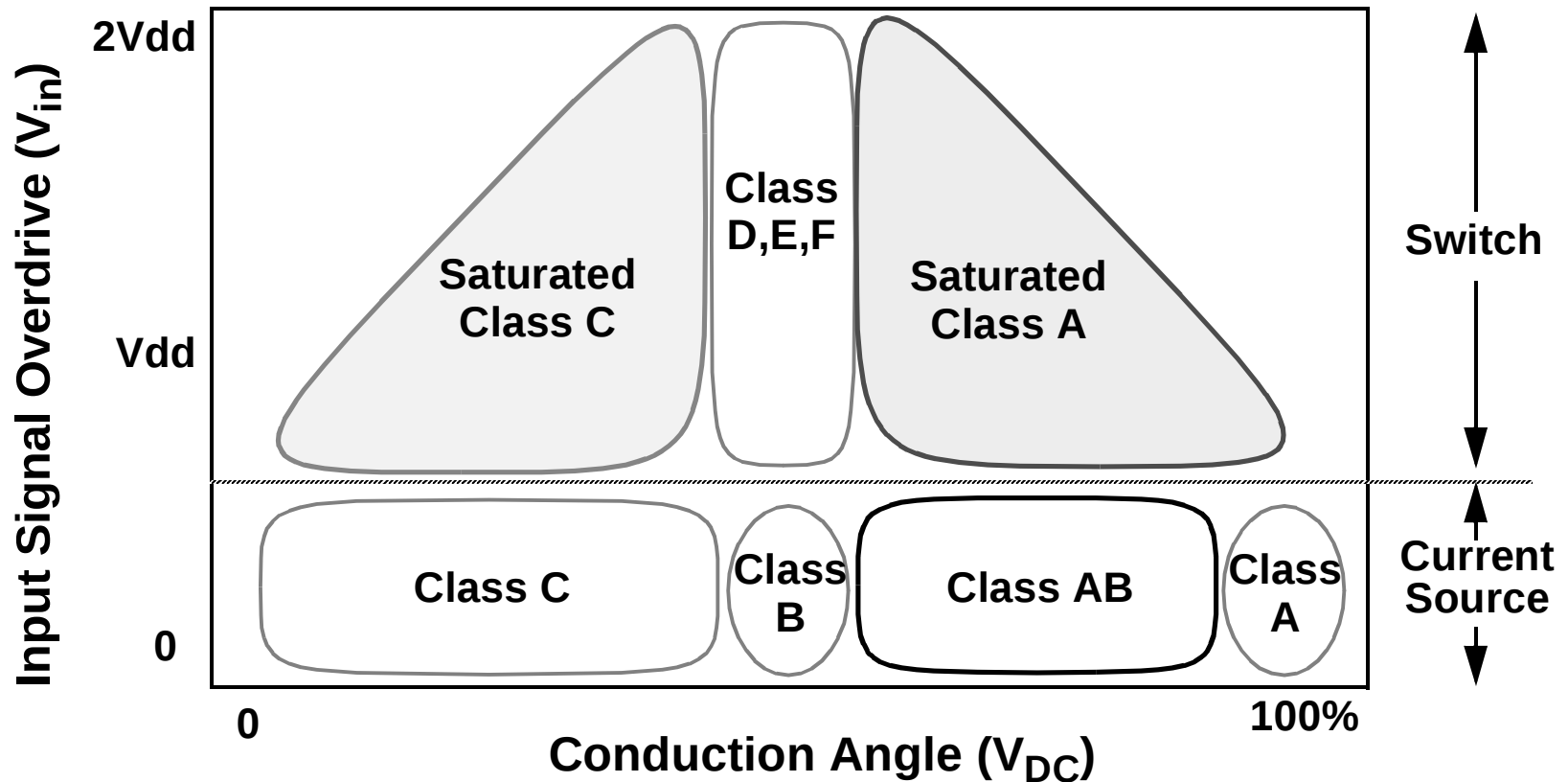
Traditional PA Classification

Class	Modes	Conduction Angle	Output Power	Maximum Efficiency	Gain	Linearity
A	Current Source	100%	moderate	50%	Large	Good
B		50%	moderate	78.5%	Moderate	Moderate
C		< 50%	small	100%	Small	Poor
D	Switch	50%	large	100%	Small	Poor
E		50%	large	100%	Small	Poor
F		50%	large	100%	Small	Poor

PA Classification & Input Drive



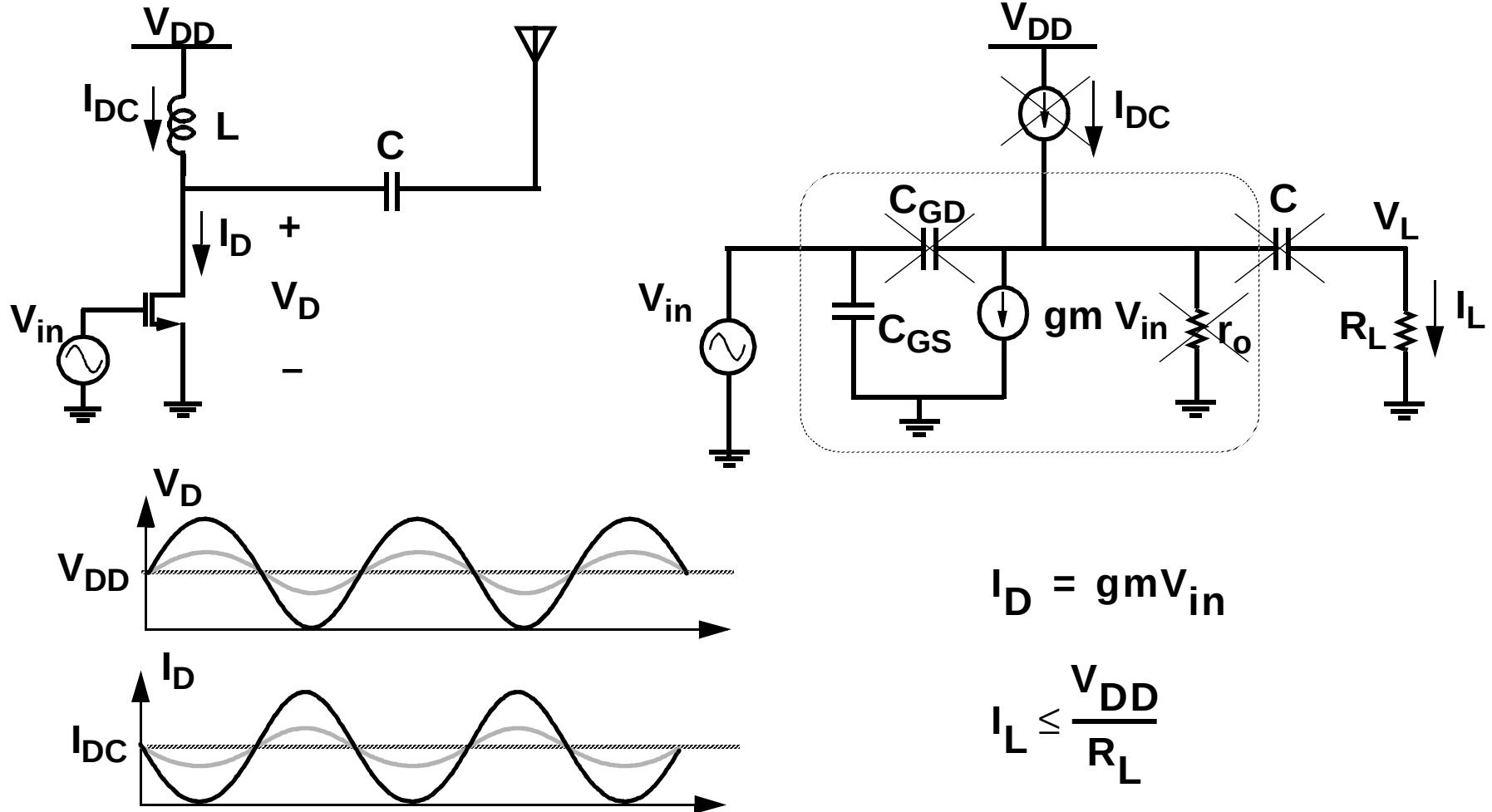
Power Amplifier Classification



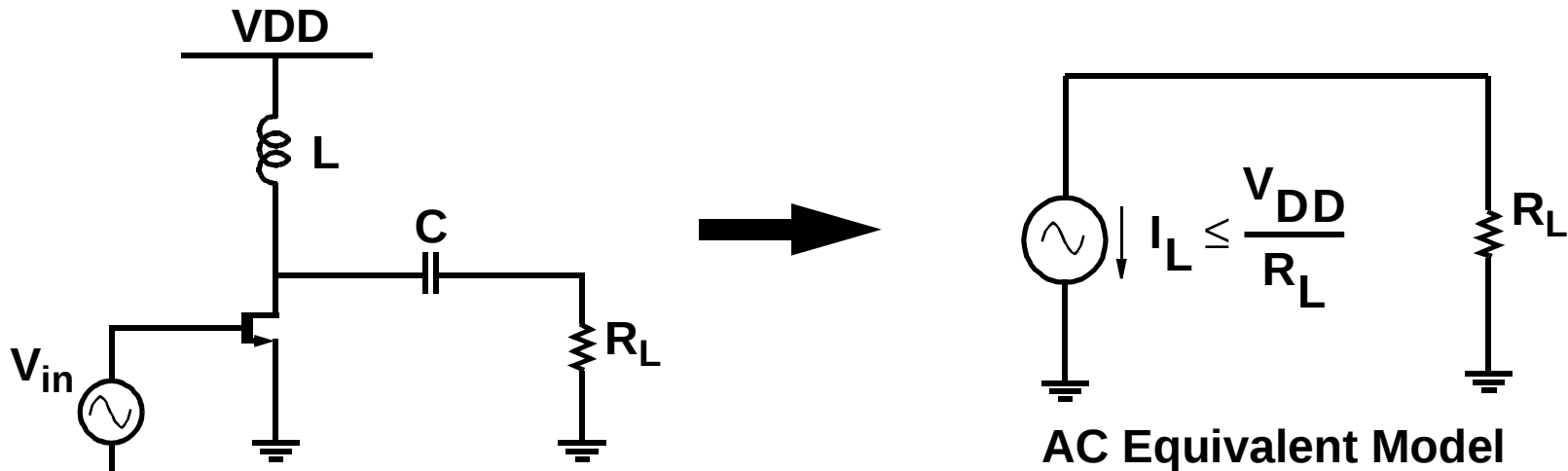
CMOS for RF Power Amplification

- **Traditional RF PAs use GaAs / Bipolar.**
- **Advantages of CMOS:**
 - Low cost, high-yield, high-integration
 - Efficient switched-mode amplifier
- **Disadvantages of CMOS:**
 - Low bandwidth
 - Low breakdown voltage

Simplified RF Output Stage



Class-A (Linear) Operation



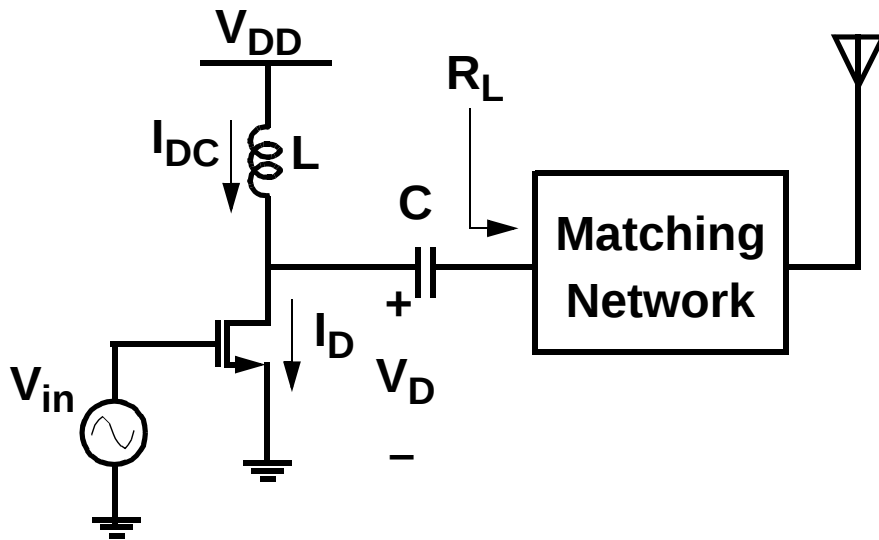
$$P_{out} = \frac{1}{2} I_L^2 R_L \leq \frac{V_{DD}^2}{2R_L}$$

For $P_{out} = 1 \text{ W}$ (Class A), $R_L = 4.5 \Omega @ V_{DD} = 3\text{V}$
 $R_L = 3.1 \Omega @ V_{DD} = 2.5\text{V}$

$\Rightarrow$ Needs Impedance Transformation Network $\rightarrow 50 \Omega$ antenna

$\Rightarrow$ Keep parasitic loss $\ll R_L$ of 3.1Ω

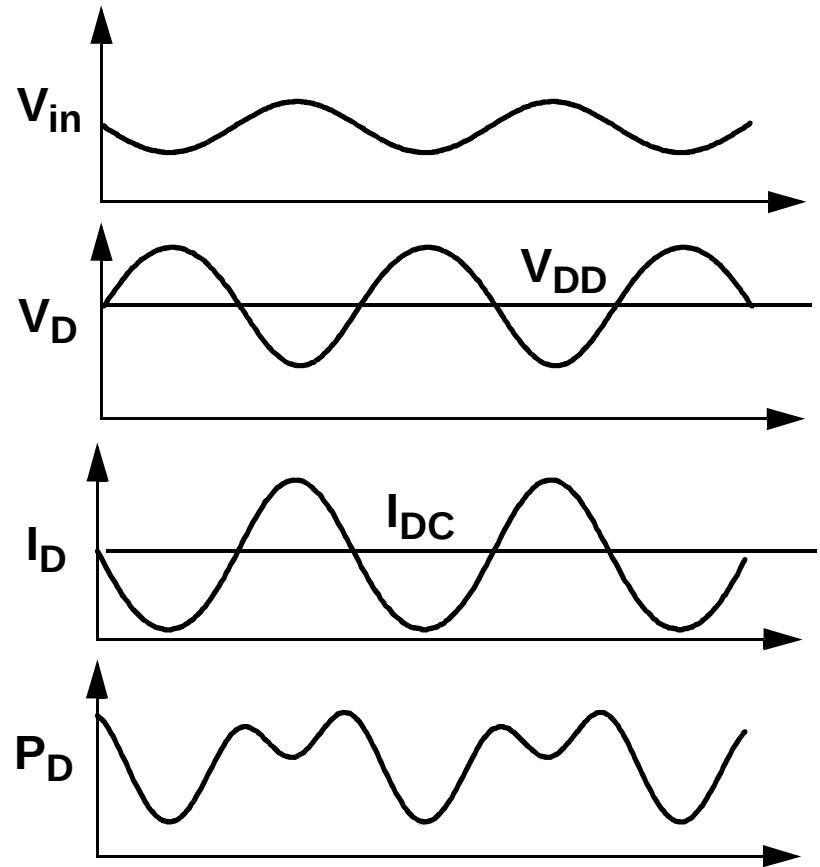
Efficiency of Class A operation



$$P_{out} \leq \frac{V_{DD}^2}{2R_L}$$

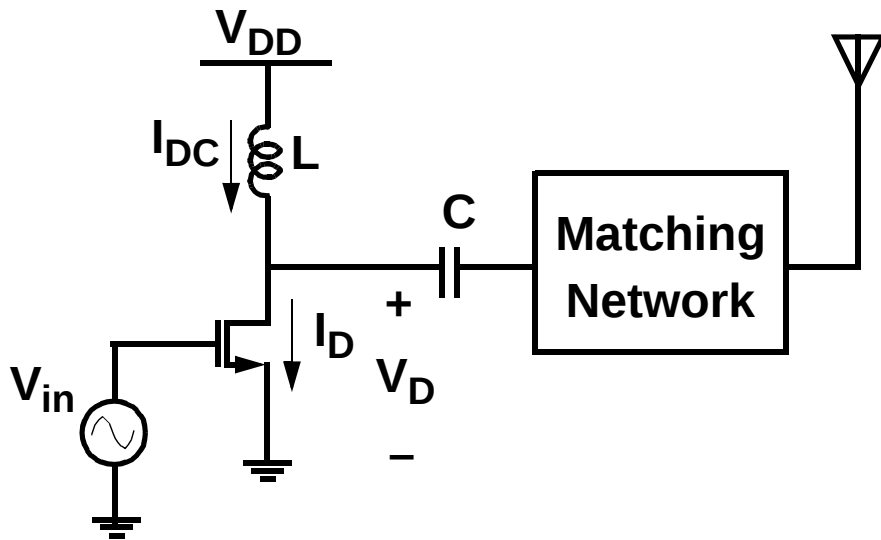
$$P_{supply} = I_{DC} \times V_{DD} = \frac{V_{DD}^2}{R_L}$$

$$\text{Efficiency} = \frac{P_{out}}{P_{supply}} \leq 50\%$$



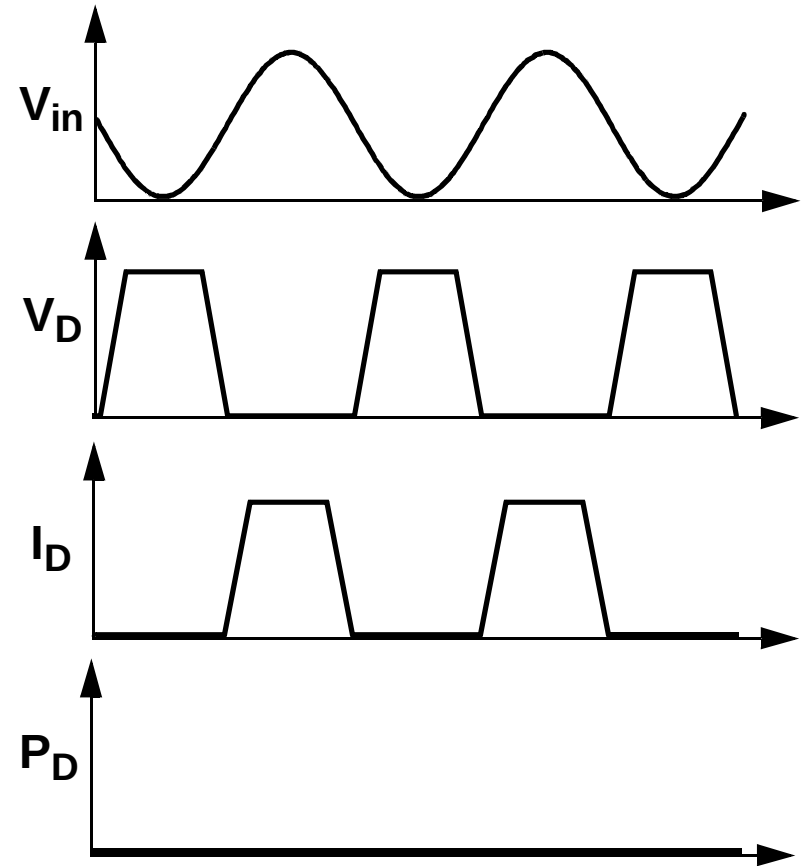
$$P_D = I_D \times V_D \downarrow \Rightarrow \text{Efficiency} \uparrow$$

Efficiency-Linearity Tradeoff



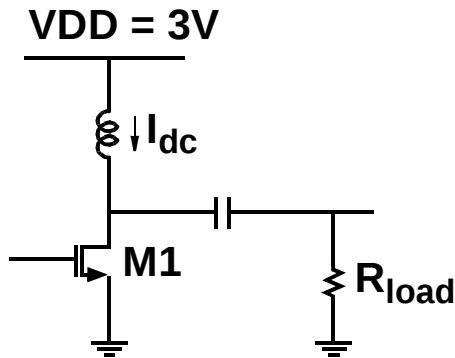
- Large input signal
- Square wave output I_D and V_D
- Non-overlapping I_D and V_D

$$P_{out} = \frac{V_{DD}^2}{R_L}$$



$$P_D = 0 \Rightarrow \text{Efficiency} = 100\%$$

Low-Voltage Operation



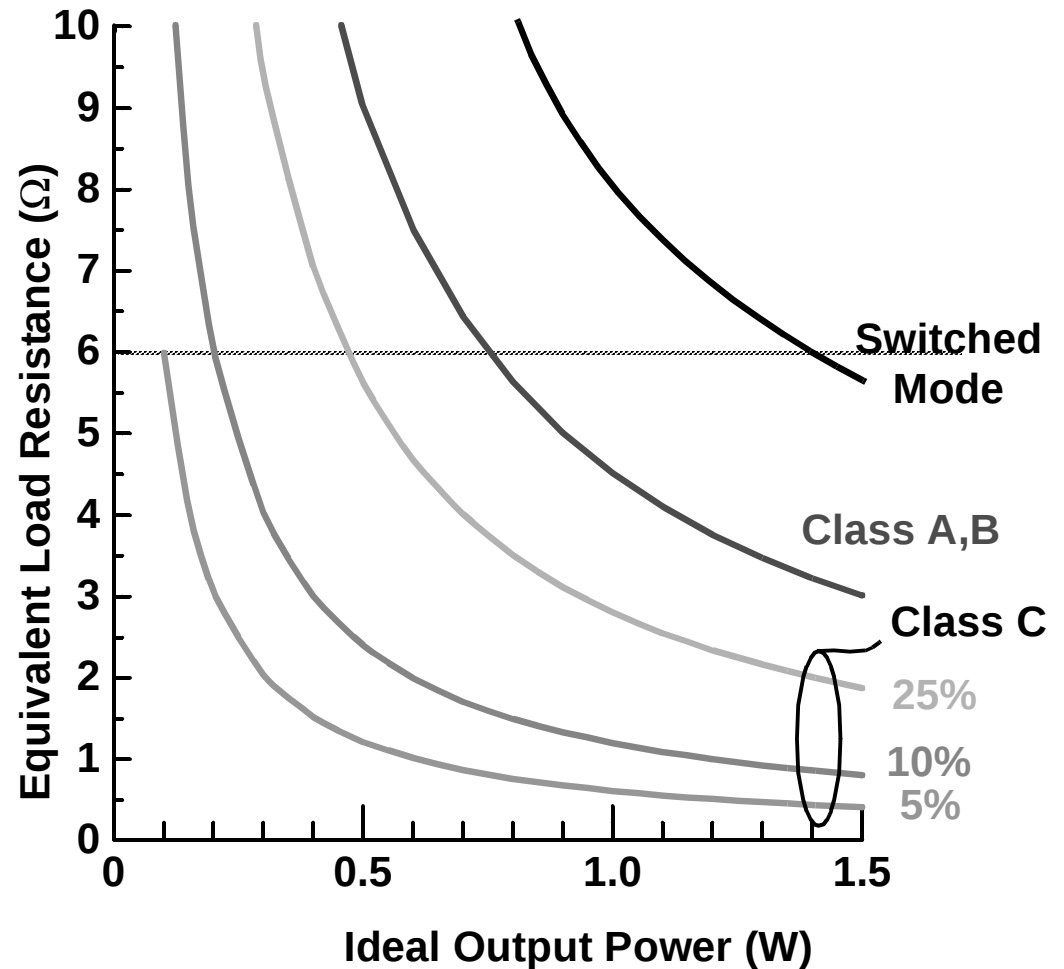
$$P_{out} \approx \frac{VDD^2}{nR_{load}}$$

$$R_{load} \approx \frac{VDD^2}{nP_{out}}$$

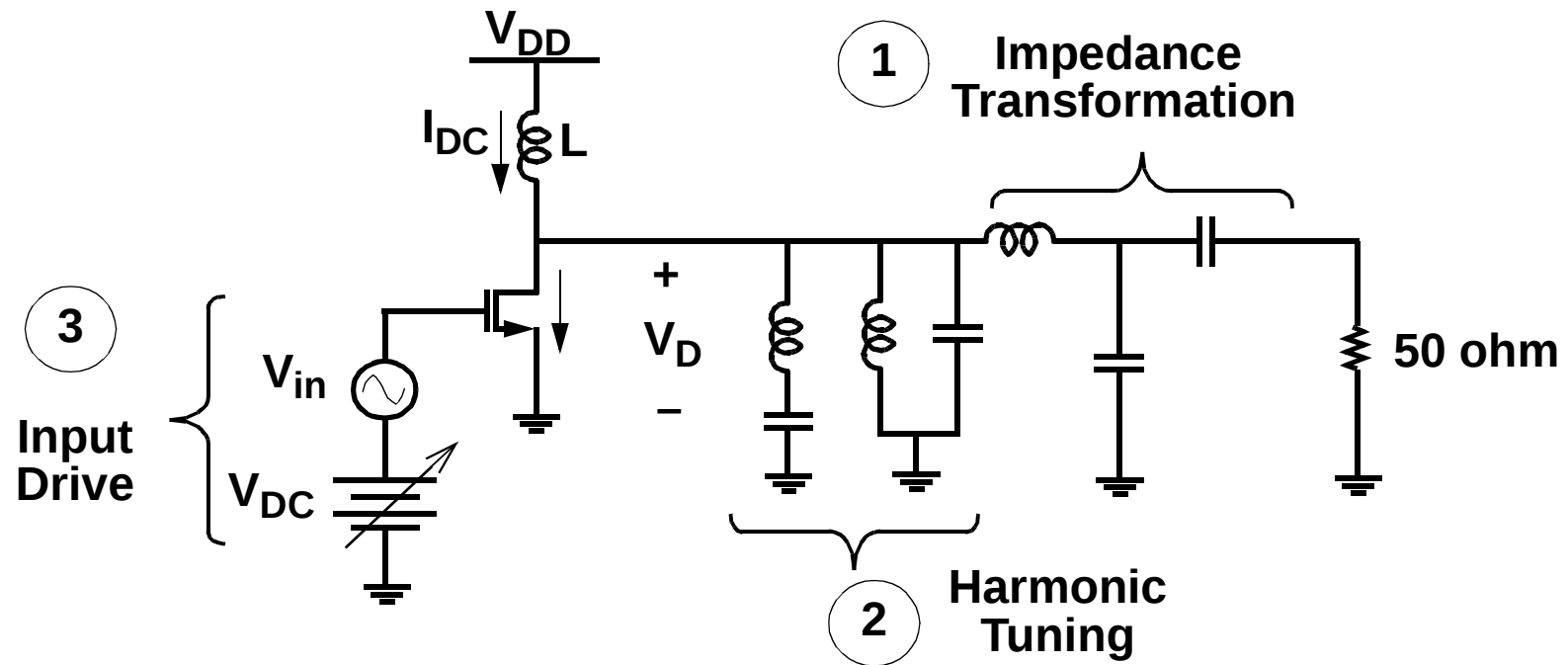
Switched-Mode: $n = 1$

Class A,B: $n = 2$

Class C: $n > 2$



Practical Power Amplifier Design



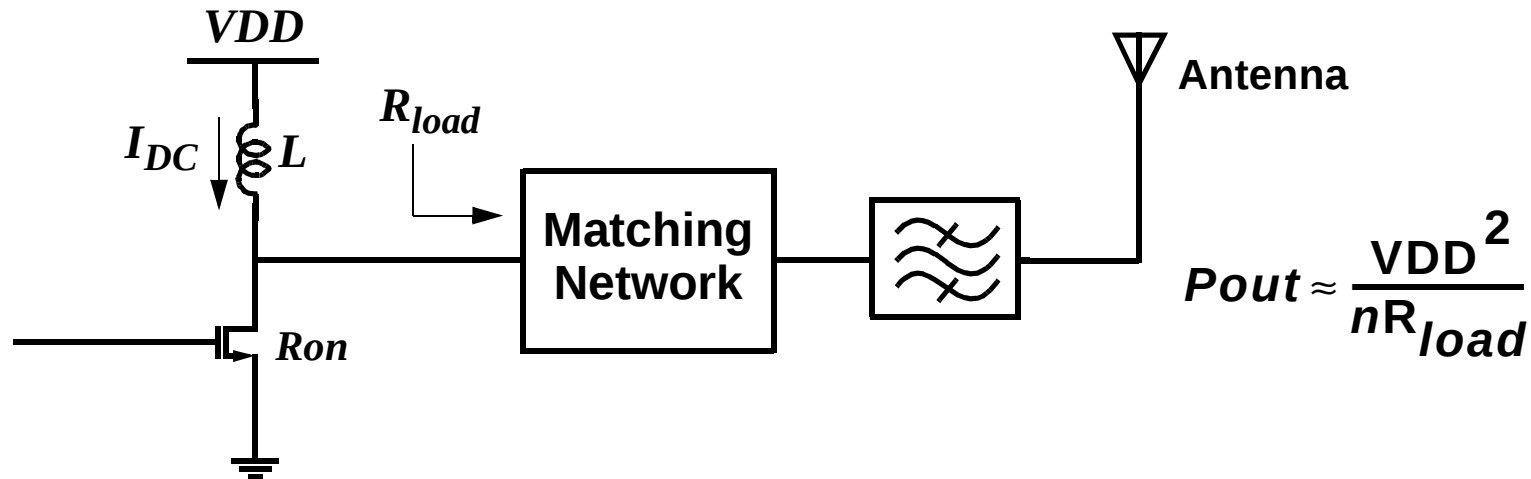
LOAD PULL Optimization

1. Impedance transformation: Output Power
2. Harmonic Tuning: short @ $2f_c$ & open @ $3f_c$ for non-overlap I_D & V_D to maximize efficiency
3. Input drive: V_{DC} $\rightarrow$ Conduction Angle; V_{in} $\rightarrow$ current source vs switch

Nonlinear Power Amplifier

- **Hewlett Packard Labs
(with W. McFarland)**
- **800-MHz 32dBm AMPS PA with 42 %
PAE in 0.8 μm CMOS**

Switched-Mode Design



Choose $n = 1.5$ (assume 67% efficiency due to $R_{on} > 0$),

$VDD = 2.5V$,

For $P_{out} = 1 W$,

$$R_{load} = 4.2 \Omega$$

$$I_{DC} = 0.49A$$

$$R_{on} = 1 \Omega$$

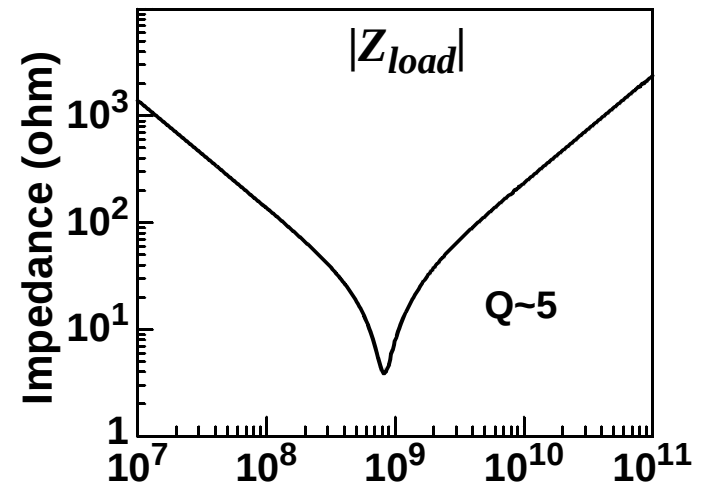
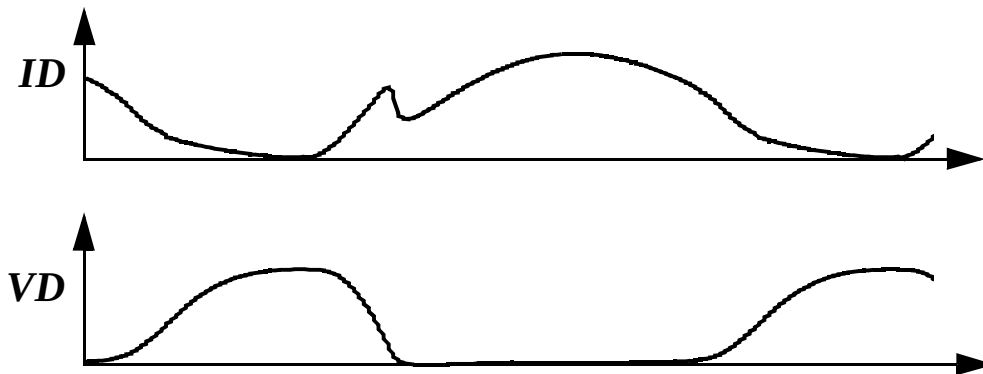
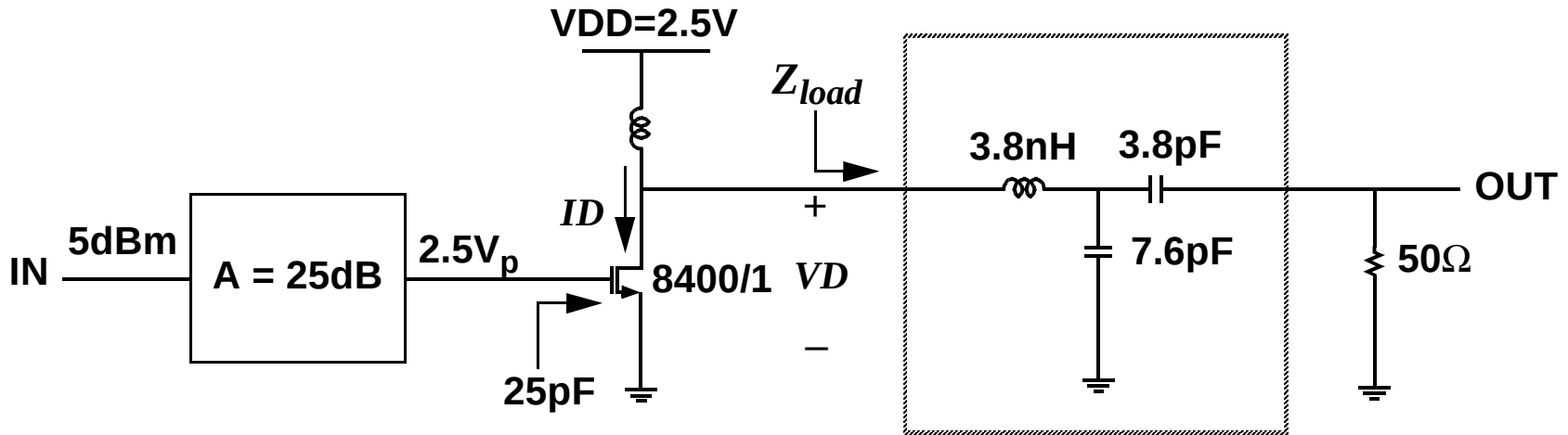
$$[P_{out} = VDD^2 / n R_{load}]$$

$$[I_L \text{ (peak)} = I_{DC} \text{ \& } P_{out} = 0.5 \times I_{DC}^2 \times R_{load}]$$

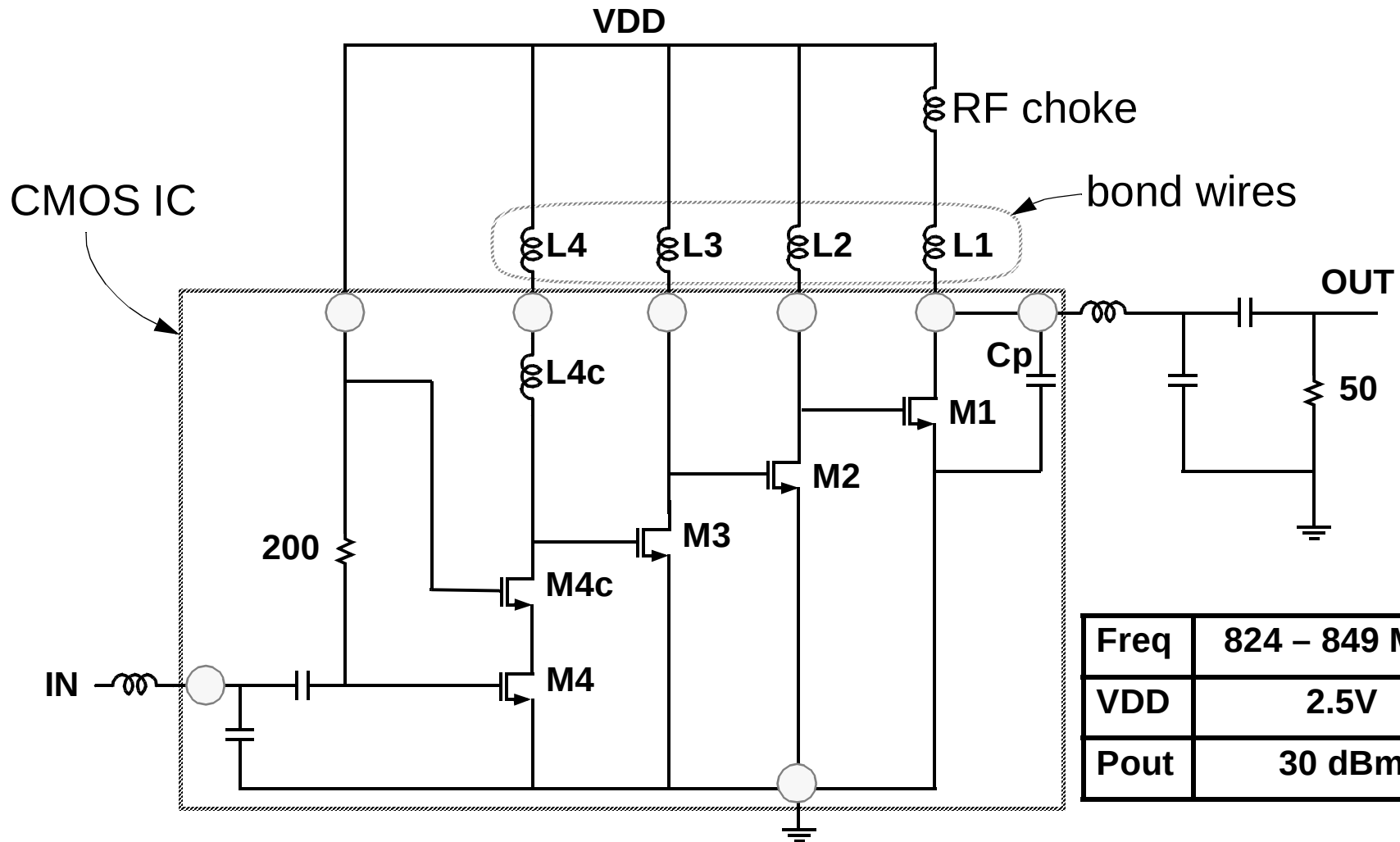
$$[\text{Assume no overlap; } P_D = 0.5W = 0.5 \times (2 I_{DC})^2 \times R_{on}]$$

$\Rightarrow$ Output transistor sizing: $R_{on} < 1 \Omega$

Output Stage Design



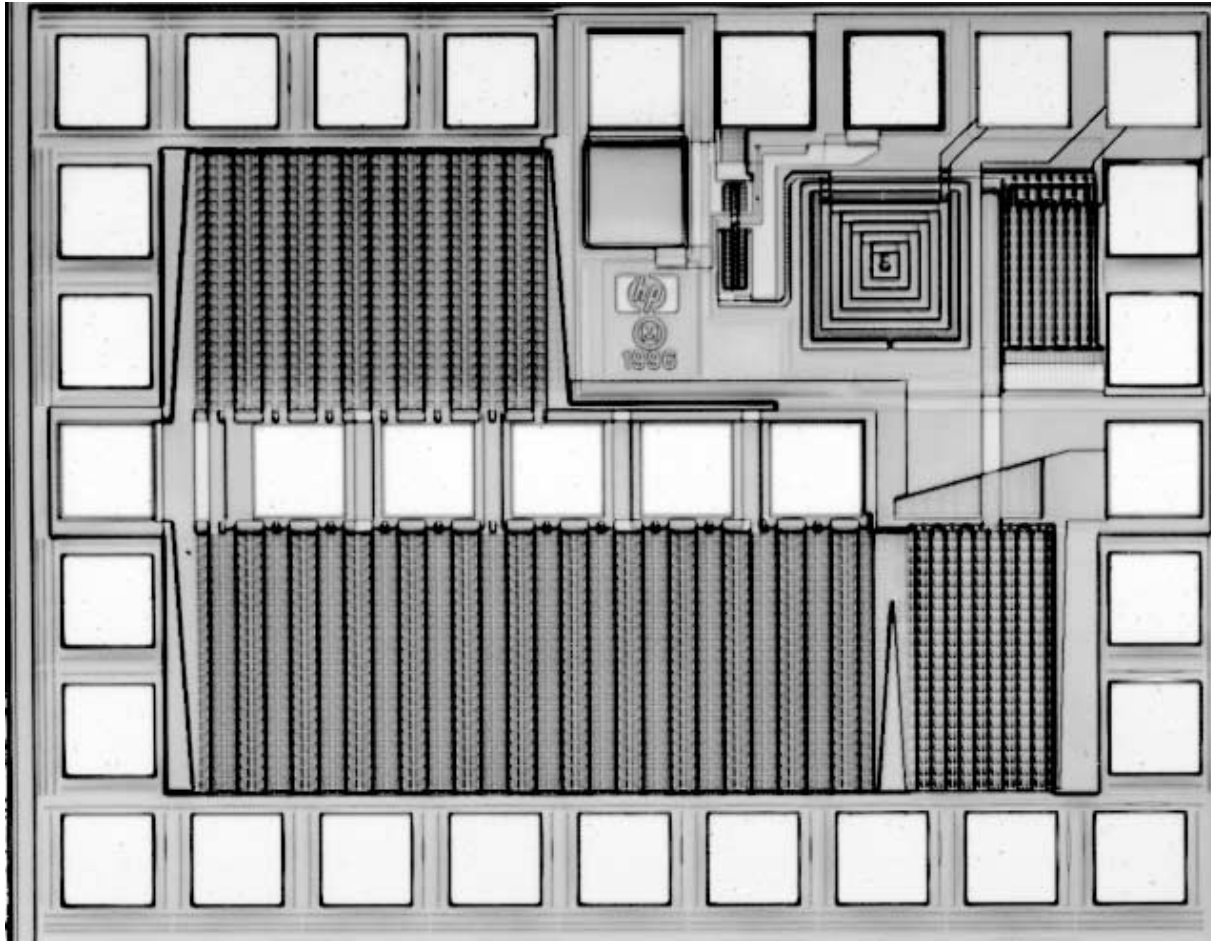
Complete Amplifier



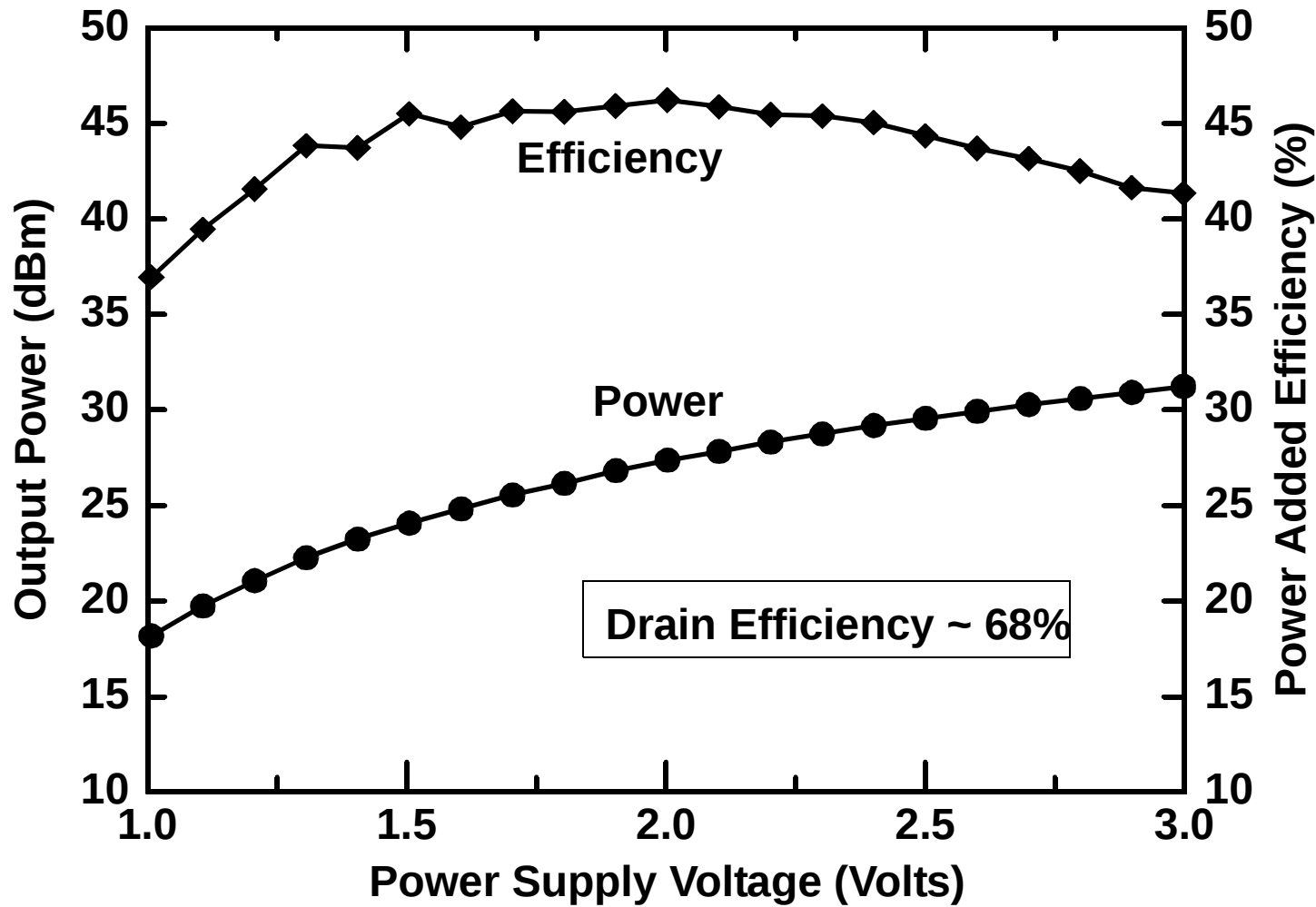
Die Photo

0.8 μ m CMOS

1.5 mm²



Measured P_{OUT} and Efficiency



Linear Power Amplifier

- **Atheros Communications
(with D. Weber et al)**
- **5-GHz 18dBm OFDM PA for IEEE
802.11a in 0.25 μm CMOS**

Spectral-Efficient Modulation

- **64-QAM (Quadrature Amplitude Modulation)**
 - Large signal to noise ratio $> 30\text{dB}$
- **OFDM (Orthogonal Frequency Division Mux)**
 - Large peak to average power ratio of $\sqrt{52}$ or 17dB

→ Requires High Linearity in PA

Power Amplifier Design

- Large peak to average ratio (PAR) of $\sqrt{52}$ or 17dB
- Signal peaks are infrequent: 0.25dB SNR degradation when PAR reduced to 6dB for 16-QAM*.
- Implications:
 - Poor power efficiency
 - With 6dB PAR, to obtain 40mW (16dBm) requires Psat of ~22dBm or 160mW
 - With 17dB PAR, to obtain 40mW (16dBm) requires Psat of ~33dBm or 2W

*Van Nee & Prasad, OFDM for Wireless Multimedia Communications, Artech House, 2000

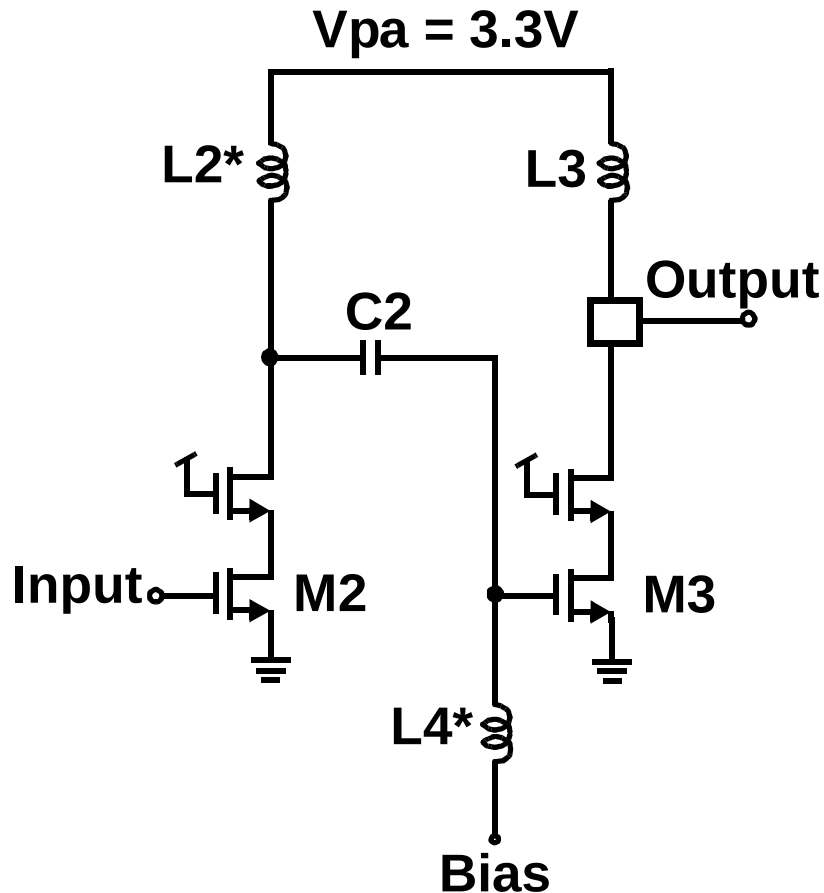
Linear PA makes efficient radios

- **Frequency bandwidth is precious**
--> Maximize network capacity
- **Energy/bit (battery life)**
More bits sent per second
--> PA + the rest of the radio
are ON for shorter duration

Linear PA Design

- **Input load impedance**
 - signal dependency
 - cascode
- **V_{GS} overdrive**
 - dc bias with capacitive level-shift
- **Output load impedance**
 - impedance matching network
- **Stability**
 - cascode

Power Amplifier Topology

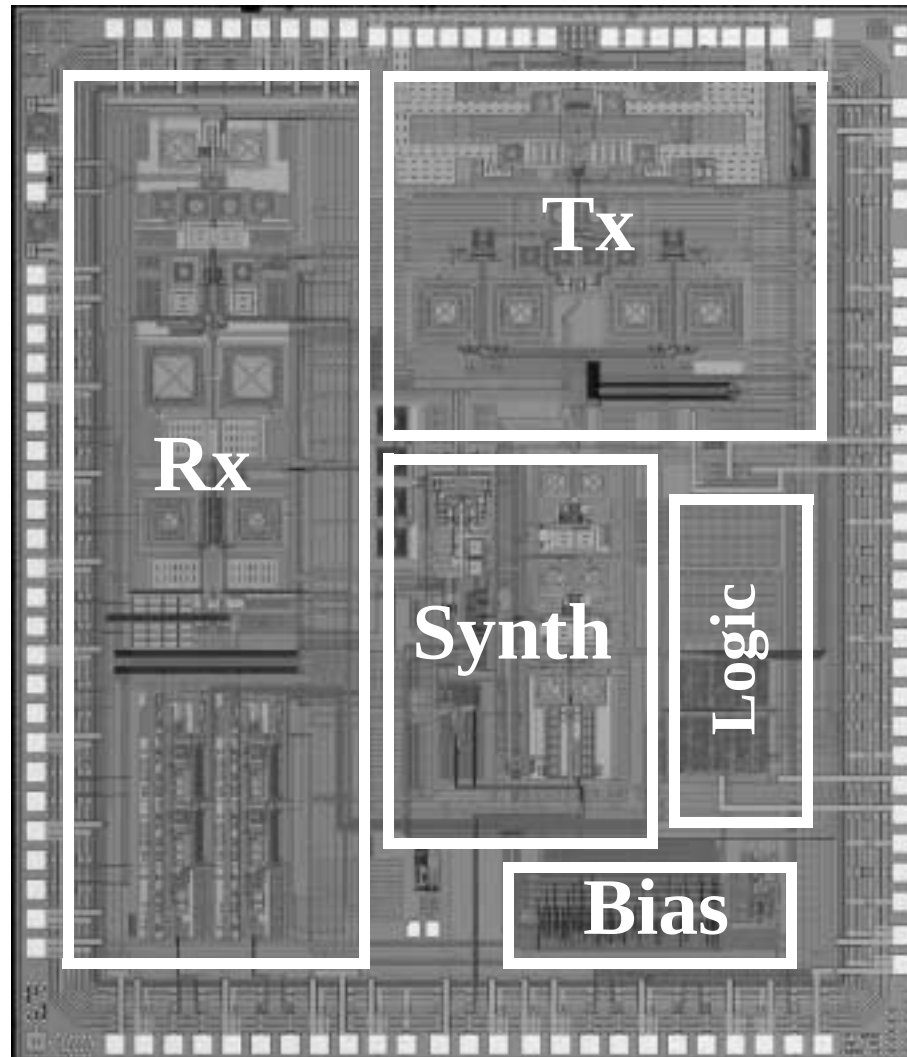


- Class A operation
- Cascoded
 - 3.3V supply voltage
 - Stability
- Capacitive Level-shift
 - Metal-2,3,4,5 stacks
- Inductive loads
- Differential
 - Off-chip balun

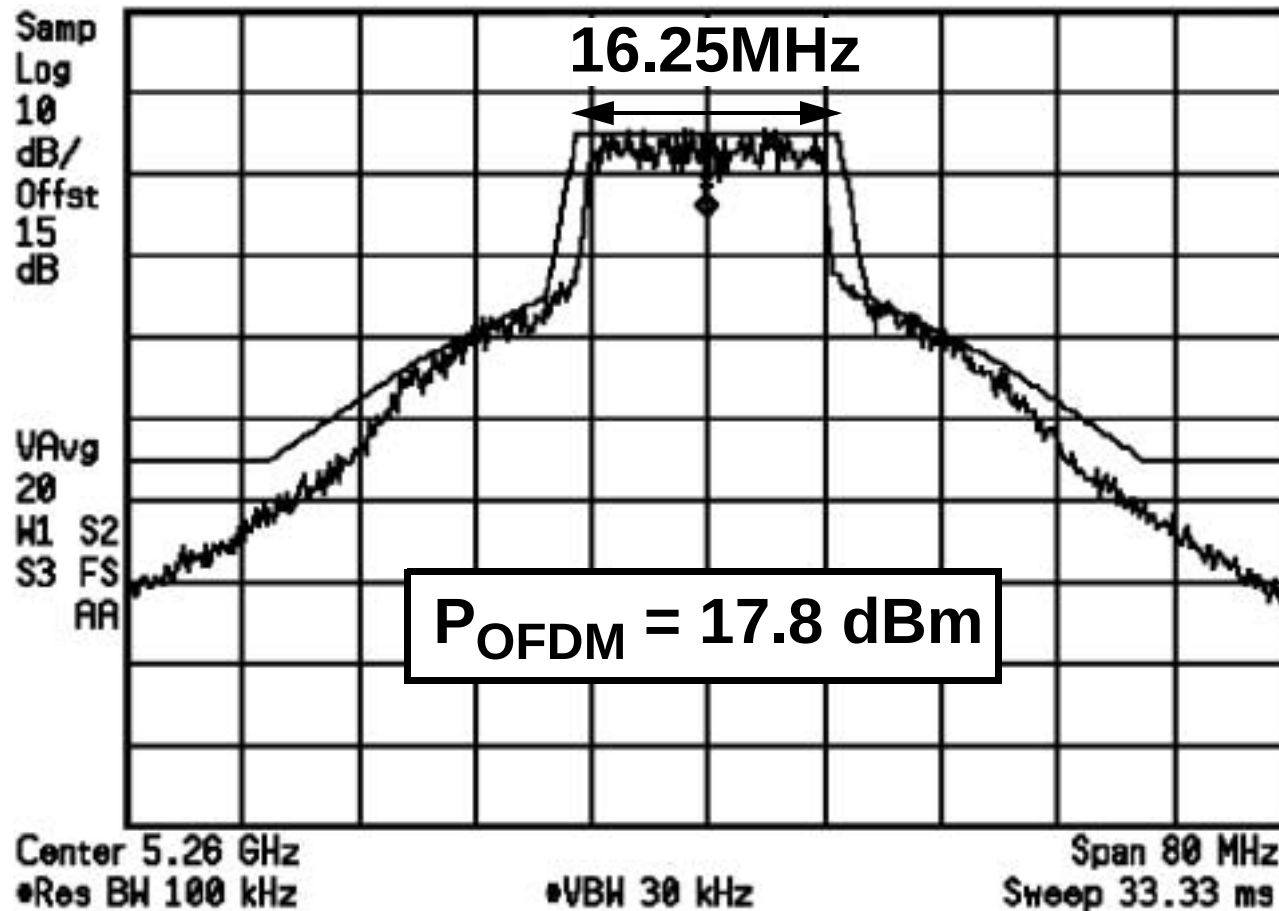
* C.P. Yue and S.S. Wong, IEEE JSSC, May 1998

Nov 2002

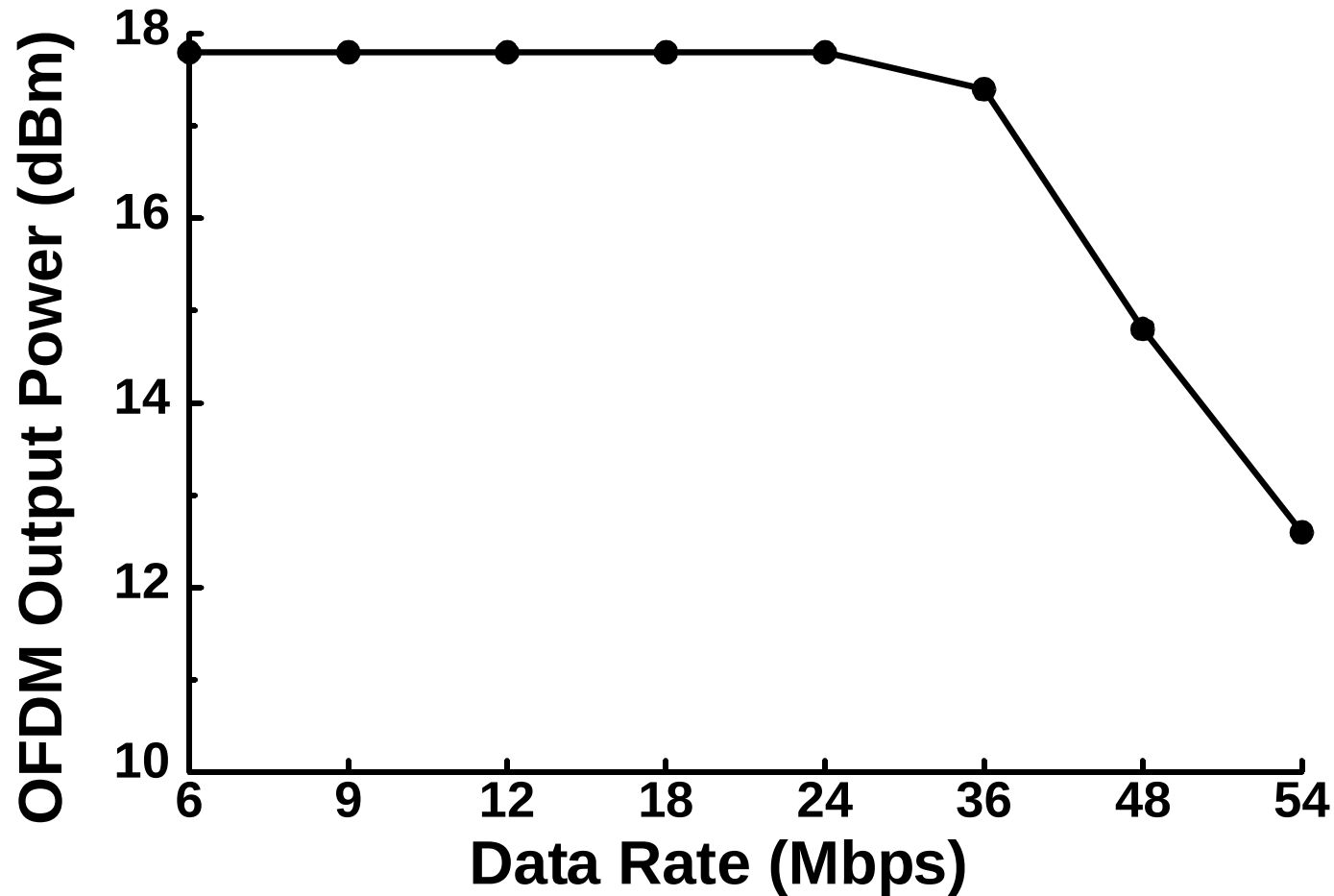
Die Photograph



Measured BPSK OFDM Spectrum



Measured Transmit Output Power



Linearized Power Amplification

- **Hewlett Packard Labs
(with W. McFarland)**
- **Linearization IC for NADC with
efficiency improvement from 36% to
49% using envelope elimination and
restoration**

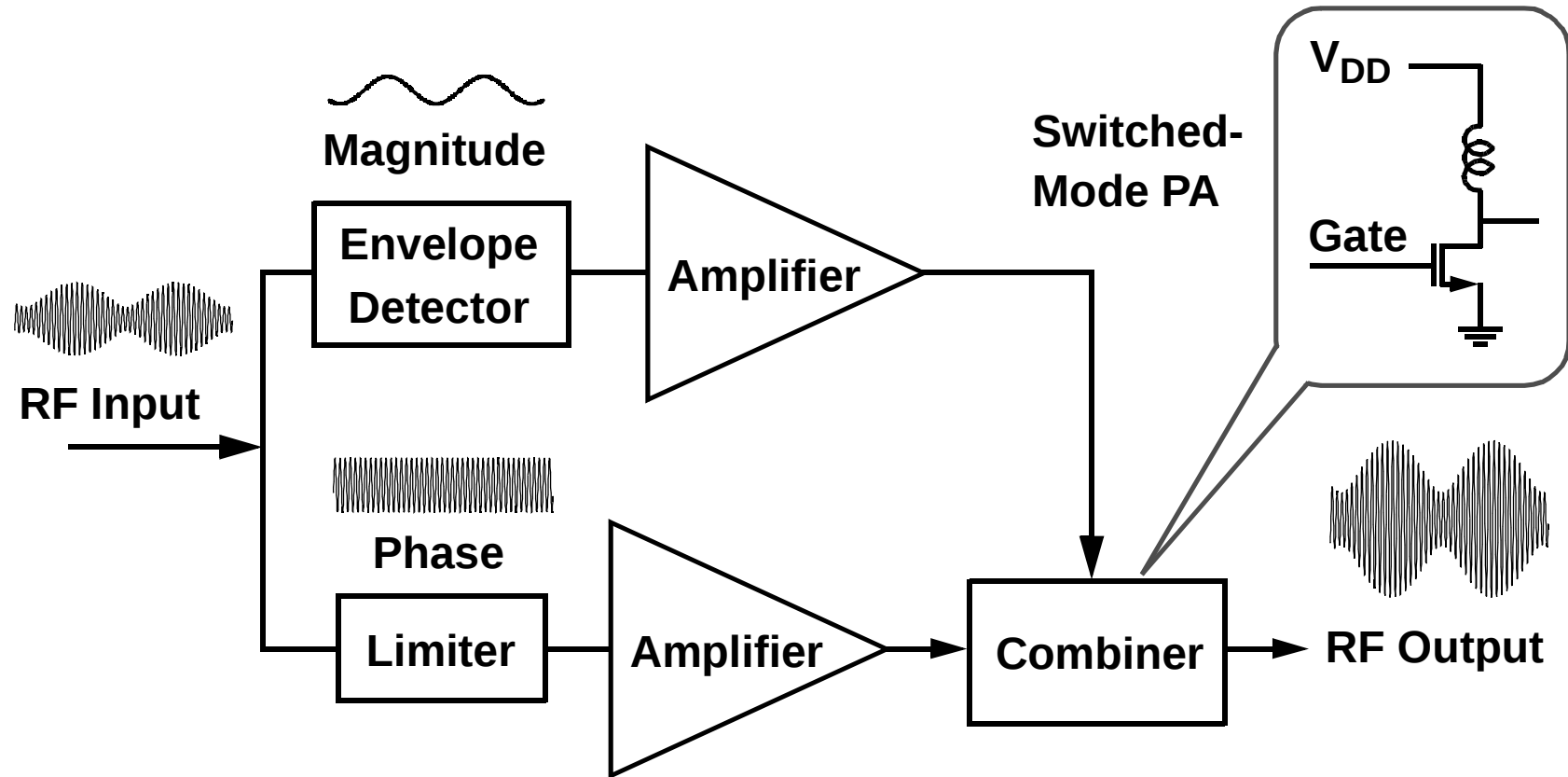
Applying Integration to RF PA

Transistors are *cheap*.

- **LARGE Output Power:** Use switched-mode output stage
- **HIGH Efficiency:** Use switched-mode output stage
- **GOOD Linearity:** Use linearization circuits so that the output stage does not need to be linear.

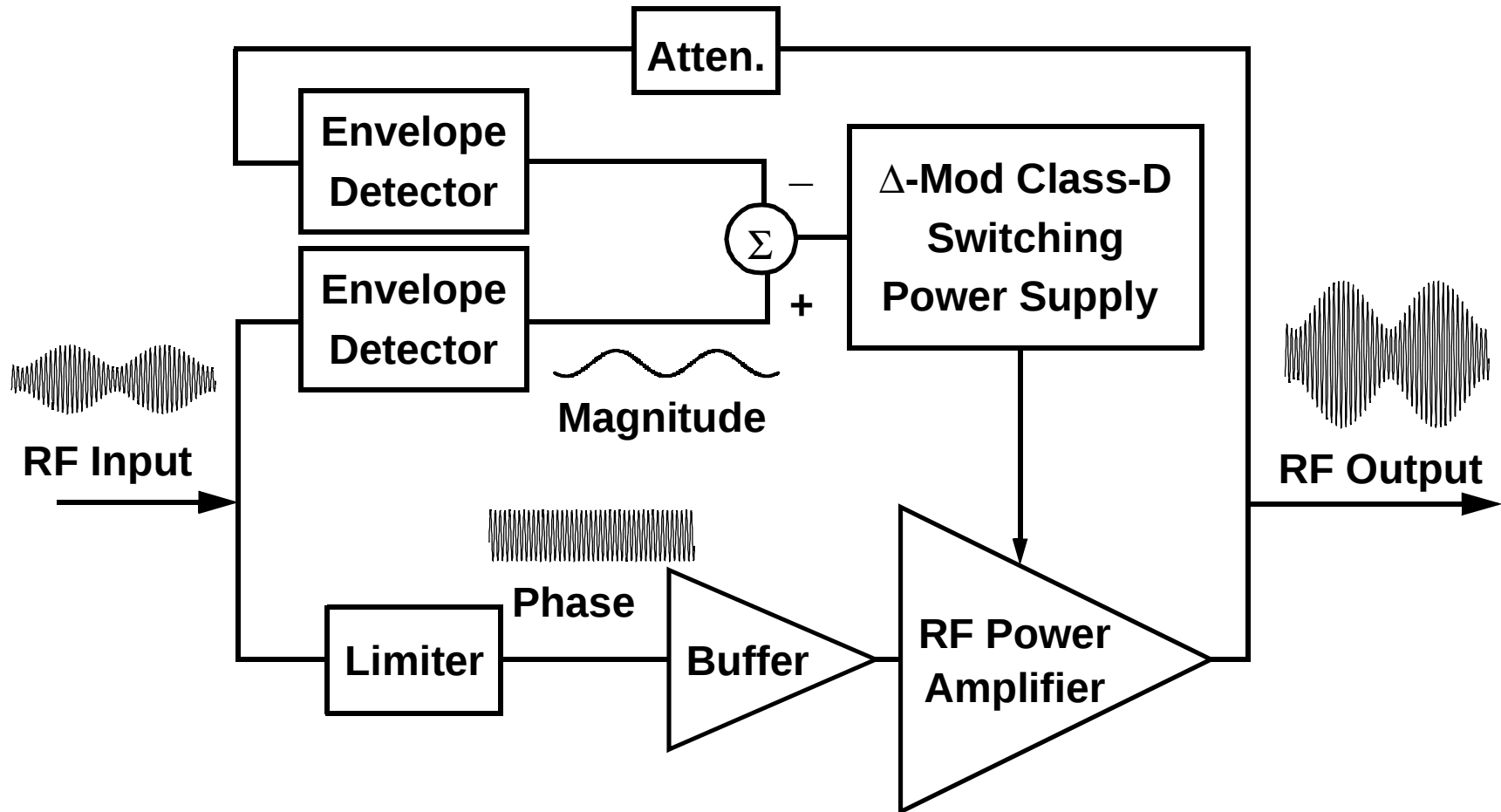
**SOLUTION: Switched-mode output stage
+ linearization.**

Envelope Elimination and Restoration

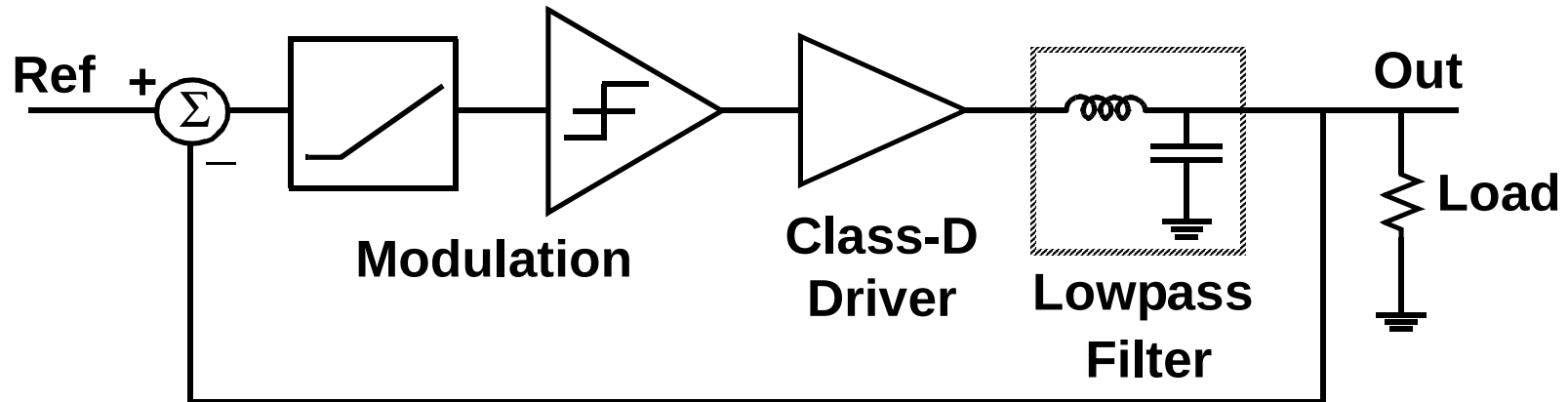


Ref: L. Kahn, Proc IRE, July 1952

Closed-Loop EER Implementation

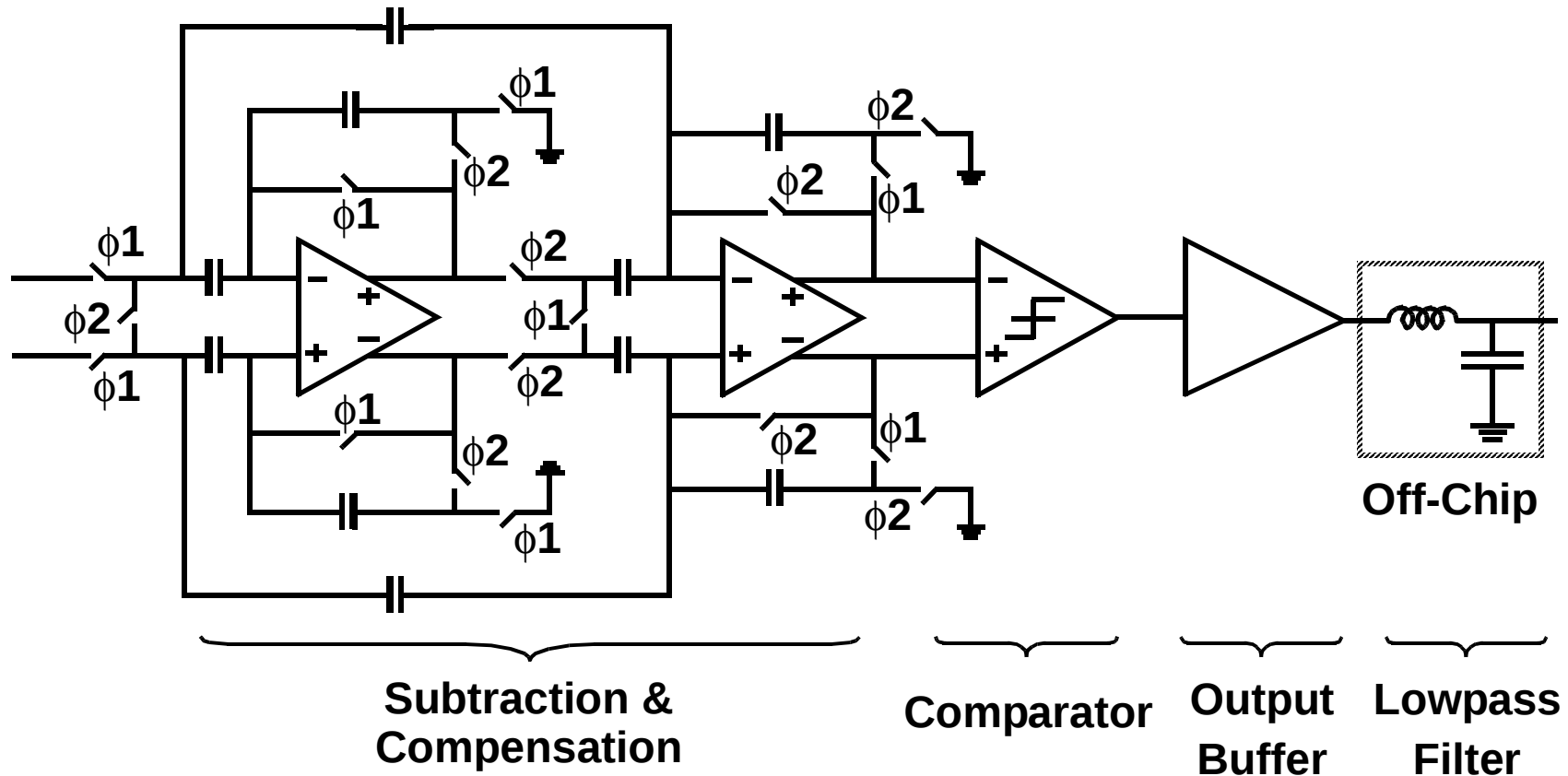


Δ -Modulated Switching Power Supply

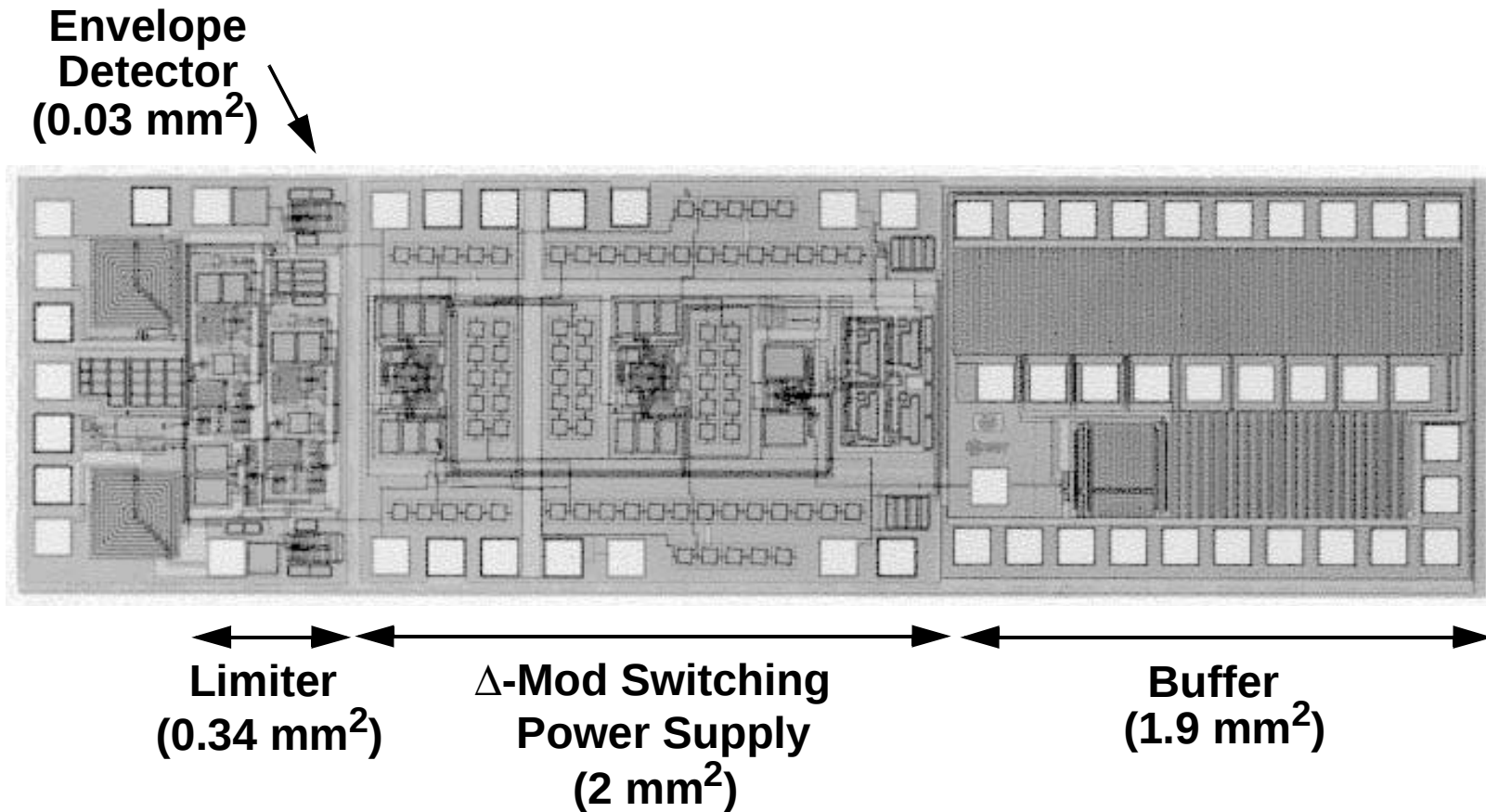


- Closed-loop system
- Modulation to generate a two-level output
 $\Rightarrow$ Pulse width modulation vs. Delta modulation
- Efficient Class-D driver

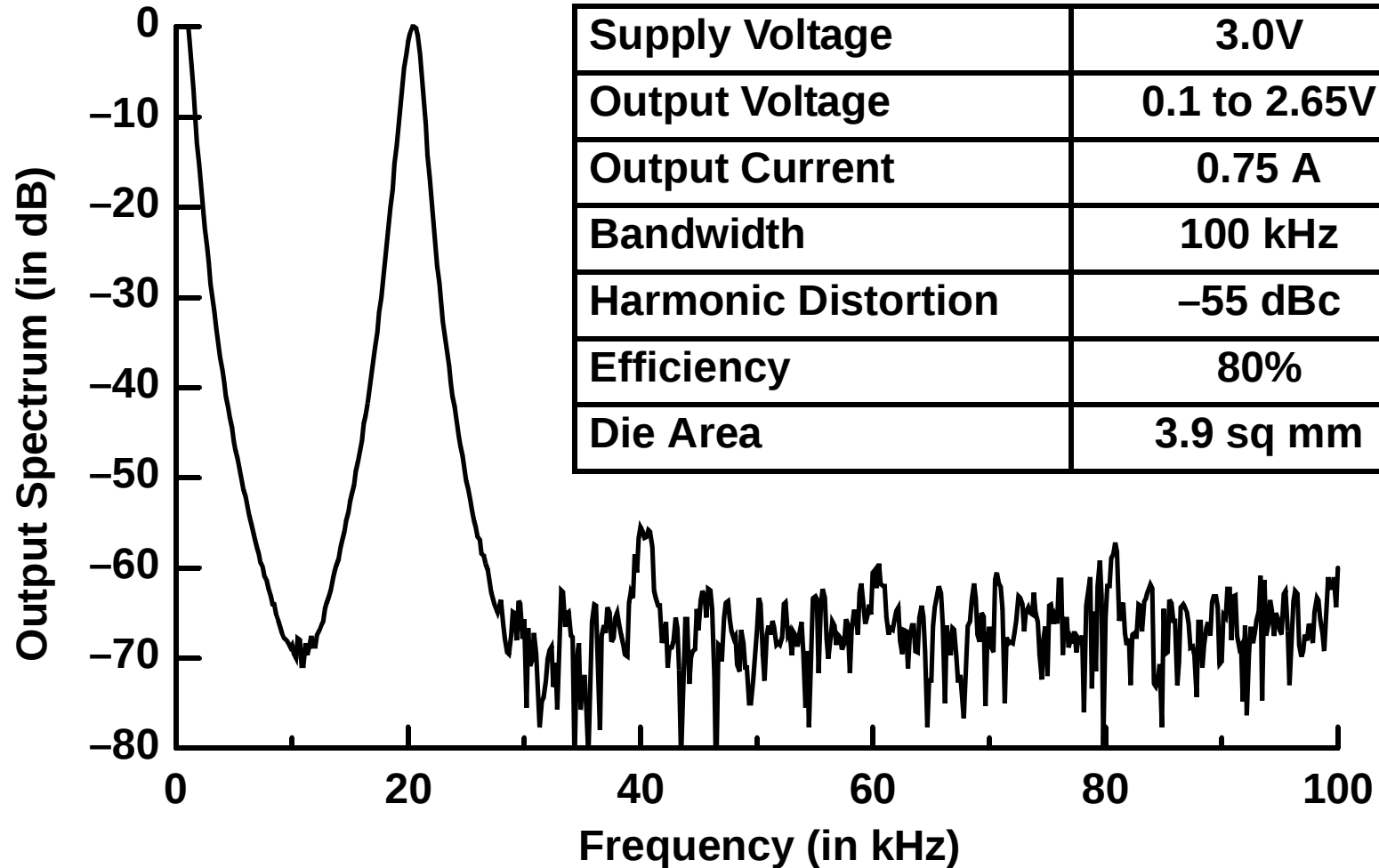
Switched-cap Circuit for Δ Modulation



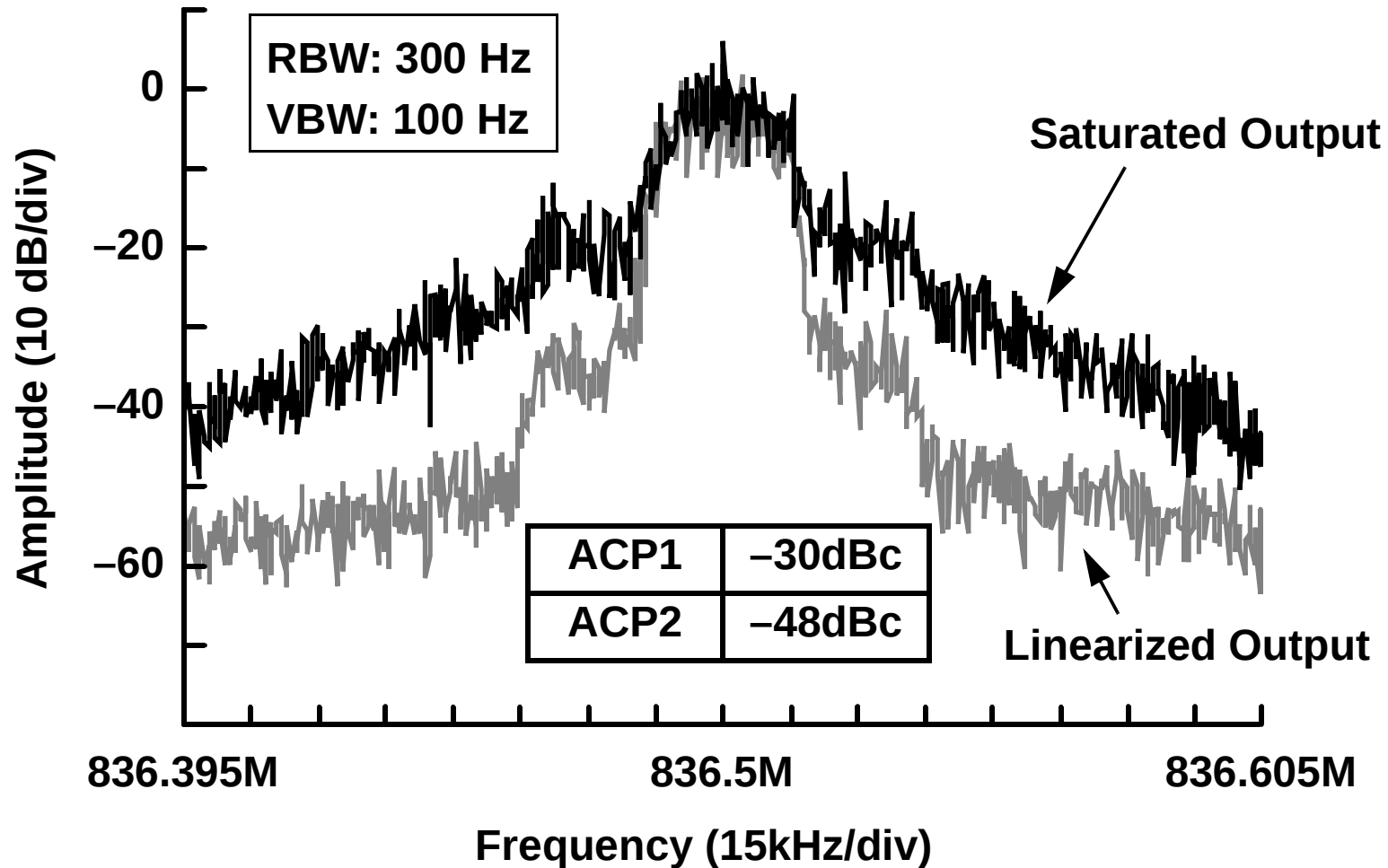
Die Photograph



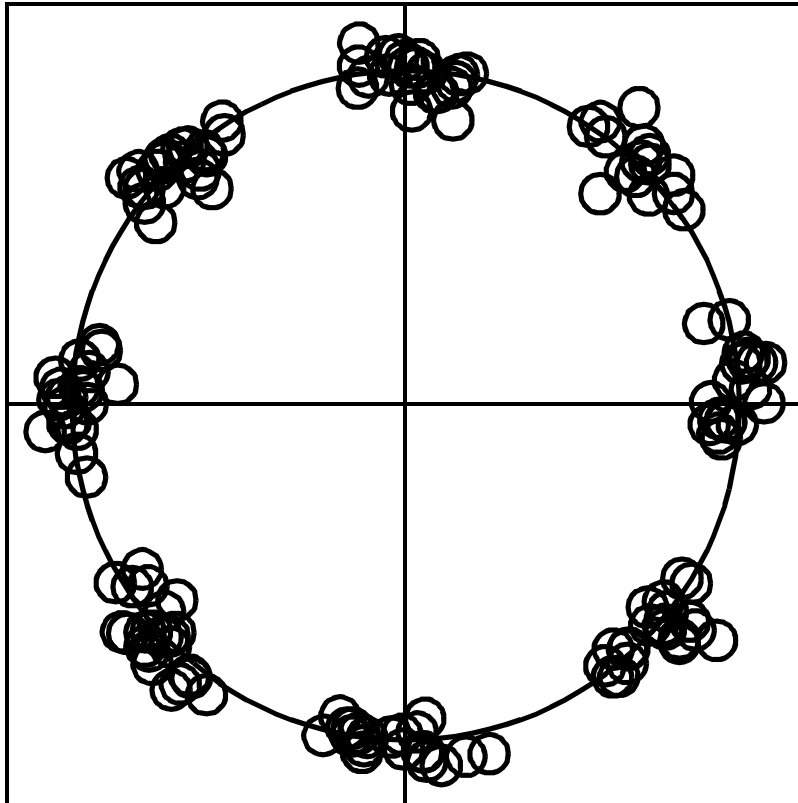
Switching Power Supply



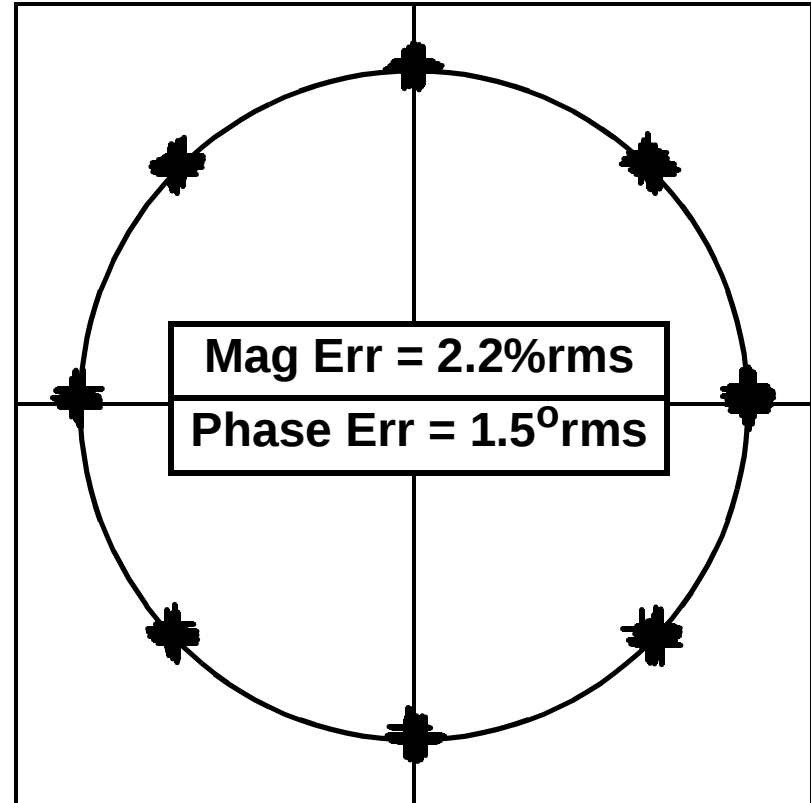
Spectral Mask of CMOS PA



$\pi/4$ QPSK Constellation of CMOS PA

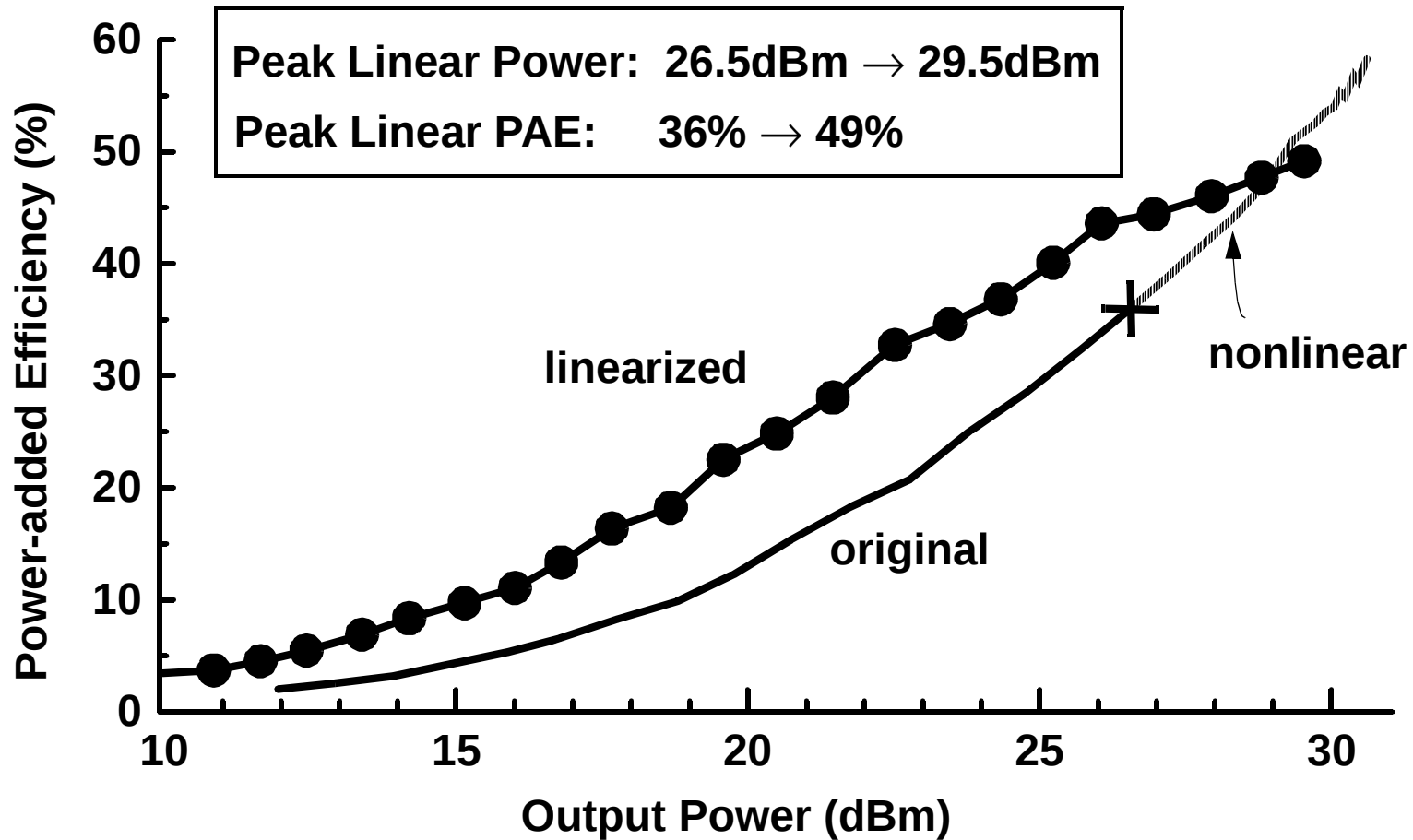


Without Linearization



With Linearization

Efficiency of 4.8-V GaAs PA



Conclusion

- **Nonlinear (switched-mode) PA provides**
(+) large output power and high efficiency
(-) poor linearity
- **Linear PA provides**
(+) linearity, spectral efficiency
(-) poor efficiency
- **Linearization using envelope elimination and restoration**
(+) linear RF output + high efficiency
(-) implementation complexity

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课程网址: <http://www.edatop.com/peixun/ads/13.html>



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