# Innofidei Integrated CMMB Receiver IF206

## Datasheet

Version 1.0.0
June, 2010

**Innofidei Inc.**
Address: 8/F, Tower A, Tsinghua Science Park
No.1, Zhongguancun East Road, Haidian district
Beijing, 100084
People's Republic of China
Website: *http://www.innofidei.com*

# Warning

# Ordering Information

| Ordering part number | Description | Package |
|---|---|---|
| IF206-49 | Innofidei Integrated CMMB Receiver IF206 | TFBGA-49 |
| | | |

# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0.0 | 2010.06.30 | Initial version |

# Table of Contents

# List of Figures

# List of Tables

# 1 Overview

This chapter gives a generaldescription on Innofidei Integrated CMMB Receiver IF206.

## Topics

# 1.1 Overview

Innofidei Integrated CMMB Receiver IF206 (IF206 for short) is the second generation of Innofidei's highly integrated single-chip CMMB receiver for China Mobile Multimedia Broadcast (CMMB) system. It combines an RF U-band tuner and a demodulator into a single 5×5mm package. IF206 provides superior mobile performance with very low power consumption. With its high level of integration, IF206 saves PCB board space and enables system manufacturers to significantly reduce the number of the discrete components used. IF206 is ideal for devices such as mobile phones with TD-SCDMA and CMMB functions, data cards, PCI-E module, and so on.

IF206 further optimizes the CMMB receiver architecture over its previous generation, yielding a much compact footprint and better performance. Its 5×5mm package, the smallest in the industry, reduces the overall BOM. The ultra-low power consumption design and the efficient power management decreases power consumption significantly.

# 1.2 IF206 Application

IF206 can be used in:

- Mobile multimedia terminals
- Cellular phones and PDAs
- Ultra mobile personal computers (UMPCs)
- Mobile Internet devices (MIDs)
- Notebook
- USB dongles

# 1.3 IF206 Key Features

- Compliant with CMMB standard GY/T 220.1-2006 and GY/T 220.2-2006
- Integrated conditional access (CA) descrambling
- Compliant with CMCC standard: Terminal Specification for Mobile Multimedia Broadcast/Mobile TV Service
- Ultra-low power consumption and smart power management
- 5x5mm BGA package with 0.65mm ball patch
- Covering the entire UHF band (470MHz to 860MHz)
- AGC dynamic range from -102 to 0dBm
- Superior sensitivity and mobility while on the go
- Superior interference suppression capability to ease RF system design

- SPI/SDIO interface (slave mode) for data/command transfer and firmware downloading
- Supporting simultaneous reception of multiple services

## 1.4 A Typical IF206 Application

*Figure 1-1* shows the way how IF206 is used in a mobile device system.

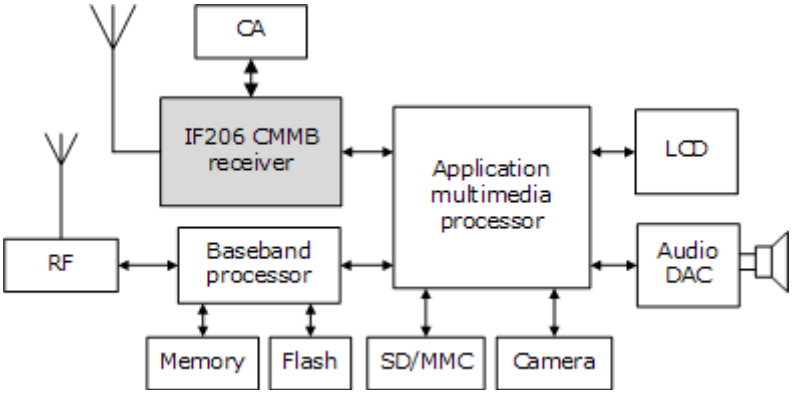



**Figure 1-1** IF206 in a mobile device system

# 2 IF206 Pin Description

This chapter describes how pins of IF206 are assigned. It also gives the pin description.

## Topics

# 2.1 IF206 Pin Assignment (Top View)

*Figure 2-1* shows IF206 pin assignment (TFBGA-49).

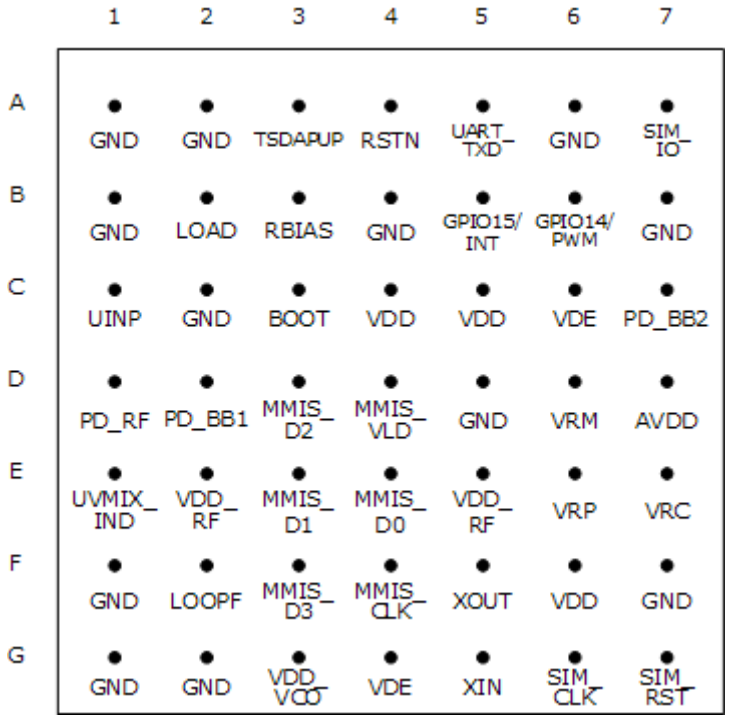



**Figure 2-1** IF206 pin assignment

# 2.2 IF206 Pin Description

*Table 2-1* describes the pins of IF206.

**Table 2-1** IF206 pin description

| Pin name | Pin ID | IO type | Description |
|---|---|---|---|
| XIN | G5 | Crystal input | Clock input |
| XOUT | F5 | Output | Clock output |
| RSTN | A4 | Input | Reset input |
| GPIO14/PWM | B6 | Pull-up I/O, 4mA drive | General purpose IO/PWM output |
| GPIO15/INT | B5 | Pull-up I/O, 4mA drive | General purpose IO/Data ready interrupt |
| MMIS_CLK | F4 | Pull-up I/O, 4ma drive strength | Clock input, which can be used in the SPI/SDIO mode. |

**Table 2-1** IF206 pin description (continued)

| Pin name | Pin ID | IO type | Description |
|---|---|---|---|
| MMIS_VLD | D4 | Pull-up I/O, 4mA drive strength | Data input in SPI mode 2, CMD line in SDIO mode |
| MMIS_D0 | E4 | Pull-up I/O, 4mA drive strength | data bit0, data output in SPI mode 2, data line in SDIO mode |
| MMIS_D1 | E3 | Pull-up I/O, 4mA drive strength | Data bit1, data line in SDIO mode |
| MMIS_D2 | D3 | Pull-up I/O, 4mA drive strength | Data bit2, data line in SDIO mode |
| MMIS_D3 | F3 | Pull-up I/O, 4mA drive strength | Data bit3, chip select in SPI mode 2, data line in SDIO mode |
| VRP | E6 | Analog output | ADC reference output |
| VRM | D6 | Analog output | ADC reference output |
| VRC | E7 | Analog output | ADC reference output |
| TSDAPUP | A3 | Digital input | A 10kohm pull-up resistor is required. |
| BOOT | C3 | Digital input | Power-on latch.<br>• 1: SDIO;<br>• 0: SPI |
| UART_TXD | A5 | Digital output | UART output for debug |
| SIM_IO | A7 | Digital I/O | ISO7816 data |
| SIM_CLK | G6 | Digital output | ISO7816 clock |
| SIM_RST | G7 | Digital output | ISO7816 reset |
| AVDD | D7 | Analog power | Analog power for demodulation block |
| VDD | C4, C5, F6 | Power | Power for the demodulation core |
| VDE | C6, G4 | Power | Power for the demodulation IO |
| LOOPF | F2 | Analog input | External loop filter. All of the components shall connect to this pin as close as possible. |
| PD_BB1 | D2 | RF signal | RF output detector |
| UVMIXIND | E1 | RF signal | RF mixer input, which needs to connect to GND through an inductor. |
| LOAD | B2 | RF signal | Load inductor for LNA |
| RBIAS | B3 | RF signal | Bias current setting resistor, which needs to be grounded through a 30kohm (±1%) resistor. |
| UINP | C1 | RF signal input | U band RF signal input |
| PD_BB2 | C7 | RF signal | RF output detector |
| PD_RF | D1 | RF signal | RF peak output detector |

**Table 2-1** IF206 pin description (continued)

| Pin name | Pin ID | IO type | Description |
|---|---|---|---|
| VDDRF | E2, E5 | RF power | RF power input for RF block |
| VDDVCO | G3 | RF power | VCO power (1.8 V). This pin shall be decoupled with a high-quality bypass circuit. |
| GND | A1, A2, A6, B1, B4, C2, D5, F1, G1, G2, B7, F7 | Ground | The chip shall be well grounded. |

# 3 Function Specification

This chapter describes the functions IF206 provides.

## Topics

# 3.1 IF206 Specification

## 3.1.1 Supporting All RF Signals within the UHF Band

- Supported RF frequency range: 470MHz to 860MHz
- RF input impedance required: 50ohm
- Input VSWR: lower than 2:1
- Typical noise figure: 3.5dB
- Typical OIIP3: -4dBm
- Maximum baseband cut-off frequency: 5.5MHz
- Stop band attenuation: 55dBc
- Phase noise (SSB@10KHz): -90dBc

## 3.1.2 CMMB Standard Options Supported

- Flexible 25 ms time slot (TS) assignments
- BPSK/QPSK/QAM16 constellations
- Inner block de-interleave
- Rate 1/2 and 3/4 LDPC decoder
- Outer block de-interleave mode 1, mode 2, and mode 3
- Triple-rate Reed-Solomon decoder

## 3.1.3 Interface

IF206 interfaces can serve as different interfaces in different modes, as listed below.

- SPI interface: two-wire mode and four-wire mode supported
- SDIO interface: conforming to SDIO specification verison 2.0 (based on SDIO function 1. See section *5.5 SDIO Interface* for related information.)

## 3.1.4 Built-in CA Descrambling

IF206 is compliant with CMMB GY/T 220.6 and implements the functiuon of de-crambling through the integrated CA library and external CA chip.

The format of output stream is compliant with the CMMB GY/T 220.2 standard.

# 3.2 IF206 Power Control

## 3.2.1 Operation States and the RSTN Pin

IF206 can be in one of these two modes:

- Normal
- Power down

The RSTN pin determines the operation state of the chip. When the pin is put low, the chip enters the power down mode; when the pin is high and then the firmware is loaded, the chip returns to the normal work mode.

## 3.2.2 Power Domain

The WAKEUP pin is only for debug and is not used in normal work mode. Tie this pin to a fixed level (such as GND or VDDIO) in actual use. IF206 can enter into the power-saving mode in 2us and wake up from the power down mode within 10ms. When IF206 wakes up from the power down mode, the firmware needs to be reloaded.

# 3.3 SPI Interface

SPI interface is used for communications between MCU and internal hardware transferring engine through Serial Peripheral Interface (SPI) connecting to a host (AP). This section describes the hardware interface protocol and its command set.

The hardware interface is fully compatible with the conventional SPI (as shown in *Figure 3-1*). In the SPI mode, the maximum frequency of the SPI clock is 10MHz (the default is 7MHz). IF206 can only operate in the SPI slave mode.

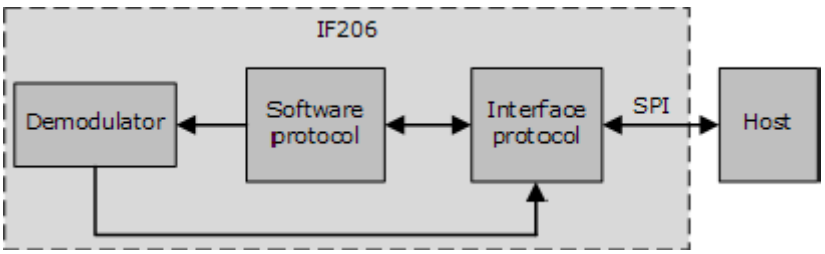



**Figure 3-1** SPI/SDIO protocol layer

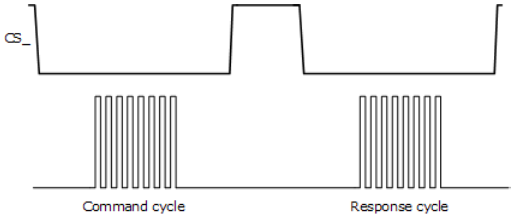



**Figure 3-2** Typical SPI operation timing: type 1

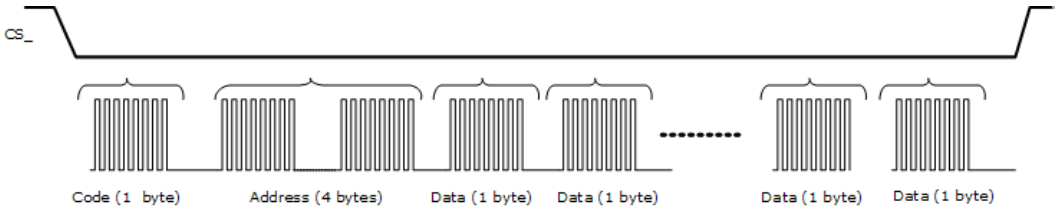



**Figure 3-3** Typical SPI operation timing: type 2

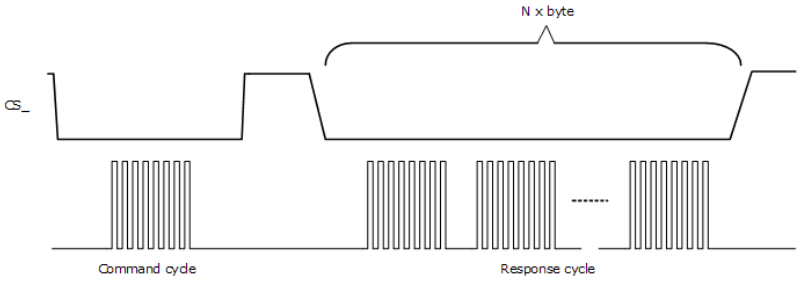



**Figure 3-4** Typical SPI operation timing: type 4

The SPI physical interface on the host side is fully compatible with standard SPI. *Table 3-1* lists the mapping relation between all SPI modes and IF206 pins.

**Table 3-1** Signal mapping of SPI interface

| SPI Mode 2 | | |
|---|---|---|
| **Pin name** | **Direction** | **SPI signal** |
| MMIS_CLK | Input from host | SPI clock |
| MMIS_VLD | Input from host | Data line-in |
| MMIS_D0 | Output to host | Data line-out |
| MMIS_D3 | Input from host | Chip select |

**Note:**

- When MMIS_D3 is de-asserted, all pads are in the high-Z state.
- The signals listed in *Table 3-1* apply to SPI timing type 1, 2, and 4.

### 3.3.1 SPI Write-Register Process (Type 1/4)

Each SPI write-register process contains two cycles: the command cycle and the

data cycle. Commands and data are transferred in octets. When MMIS_D3 is asserted, IF206 receives commands in command cycles and obtains write-register contents in data cycles.

In type 4, the number of the bytes to be transmitted is specified by the command.

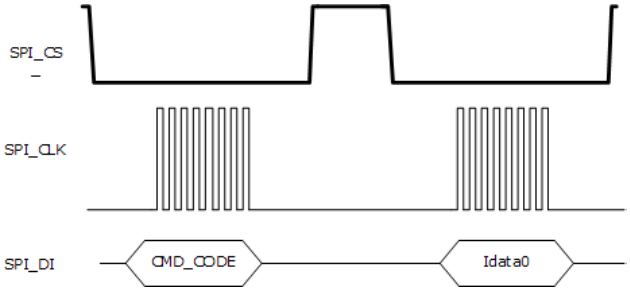



**Figure 3-5** SPI host-writing-register timing: type 1

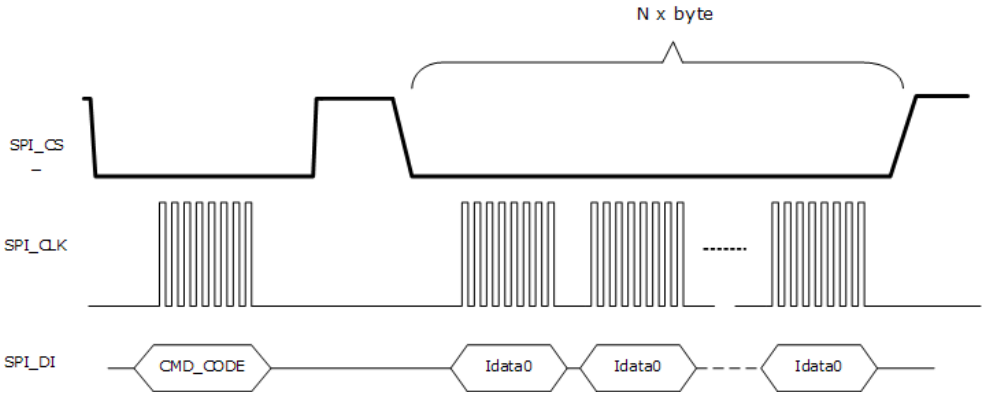



**Figure 3-6** SPI host-writing-register timing: type 4

## 3.3.2 SPI Read-Register Process (Type 1/4)

Each SPI read-register process contains two cycles: the command cycle and the data cycle. Commands and data are transferred in octets. When MMIS_D3 is asserted, IF206 receives commands in command cycles and sends data in data cycles.

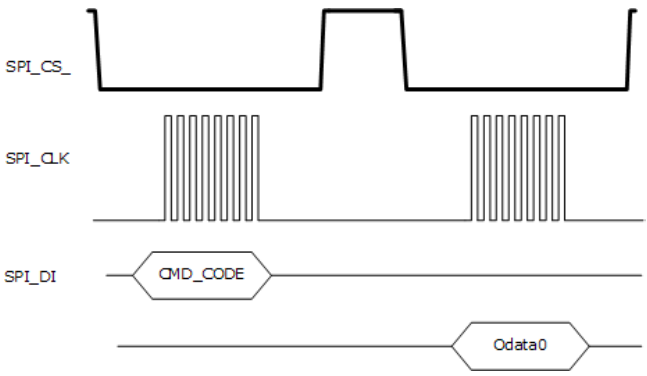



**Figure 3-7** SPI host-reading-register timing: type 1

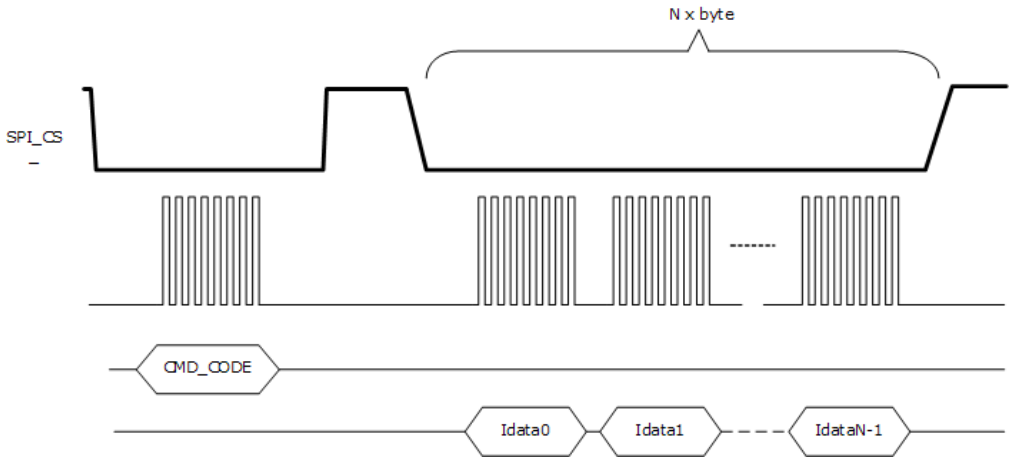



**Figure 3-8** SPI host-reading-register timing: type 4

### 3.3.3 SPI Read in the Burst Mode (Type 1/4)

In the burst mode, IF206 sends the data till all the data is transferred or MMIS_D3 is de-asserted in a read-operation. In this process, all the data will be transferred in the data cycle and only one command is required. The size of the data to be transmitted is determined by the data size of the logical channel.

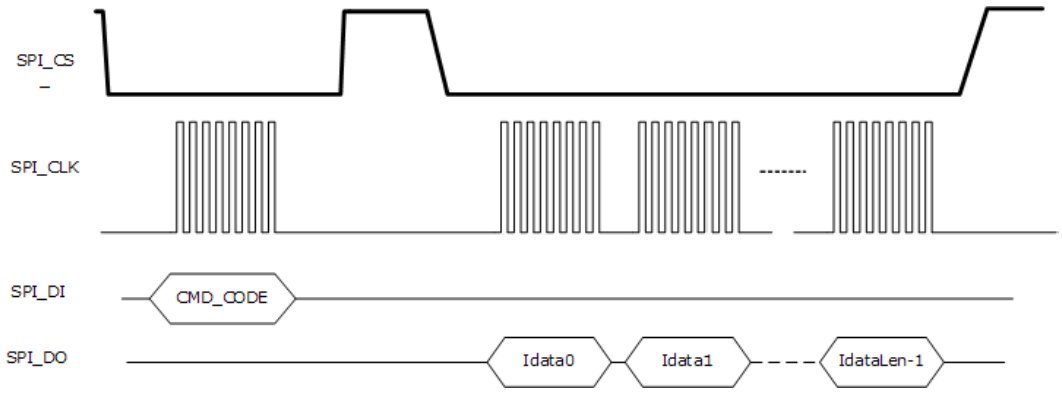



**Figure 3-9** Host-read timing: the burst mode

### 3.3.4 SPI Transfer: Type 2

In type 2, registers and the data in the memory can be accessed through the corresponding addresses. The access operation (write or read) to each byte requires an internal bus operation.

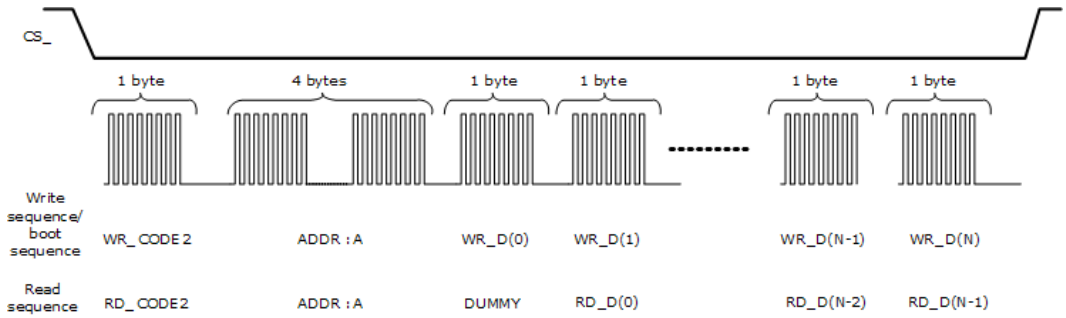
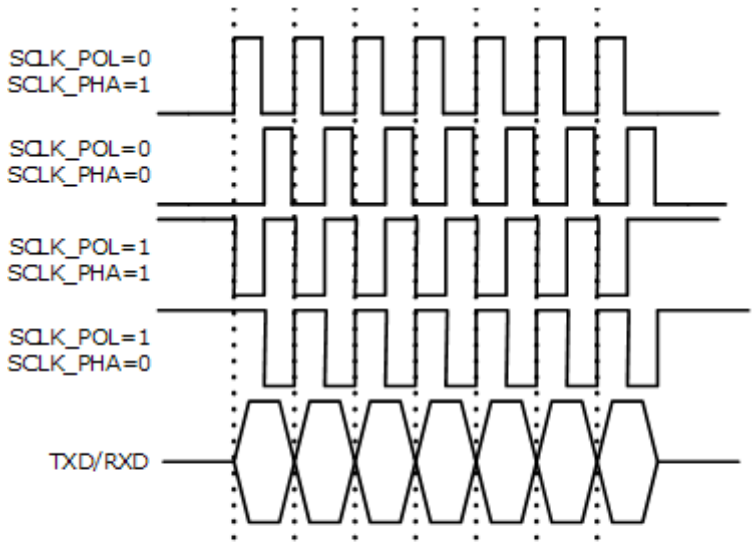



**Figure 3-10** SPI operation sequence: boot, write, and read (type 2)

## 3.3.5 Clock Timing

MMIS_CLK can be configured in MMIS_CONFIG [1:0]. The MMIS_CONFIG [1:0] setting determines MMIS_CLK transmitting edge and data receiving edge between a host and the MMIS bus on the device side.

It is also recommended that the maximum SCLK frequency be set to 10MHz. Currently, IF206 firmware is only supported by the condition of phase and polarity: SCLK_POL=0, SCLK_PHA=0, transmitted data is driven on the falling edge of SCLK and receive data is latched on the rising edge of SCLK.




| SCLK_POL | SCLK_PHA | Transmitting side | Receiving side |
|---|---|---|---|
| 0 | 0 | Falling edge | Rising edge |
| 0 | 1 | Rising edge | Falling edge |
| 1 | 0 | Rising edge | Falling edge |
| 1 | 1 | Falling edge | Rising edge |

**Figure 3-11** Configuration of signals edge and phase

# 4 Electrical Characteristics

This chapter gives the electrical characteristics of IF206.

## Topics

# 4.1 Absolute Maximum Rating Parameters

*Table 4-1* lists the absolute maximum rating indexes of IF206.

**Table 4-1** Absolute maximum rating indexes

| Index | Rating |
|---|---|
| Operating ambient temperature range | -40 to +85ºC |
| Storage temperature range | -65 to +150ºC |
| Power supply (VDDIO) | -0.3 to +5.5V |
| Power supply (core voltage) | -0.3 to +1.5V |
| Power supply (for RF) | -0.3 to +2.0V |
| ESD (HBM) | ±2KV |

# 4.2 DC Electrical Characteristics

*Table 4-2* lists the DC electrical characteristics of IF206.

**Table 4-2** DC electrical characteristics

| Index | | Symbol | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|---|
| Operation voltage for demodulator block | IO voltage | VDDIO | 1.62 | 1.80 | 3.60 | V |
| | Core voltage | VDD12, AVDD12 | 1.08 | 1.20 | 1.32 | V |
| Operation voltage for RF block | Core voltage | VDD_VCO, VDD_RF | 1.70 | 1.80 | 1.90 | V |
| Digital input/ output | High input level range | VIH | VDDIO-0.6 | | VDDIO +0.3 | V |
| | Low input level range | VIL | | | 0.5 | V |
| | High output level range | VOH | VDDIO-0.6 | | | V |
| | Low output level range | VOL | | | 0.3 | V |
| Power dissipation (demodulator + RF) | QPSK | PD_QPSK | | TBD | | mW |
| | 16QAM | PD_QAM16 | | TBD | | mW |
| Power consumption in the sleep mode | | TBD | | | | |

**Note:**

A TS (time slot) is a physical layer frame segment that can be received by a terminal.

# 4.3 AC Timing Characteristics

*Table 4-3* lists the AC timing characteristics of IF206.

**Table 4-3** AC timing characteristics

| Index | | Symbol | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|---|
| Reference clock (crystal) | Frequency | $F_{clk}$ | | 10/12/13/19.2/20/24/26/27/30 | | MHz |
| | Frequency tolerance | $\Delta_F$ | | 30 | | ppm |
| SPI interface | Cycle time | $T_{CYC}$ | 100[1] | 167 | 333 | ns |
| | CS setup time | $T_{CSS}$ | 80 | 100 | | ns |
| | CS high level time | $T_{CSW}$ | 80 | 100 | | ns |
| | Data delay from clock edge | $T_D$ | 32 | 36 | 40 | ns |
| | Data input setup time | $T_{IS}$ | 4 | 8 | | ns |
| | Data input hold time | $T_{IH}$ | 4 | 8 | | ns |
| SDIO interface | Conforming to the standard SDIO version 2. | | | | | |

1.The minimum $T_{cyc}$ depends on the external crystal oscillator at the boot time.

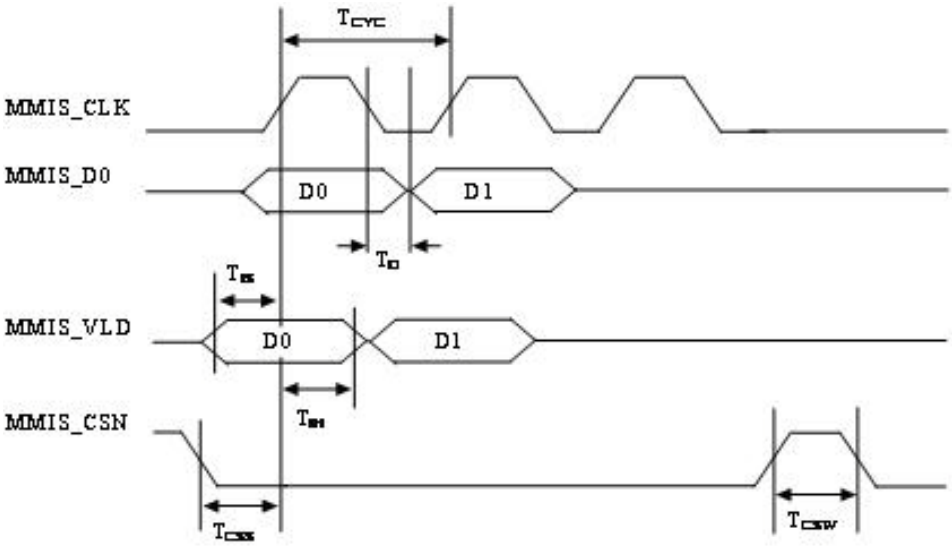



**Figure 4-1** AC Timing of SPI interface

# 5 Register Description

This chapter describes the registers of IF206.

## Topics

# 5.1 SPI Communication Mode

Innofidei provides firmware for these communication modes: the SPI mode and the SDIO mode.

In the SPI mode, both data and commands are transferred over SPI bus.

In the SDIO mode, both data and commands are transferred over SDIO bus.

The addresses of some registers vary with the communication mode.

# 5.2 Register Mapping

*Table 5-1* lists the mapping relationship between IF206 registers and command codes.

**Table 5-1** IF206 registers and command codes

| Command code | Value | Description | Timing type |
|---|---|---|---|
| INT0_ENABLE | 0x04 | Interface 0 interrupt enable/disable | Type 1 |
| INT1_ENABLE | 0x05 | Interface 1 interrupt enable/disable | Type 1 |
| INT2_ENABLE | 0x06 | Interface 2 interrupt enable/disable | Type 1 |
| INT0_STATUS | 0x0a | Interface 0 interrupt status | Type 1 |
| INT1_STATUS | 0x0b | Interface 1 interrupt status | Type 1 |
| INT2_STATUS | 0x0c | Interface 2 interrupt status | Type 1 |
| LG0_LEN_LOW | 0x15 | Lower byte of logical channel 0 | Type 1 |
| LG0_LEN_MID | 0x16 | Middle byte of logical channel 0 | Type 1 |
| LG0_LEN_HIGH | 0x17 | Higher byte of logical channel 0 | Type 1 |
| LG1_LEN_LOW | 0x18 | Lower byte of logical channel 1 | Type 1 |
| LG1_LEN_MID | 0x19 | Middle byte of logical channel 1 | Type 1 |
| LG1_LEN_HIGH | 0x1a | Higher byte of logical channel 1 | Type 1 |
| LDPC_TOTAL_NUM_0 | 0x30 | | Type 1 |
| LDPC_TOTAL_NUM_1 | 0x31 | | Type 1 |
| LDPC_TOTAL_NUM_2 | 0x32 | | Type 1 |
| LDPC_TOTAL_NUM_3 | 0x33 | | Type 1 |
| LDPC_ERR_NUM_0 | 0x34 | | Type 1 |
| LDPC_ERR_NUM_1 | 0x35 | | Type 1 |
| LDPC_ERR_NUM_2 | 0x36 | | Type 1 |
| LDPC_ERR_NUM_3 | 0x37 | | Type 1 |

**Table 5-1** IF206 registers and command codes (continued)

| Command code | Value | Description | Timing type |
|---|---|---|---|
| RS_TOTAL_NUM_0 | 0x38 | | Type 1 |
| RS_TOTAL_NUM_1 | 0x39 | | Type 1 |
| RS_TOTAL_NUM_2 | 0x3a | | Type 1 |
| RS_TOTAL_NUM_3 | 0x3b | | Type 1 |
| RS_ERR_NUM_0 | 0x3c | | Type 1 |
| RS_ERR_NUM_1 | 0x3d | | Type 1 |
| RS_ERR_NUM_2 | 0x3e | | Type 1 |
| RS_ERR_NUM_3 | 0x3f | | Type 1 |
| SYNC_STATE | 0x50 | | Type 1 |
| FETCH_LG0_DATA | 0x99 | Reading service data of logical channel 0 | Type 1 |
| FETCH_LG1_DATA | 0x9b | Reading service data of logical channel 1 | Type 1 |
| TS0_LEN_LOW | 0x1b | The lower byte of TS0 | Type 1 |
| TS0_LEN_MID | 0x1c | The middle byte of TS0 | Type 1 |
| TS0_LEN_HIGH | 0x1d | The higher byte of TS0 | Type 1 |
| FETCH_TS0_DATA | 0x9d | Reading TS0 data | Type 1 |
| FETCH_LG2_DATA | 0x80 | Reading service data of logical channel 2 | Type 1 |
| FETCH_LG3_DATA | 0x81 | Reading service data of logical channel 3 | Type 1 |
| FETCH_LG4_DATA | 0x82 | Reading service data of logical channel 4 | Type 1 |
| FETCH_LG5_DATA | 0x83 | Reading service data of logical channel 5 | Type 1 |
| FETCH_LG6_DATA | 0x84 | Reading service data of logical channel 6 | Type 1 |
| FETCH_LG7_DATA | 0x85 | Reading service data of logical channel 7 | Type 1 |
| FETCH_LG8_DATA | 0x86 | Reading service data of logical channel 8 | Type 1 |
| FETCH_LG9_DATA | 0x87 | Reading service data of logical channel 9 | Type 1 |
| LG0_LEN | 0x62 | Reading logical channel 0 length | Type 4, N=3 |
| LG1_LEN | 0x63 | Reading logical channel 1 length | Type 4, N=3 |
| LG2_LEN | 0x64 | Reading logical channel 2 length | Type 4, N=3 |
| LG3_LEN | 0x65 | Reading logical channel 3 length | Type 4, N=3 |
| LG4_LEN | 0x66 | Reading logical channel 4 length | Type 4, N=3 |
| LG5_LEN | 0x67 | Reading logical channel 5 length | Type 4, N=3 |
| LG6_LEN | 0x68 | Reading logical channel 6 length | Type 4, N=3 |
| LG7_LEN | 0x69 | Reading logical channel 7 length | Type 4, N=3 |
| LG8_LEN | 0x6a | Reading logical channel 8 length | Type 4, N=3 |

**Table 5-1** IF206 registers and command codes (continued)

| Command code | Value | Description | Timing type |
|---|---|---|---|
| LG9_LEN | 0x6b | Reading logical channel 9 length | Type 4, N=3 |
| INT_STATUS | 0x6e | Reading interrupt status | Type 4, N=2 |
| READ_PER_COMM0 | 0xA0 | | Type1 |
| WRITE_PER_COMM0 | 0xA1 | | Type1 |
| READ_PER_COMM1 | 0xA2 | | Type1 |
| WRITE_PER_COMM1 | 0xA3 | | Type1 |
| READ_PER_COMM2 | 0xA4 | | Type1 |
| WRITE_PER_COMM2 | 0xA5 | | Type1 |
| READ_PER_COMM3 | 0xA6 | | Type1 |
| WRITE_PER_COMM3 | 0xA7 | | Type1 |
| READ_PER_COMM4 | 0xA8 | | Type1 |
| WRITE_PER_COMM4 | 0xA9 | | Type1 |
| READ_PER_COMM5 | 0xAA | | Type1 |
| WRITE_PER_COMM5 | 0xAB | | Type1 |
| READ_PER_COMM6 | 0xAC | | Type1 |
| WRITE_PER_COMM6 | 0xAD | | Type1 |
| READ_PER_COMM7 | 0xAE | | Type1 |
| WRITE_PER_COMM7 | 0xAF | | Type1 |
| READ_PER_COMM8 | 0xB0 | | Type1 |
| WRITE_PER_COMM8 | 0xB1 | | Type1 |
| READ_PER_COMM9 | 0xB2 | | Type1 |
| WRITE_PER_COMM9 | 0xB3 | | Type1 |
| READ_PER_COMM10 | 0xB4 | | Type1 |
| WRITE_PER_COMM10 | 0xB5 | | Type1 |
| READ_PER_COMM11 | 0xB6 | | Type1 |
| WRITE_PER_COMM11 | 0xB7 | | Type1 |
| READ_PER_COMM12 | 0xB8 | | Type1 |
| WRITE_PER_COMM12 | 0xB9 | | Type1 |
| READ_PER_COMM13 | 0xBA | | Type1 |
| WRITE_PER_COMM13 | 0xBB | | Type1 |
| READ_PER_COMM14 | 0xBC | | Type1 |
| WRITE_PER_COMM14 | 0xBD | | Type1 |
| READ_PER_COMM15 | 0xBE | | Type1 |
| WRITE_PER_COMM15 | 0xBF | | Type1 |
| READ_PER_COMM16 | 0xC0 | | Type1 |
| WRITE_PER_COMM16 | 0xC1 | | Type1 |
| READ_PER_COMM17 | 0xC2 | | Type1 |
| WRITE_PER_COMM17 | 0xC3 | | Type1 |
| READ_PER_COMM18 | 0xC4 | | Type1 |
| WRITE_PER_COMM18 | 0xC5 | | Type1 |

**Table 5-1** IF206 registers and command codes (continued)

| Command code | Value | Description | Timing type |
|---|---|---|---|
| READ_PER_COMM19 | 0xC6 | | Type1 |
| WRITE_PER_COMM19 | 0xC7 | | Type1 |
| READ_PER_COMM20 | 0xC8 | | Type1 |
| WRITE_PER_COMM20 | 0xC9 | | Type1 |
| READ_PER_COMM21 | 0xCA | | Type1 |
| WRITE_PER_COMM21 | 0xCB | | Type1 |
| READ_PER_COMM22 | 0xCC | | Type1 |
| WRITE_PER_COMM22 | 0xCD | | Type1 |
| READ_PER_COMM23 | 0xCE | | Type1 |
| WRITE_PER_COMM23 | 0xCF | | Type1 |
| READ_PER_COMM24 | 0xD0 | | Type1 |
| WRITE_PER_COMM24 | 0xD1 | | Type1 |
| READ_PER_COMM25 | 0xD2 | | Type1 |
| WRITE_PER_COMM25 | 0xD3 | | Type1 |
| READ_PER_COMM26 | 0xD4 | | Type1 |
| WRITE_PER_COMM26 | 0xD5 | | Type1 |
| READ_PER_COMM27 | 0xD6 | | Type1 |
| WRITE_PER_COMM27 | 0xD7 | | Type1 |
| READ_PER_COMM28 | 0xD8 | | Type1 |
| WRITE_PER_COMM28 | 0xD9 | | Type1 |
| READ_PER_COMM29 | 0xDA | | Type1 |
| WRITE_PER_COMM29 | 0xDB | | Type1 |
| READ_PER_COMM30 | 0xDC | | Type1 |
| WRITE_PER_COMM30 | 0xDD | | Type1 |
| READ_PER_COMM31 | 0xDE | | Type1 |
| WRITE_PER_COMM31 | 0xDF | | Type1 |
| READ_AHBM2 | 0x71 | Reading AHB space method2 | Type 2 |
| WRITE_AHBM2 | 0x73 | Writing AHB space method2 | Type 2 |

# 5.3 SPI Communication Register

# 5.4 SPI Status Register

## 5.4.1 MMIS_LG0_LEN (0-2): Logical Channel 0 Data Length

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| MMIS_LG0_LEN0 | MMIS_LG0_LEN (bit 7 through bit 0) | | | | | | | |
| MMIS_LG0_LEN1 | MMIS_LG0_LEN (bit 15 through bit 8) | | | | | | | |
| MMIS_LG0_LEN2 | MMIS_LG0_LEN (bit 23 through bit 16) | | | | | | | |

Bit 23 through bit 0 carry the data of logical channel 0.

## 5.4.2 MMIS_LG1_LEN (0-2): Logical Channel 1 Data Length

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| MMIS_LG1_LEN0 | MMIS_LG1_LEN (bit 7 through bit 0) | | | | | | | |
| MMIS_LG1_LEN1 | MMIS_LG1_LEN (bit 15 through bit 8) | | | | | | | |
| MMIS_LG1_LEN2 | MMIS_LG1_LEN (bit 23 through bit 16) | | | | | | | |

Bit 23 through bit 0 carry the data of logical channel 1.

## 5.4.3 MMIS_LDPC_TTL_NUM (0-3): Total LDPC Count

| Name | Definition |
|---|---|
| MMIS_LDPC_TTL_NUM0 | Total LDPC count (bit 7 through.bit 0) |
| MMIS_LDPC_TTL_NUM1 | Total LDPC count (bit 15 through bit 8) |
| MMIS_LDPC_TTL_NUM2 | Total LDPC count (bit 23 through bit 16) |
| MMIS_LDPC_TTL_NUM3 | Total LDPC count (bit 31 through bit 24) |

### 5.4.4 MMIS_LDPC_ERR_NUM (0-3): LDPC Error Count

| Name | Definition |
|---|---|
| MMIS_LDPC_ERR_NUM0 | LDPC error count (bit 7 through bit 0) |
| MMIS_LDPC_ERR_NUM1 | LDPC error count (bit 15 through bit 8) |
| MMIS_LDPC_ERR_NUM2 | LDPC error count (bit 23 through bit 16) |
| MMIS_LDPC_ERR_NUM3 | LDPC error count (bit 31 through bit 24) |

### 5.4.5 MMIS_RS_TTL_NUM (0-3): Total LDPC Count

| Name | Definition |
|---|---|
| MMIS_RS_TTL_NUM0 | Total RS count (bit7 through bit 0) |
| MMIS_RS_TTL_NUM1 | Total RS count (bit 15 through.bit 8) |
| MMIS_RS_TTL_NUM2 | Total RS count (bit 23 through bit 16) |
| MMIS_RS_TTL_NUM3 | Total RS count (bit 31 through bit 24) |

### 5.4.6 MMIS_RS_ERR_NUM (0-3): RS Error Count

| Name | Definition |
|---|---|
| MMIS_RS_ERR_NUM0 | RS error count (bit7 through bit 0) |
| MMIS_RS_ERR_NUM1 | RS error count (bit 15 through.bit 8) |
| MMIS_RS_ERR_NUM2 | RS error count (bit 23 through bit 16) |
| MMIS_RS_ERR_NUM3 | RS error count (bit 31.through.bit 24) |

## 5.5 SDIO Interface

IF206 supports SDIO Specification version 2 and can transmit data in the one-line and four-line transmission modes. The highest frequency supported is 25MHz.

IF206 also supports a more effective transmission mode: the block transmitting mode, which allows for communication and mass data transmission between AP and devices. In addition, SDIO function 1 extension enables IF206 to integrate

various extended functions.

### 5.5.1 SDIO Function 1 Address Mapping

**Table 5-2** Function 1 address mapping

| Name | Address | Width | Description | RW type |
|---|---|---|---|---|
| INT0_STATUS | 0x00 | 8 | Logic channel 0 through 7 are ready.<br>Generate a interrupt to AP when set to 1. | RC |
| INT1_STATUS | 0x01 | 8 | Logical channel 8 and 9 are ready.<br>Bit 12 through 15 TBD. | RC |
| INT2_STATUS | 0x02 | 8 | TBD | RC |
| INT0_ENABLE | 0x03 | 8 | Corresponding to int_enable[7:0].<br>Disables interrupt. | RW |
| INT1_ENABLE | 0x04 | 8 | Corresponding to int_enable[15:8].<br>Disable interrupt | RW |
| INT2_ENABLE | 0x05 | 8 | Corresponding to int_enable[23:16].<br>Disable interrupt | RW |
| FILTER0_PID_L | 0x07 | 8 | General registers for commu-nication | RW |
| FILTER0_PID_H | 0x08 | 8 | | |
| FILTER1_PID_L | 0x09 | 8 | | |
| FILTER1_PID_H | 0x0a | 8 | | |
| TS0_LEN_LOW | 0x0b | 8 | TS0 length lower 8 bits | RO |
| TS0_LEN_MID | 0x0c | 8 | TS0 length middle 8 bits | |
| TS0_LEN_HIGH | 0x0d | 8 | TS0 length higher 8 bits<br>TS0 length defaults to 24'h00. | |
| LG0_LEN_LOW | 0x0e | 8 | logic channel 0 lower 8 bits | RO |
| LG0_LEN_MID | 0x0f | 8 | logic channel 0 middle 8 bits | |
| LG0_LEN_HIGH | 0x10 | 8 | logic channel 0 higher 8 bits.<br>Logical channel 0 length defaults to 24'h00. | |
| LG1_LEN_LOW | 0x11 | 8 | logic channel 1 lower 8 bits | RO |
| LG1_LEN_MID | 0x12 | 8 | logic channel middle 8 bits | |
| LG1_LEN_HIGH | 0x13 | 8 | logic channel, high 8bit length<br>*LG1 length default: 24'h00 | |

**Table 5-2** Function 1 address mapping (continued)

| Name | Address | Width | Description | RW type |
|---|---|---|---|---|
| LDPC_ERR_COUNTER0 | 0x44 | 8 | LDPC error counter 7 through 0 bit | WC |
| LDPC_ERR_COUNTER1 | 0x45 | 8 | LDPC error counter 15 through 8 bit | |
| LDPC_ERR_COUNTER2 | 0x46 | 8 | LDPC error counter 23 through 16 bit | |
| LDPC_ERR_COUNTER3 | 0x47 | 8 | LDPC error counter 31 through 24 bit<br>Write to clear. | |
| LDPC_TTL_NUM0 | 0x40 | 8 | LDPC total number.<br>Write to clear. | WC |
| LDPC_TTL_NUM1 | 0x41 | 8 | | |
| LDPC_TTL_NUM2 | 0x42 | 8 | | |
| LDPC_TTL_NUM3 | 0x43 | 8 | | |
| RS_ERR_CNT0 | 0x4c | 8 | RS error counter, based on V2 algorithm.<br>Write to clear. | WC |
| RS_ERR_CNT1 | 0x4d | 8 | | |
| RS_ERR_CNT2 | 0x4e | 8 | | |
| RS_ERR_CNT3 | 0x4f | 8 | | |
| RS_UNIT_ERR_CNT0 | | 8 | RS unit error counter, based on V1 algorithm.<br>Write to clear. | WC |
| RS_UNIT_ERR_CNT1 | | 8 | | |
| RS_UNIT_ERR_CNT2 | | 8 | | |
| RS_UNIT_ERR_CNT3 | | 8 | | |
| RS_TTL_NUM0 | 0x48 | 8 | RS total number 7 through 0 bit | WC |
| RS_TTL_NUM1 | 0x49 | 8 | RS total number 15 through 8 bit | |
| RS_TTL_NUM2 | 0x4a | 8 | RS total number 23 through 16 bit | |
| RS_TTL_NUM3 | 0x4b | 8 | RS total number 31 through 24 bit<br>Write to clear. | |
| SYNC_STATE | 0x60 | | Synchronization information | RO |
| CMNCT0 | 0x15 | 8 | General registers for communication with AP | RW |
| CMNCT1 | 0x16 | 8 | | |
| CMNCT2 | 0x17 | 8 | | |
| CMNCT3 | 0x18 | 8 | | |
| CMNCT4 | 0x50 | 8 | | |
| CMNCT5 | 0x51 | 8 | | |
| CMNCT6 | 0x52 | 8 | | |
| CMNCT7 | 0x53 | 8 | | |

**Table 5-2** Function 1 address mapping (continued)

| Name | Address | Width | Description | RW type |
|---|---|---|---|---|
| SDIO command register | 0x14 | 8 | Command port.<br>Write the command codes listed in *Table 5-3* to perform specific operations. See section *5.5.3 SDIO Register Operation Examples* for related information. | RW |
| SDIO fetch buffer read port | 0x19 | 8 | Read this port to get stream data.<br>Use fix_address defined in *SDIO Specification version 2* to access this register. | RO |
| SDIO AHB read port | 0x31 | 8 | Read this port to get AHB space data.<br>Use fix_address defined in *SDIO Specification version 2* to access this register. | RO |
| SDIO AHB write port | 0x32 | 8 | Write data to AHB space.<br>Use fix_address defined in *SDIO Specification version 2* to access this register. | WO |
| SDIO fetch base0 | 0x70 | 8 | These 24 bits are used to set the base address of fetch buffer for SDIO write port. | RW |
| SDIO fetch base1 | 0x71 | 8 | | |
| SDIO fetch base2 | 0x72 | 8 | | |
| SDIO AHB base0 | 0x73 | 8 | The base address of AHB space. | RW |
| SDIO AHB base1 | 0x74 | 8 | | |
| SDIO AHB base2 | 0x75 | 8 | | |
| SDIO AHB base3 | 0x76 | 8 | | |
| LG2 LEN_LOW | 0x80 | | The data of logic channel 2, 24 bits in length | RO |
| LG2_LEN_MID | 0x81 | | | |
| LG2_LEN_HIGH | 0x82 | | | |
| LG3 LEN_LOW | 0x83 | | The data of logic channel 3, 24 bits in length | RO |
| LG3_LEN_MID | 0x84 | | | |
| LG3_LEN_HIGH | 0x85 | | | |
| LG4 LEN_LOW | 0x86 | | The data of logic channel 4, 24 bits in length | RO |
| LG4_LEN_MID | 0x87 | | | |
| LG4_LEN_HIGH | 0x88 | | | |
| LG5 LEN_LOW | 0x89 | | The data of logic channel 5, 24 bits in length | RO |
| LG5_LEN_MID | 0x8a | | | |
| LG5_LEN_HIGH | 0x8b | | | |
| LG6 LEN_LOW | 0x8c | | The data of logic channel 6, 24 bits in length | RO |
| LG6_LEN_MID | 0x8d | | | |
| LG6_LEN_HIGH | 0x8e | | | |

**Table 5-2** Function 1 address mapping (continued)

| Name | Address | Width | Description | RW type |
|---|---|---|---|---|
| LG7 LEN_LOW | 0x8f | | The data of logic channel 7, 24 bits in length | RO |
| LG7_LEN_MID | 0x90 | | | |
| LG7_LEN_HIGH | 0x91 | | | |
| LG8 LEN_LOW | 0x92 | | The data of logic channel 8, 24 bits in length | RO |
| LG8_LEN_MID | 0x93 | | | |
| LG8_LEN_HIGH | 0x94 | | | |
| LG9 LEN_LOW | 0x95 | | The data of logic channel 9, 24 bits in length | RO |
| LG9_LEN_MID | 0x96 | | | |
| LG9_LEN_HIGH | 0x97 | | | |
| PER_COMM0 | 0xa0 | | | RW |
| PER_COMM1 | 0xa1 | | | RW |
| PER_COMM2 | 0xa2 | | | RW |
| PER_COMM3 | 0xa3 | | | RW |
| PER_COMM4 | 0xa4 | | | RW |
| PER_COMM5 | 0xa5 | | | RW |
| PER_COMM6 | 0xa6 | | | RW |
| PER_COMM7 | 0xa7 | | | RW |
| PER_COMM8 | 0xa8 | | | RW |
| PER_COMM9 | 0xa9 | | | RW |
| PER_COMM10 | 0xaa | | | RW |
| PER_COMM11 | 0xab | | | RW |
| PER_COMM12 | 0xac | | | RW |
| PER_COMM13 | 0xad | | | RW |
| PER_COMM14 | 0xae | | | RW |
| PER_COMM15 | 0xaf | | | RW |
| PER_COMM16 | 0xb0 | | | RW |
| PER_COMM17 | 0xb1 | | | RW |
| PER_COMM18 | 0xb2 | | | RW |
| PER_COMM19 | 0xb3 | | | RW |
| PER_COMM20 | 0xb4 | | | RW |
| PER_COMM21 | 0xb5 | | | RW |
| PER_COMM22 | 0xb6 | | | RW |
| PER_COMM23 | 0xb7 | | | RW |
| PER_COMM24 | 0xb8 | | | RW |
| PER_COMM25 | 0xb9 | | | RW |
| PER_COMM26 | 0xba | | | RW |
| PER_COMM27 | 0xbb | | | RW |
| PER_COMM28 | 0xbc | | | RW |

**Table 5-2** Function 1 address mapping (continued)

| Name | Address | Width | Description | RW type |
|---|---|---|---|---|
| PER_COMM29 | 0xbd | | | RW |
| PER_COMM30 | 0xbe | | | RW |
| PER_COMM31 | 0xbf | | | RW |

## 5.5.2 SDIO Command Table

Write 0x14 to perform the corresponding operations. See section *5.5.3 SDIO Register Operation Examples* for related information.

**Table 5-3** SDIO commands

| Name | Value | Description |
|---|---|---|
| FETCH TS0 DATA | 0x02 | Get TS0 data |
| FETCH LG0 DATA | 0x03 | Get LG0 data |
| FETCH LG1 DATA | 0x04 | Get LG1 data |
| FETCH LG2 DATA | 0x05 | Get LG2 data |
| FETCH LG3 DATA | 0x06 | Get LG3 data |
| FETCH LG4 DATA | 0x07 | Get LG4 data |
| FETCH LG5 DATA | 0x08 | Get LG5 data |
| FETCH LG6 DATA | 0x09 | Get LG6 data |
| FETCH LG7 DATA | 0x0a | Get LG7 data |
| FETCH LG8 DATA | 0x0b | Get LG8 data |
| FETCH LG9 DATA | 0x0c | Get LG9 data |

## 5.5.3 SDIO Register Operation Examples

All the SDIO register operations shall comply to SDIO protocol. The max frequency is 25MHz.

- Writing the register INT0_ENABLE (0x03)

Command cycle: CMD52_Address(0x03)_WriteOption_WriteData

Response cycle: R5_RespStatus_xxxxxx

- Reading the register INT0_ENABLE (0x03)

Command cycle: CMD52_Address(0x03)_ReadOption_xxxxxxxxx

Response cycle: R5_RespStatus_ReadData

**I. Fetching the data in Logic Channel 2**

All the SDIO register operations shall comply to SDIO protocol. The max frequency is 25MHz.

- Writing the Command FETCH LG2 DATA (0x05) to SDIO command register (0x14)

Command cycle: CMD52_Address(0x14)_WriteOption_0x05

Response cycle: R5_RespStatus_xxxxxx

- Reading SDIO Fetch Buffer Read Port (0x19) to get the data

Command cycle: CMD53_Address(0x19)_ReadOption_xxxxxx

Response cycle: R5_RespStatus_xxxxxx

Data cycle: Data_transfer

**II. SDIO Write Data to AHB**

The process of Write data to AHB is similar to the following.

- Setting the SDIO AHB base address to 0x50002000

Writing 0x50002000 to registers SDIO AHB base0/1/2/3

Command cycle: CMD52_Adddress (0x73)_WriteOption_0x00

Response cycle: R5_RespStatus_xxxxxx

Command cycle: CMD52_Adddress (0x74)_WriteOption_0x20

Response cycle: R5_RespStatus_xxxxxx

Command cycle:CMD52_Adddress (0x75)_WriteOption_0x00

Response cycle: R5_RespStatus_xxxxxx

Command cycle: CMD52_Adddress (0x76)_WriteOption_0x50

Response cycle: R5_RespStatus_xxxxxx

- Write Data to SDIO_AHB_WRITE_PORT(0x32)

Command cycle: CMD53_address(0x32)_WriteOption_xxxxx

Response cycle: R5_RespStatus_xxxxx

Data cycle: Data_transfer

**III. SDIO Read Data from AHB Space**

- Setting the SDIO AHB Base address to 0x50002000

Writing 0x50002000 to registers SDIO AHB base0/1/2/3

Command cycle: CMD52_Adddress (0x73)_WriteOption_0x00

Response cycle: R5_RespStatus_xxxxxx

Command cycle: CMD52_Adddress (0x74)_WriteOption_0x20

Response cycle: R5_RespStatus_xxxxxx

Command cycle:CMD52_Adddress (0x75)_WriteOption_0x00

Response cycle: R5_RespStatus_xxxxxx

Command cycle: CMD52_Adddress (0x76)_WriteOption_0x50

Response cycle: R5_RespStatus_xxxxxx

- Reading data from SDIO AHB Read Port (0x31)

Command cycle: CMD53_Address(0x31)_ReadOption_xxxxx

Response cycle: R5_RespStatus_xxxxxx

Data cycle: Data_transfer

# 6 Reference Design

*Figure 6-1* and *Figure 6-5* illustrates IF206 reference design.

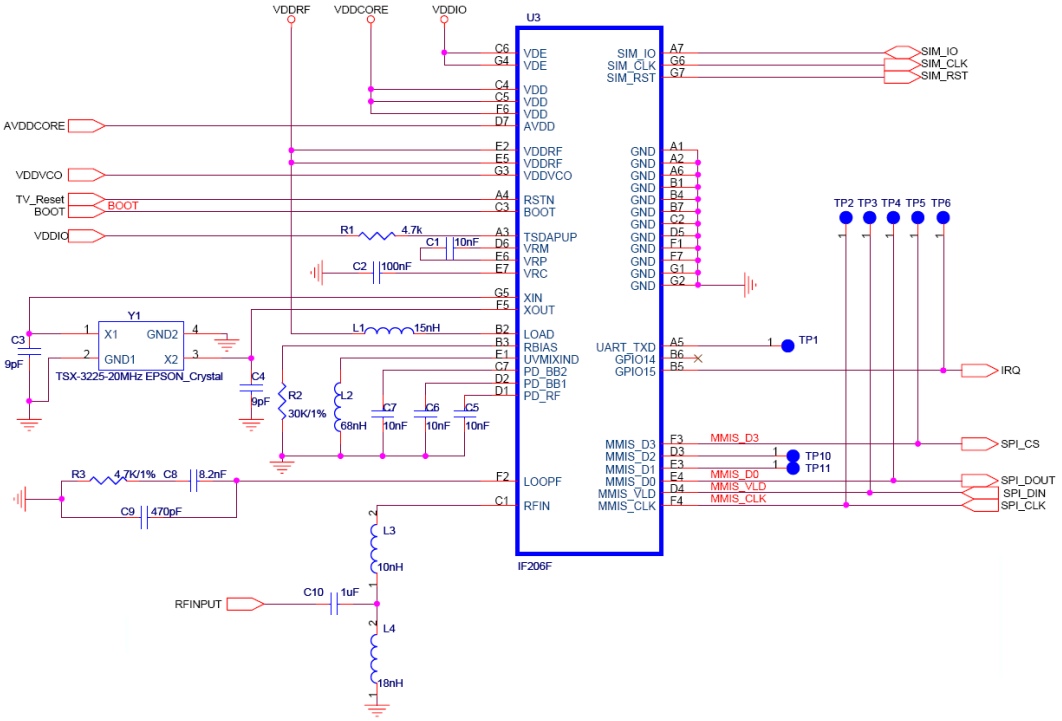



**Figure 6-1** IF206 reference design (1) (zoom in for details)

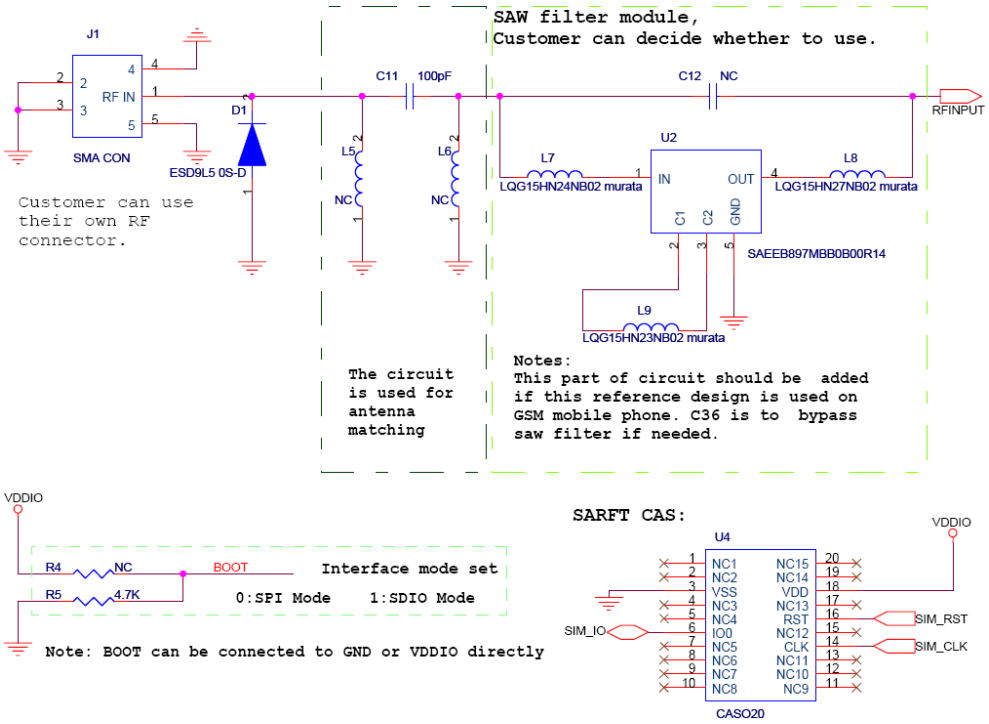



**Figure 6-2** IF206 reference design (2) (zoom in for details)

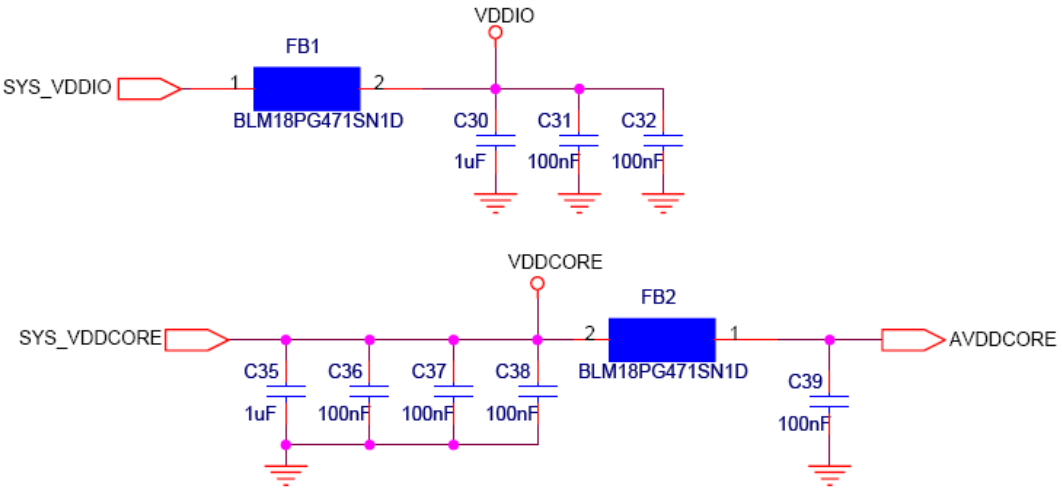



**Figure 6-3** IF206 reference design (3): power supply connection (zoom in for details)

**Note:**

- VDDIO and VDDCORE can be from AP board. Dedicated DC/LDO are unnecessary.
- The capacitances of the bypass capacitors are for reference only.

When VDDIO is higher than 2.5V, VDDRF is generated by LDO from VDDIO, as shown in *Figure 6-4*.

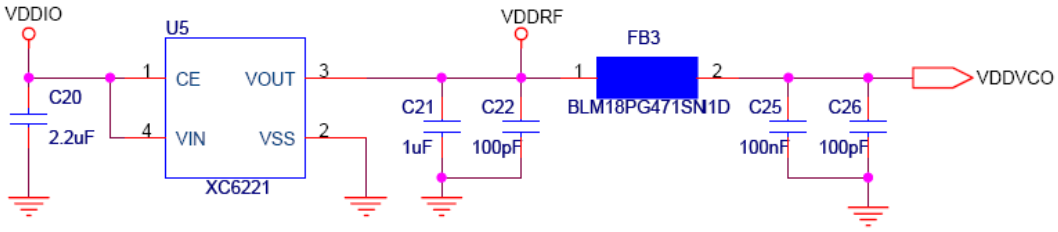



**Figure 6-4** IF206 reference design (4): VDDIO higher than 2.5V (zoom in for details)

When VDDIO is 1.8V, tie VDDRF to VDDIO through an RF ferrite bead, as shown in *Figure 6-5*.

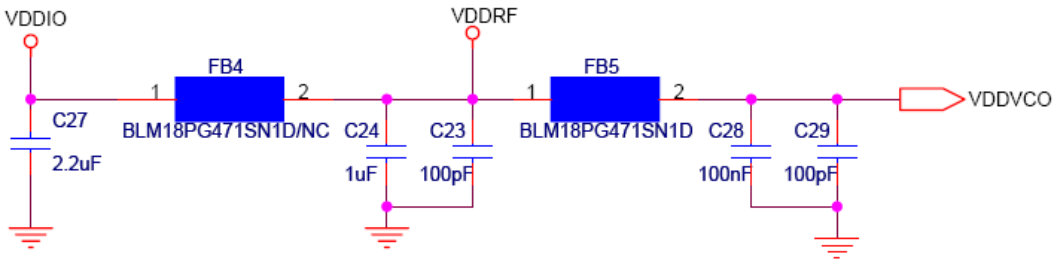



**Figure 6-5** IF206 reference design (5): 1.8V VDDIO (zoom in for details)

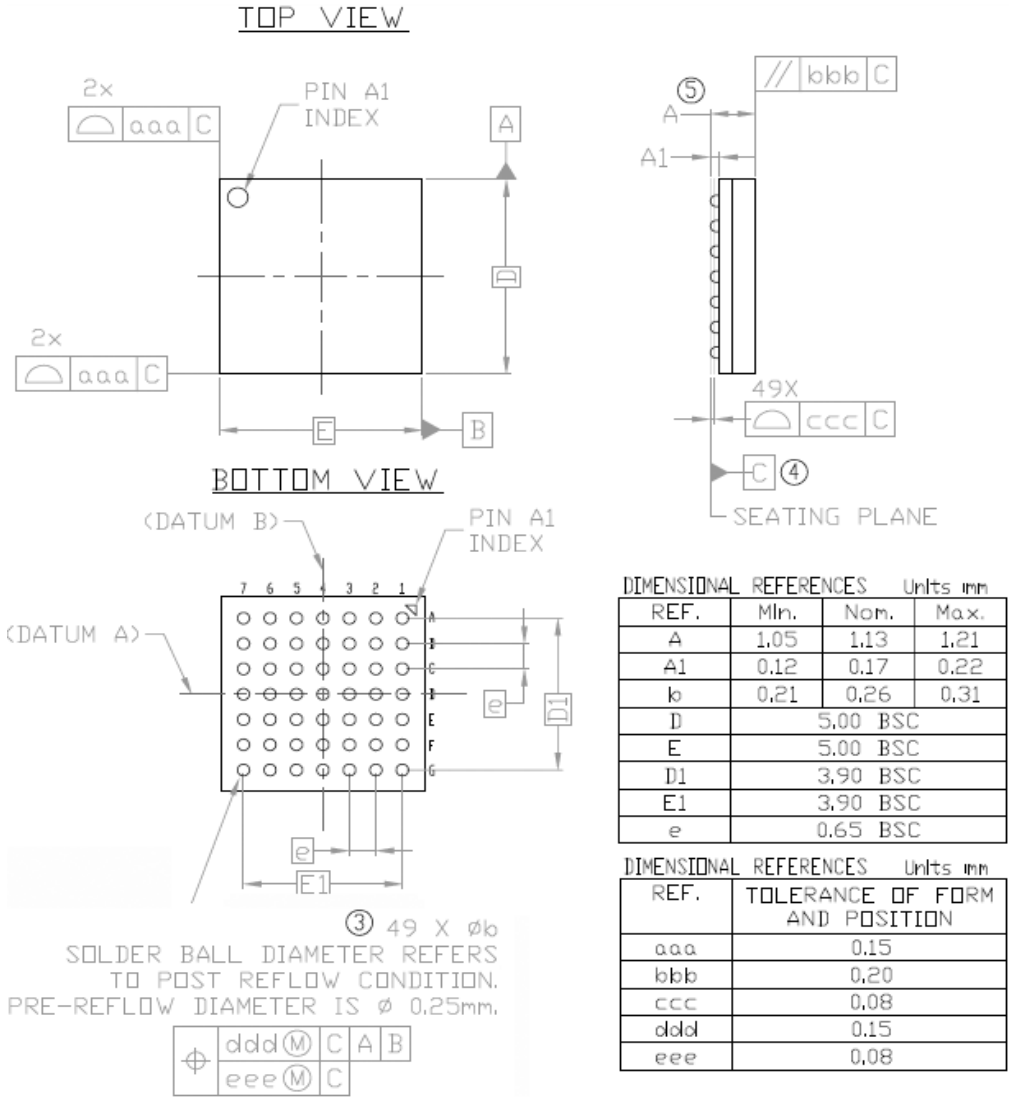
# 7 Mechanical Specification

This chapter gives the mechanical specification of IF206.

## Topics

# 7.1 Mechanical Specification of IF206

*Figure 7-1* shows the package specification of IF206.




DIMENSIONAL REFERENCES Units mm

| REF. | Min. | Nom. | Max. |
|---|---|---|---|
| A | 1.05 | 1.13 | 1.21 |
| A1 | 0.12 | 0.17 | 0.22 |
| b | 0.21 | 0.26 | 0.31 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| D1 | | 3.90 BSC | |
| E1 | | 3.90 BSC | |
| e | | 0.65 BSC | |

DIMENSIONAL REFERENCES Units mm

| REF. | TOLERANCE OF FORM AND POSITION |
|---|---|
| aaa | 0.15 |
| bbb | 0.20 |
| ccc | 0.08 |
| ddd | 0.15 |
| eee | 0.08 |

Notes:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
③ DIMENSION 'b' IS MEASURABLE AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
④ PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
⑤ DIMENSION 'A' INCLUDES STANDOFF HEIGHT 'A1', PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACH FEATURES.

**Figure 7-1** IF206 package specification

# Index

# 射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训推荐课程列表： http://www.edatop.com/peixun/tuijian/


## 射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

课程网址：http://www.edatop.com/peixun/rfe/110.html

## 手机天线设计培训视频课程


该套课程全面讲授了当前手机天线相关设计技术，内容涵盖了早期的外置螺旋手机天线设计，最常用的几种手机内置天线类型——如 monopole 天线、PIFA 天线、Loop 天线和 FICA 天线的设计，以及当前高端智能手机中较常用的金属边框和全金属外壳手机天线的设计；通过该套课程的学习，可以帮助您快速、全面、系统地学习、了解和掌握各种类型的手机天线设计，以及天线及其匹配电路的设计和调试...

课程网址： http://www.edatop.com/peixun/antenna/133.html

## WiFi 和蓝牙天线设计培训课程

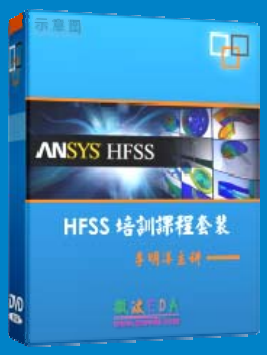
该套课程是李明洋老师应邀给惠普 (HP)公司工程师讲授的 3 天员工内训课程录像，课程内容是李明洋老师十多年工作经验积累和总结，主要讲解了 WiFi 天线设计、HFSS 天线设计软件的使用，匹配电路设计调试、矢量网络分析仪的使用操作、WiFi 射频电路和 PCB Layout 知识，以及 EMC 问题的分析解决思路等内容。对于正在从事射频设计和天线设计领域工作的您，绝对值得拥有和学习！…

课程网址：http://www.edatop.com/peixun/antenna/134.html

## CST 学习培训课程套装


该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

**课程网址：**http://www.edatop.com/peixun/cst/24.html

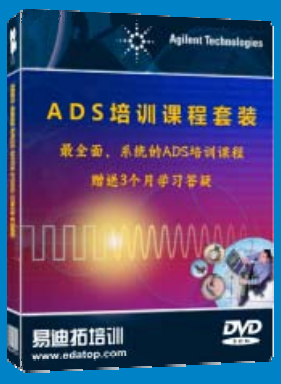



## HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

**课程网址：**http://www.edatop.com/peixun/hfss/11.html

## ADS 学习培训课程套装




该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

**课程网址：** http://www.edatop.com/peixun/ads/13.html

## 我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

## 联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com