FM8PC71A
FTC 8-Bit Micro-Controller

Datasheet V12

January 13, 2011

Version Control

Version	Date.	Description
V01	2010-03-10	Release of prototype
V02	2010-04-26	Modify PA,PB Mode
V03	2010-05-13	Modify CLKCFG(3Ah) register Default.
V05	2010-06-02	Modify Slow and Green mode.
V06	2010-06-07	Modify condition description for system switch mode.
V07	2010-0611	Modify Contents.
V08	2010-0914	Modify P-29 CLKCFG Register address
V09	2010-0929	Add DC characteristics
V10	2010-1201	Add AC,DC Measure parameter
V11	2011-0101	Modify Feature Description.
V12	2011-0113	Add Internal High and slow RC characteristic

Contents

【1】 FM8PC71A REVIEW

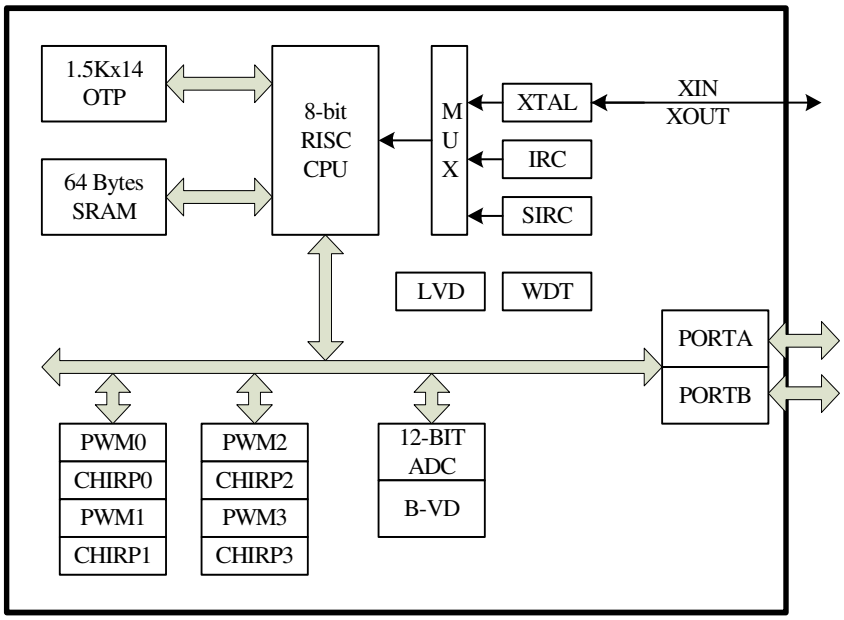
1.1 General Description

The FM8PC71A is an 8-bit microprocessor embedded device. It includes an 8-bit RISC MCU core, 64 bytes SRAM, 4XPWM,ADC and a 1.5K internal program OTP-ROM.

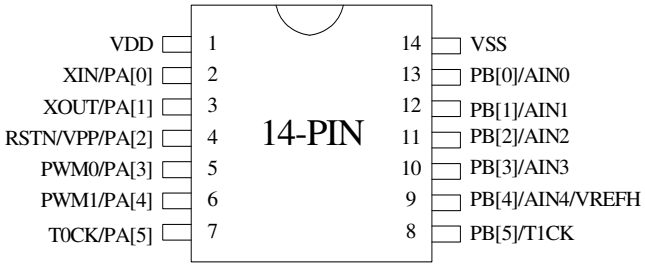
1.2 Features

- **8-bit RISC microprocessor**
  - On chip 1.5K x 14 program OTP Memory .
  - 6 level stack.
  - 64 bytes internal SRAM.
  - Optional Fosc/(1,2,4,8,16) MCU clock.
  - MCU can switch to work on External clock / internal slow 32K Hz clock.
  - Four 12-bit Timers/Counters are PTM0,PTM1,PTM2,PTM3 individually.
  - Watch dog Timer.
- **System Clock**
  - Internal Oscillator
    - Internal +/- 2% 16MHz Oscillator.
    - Internal oscillator 32KHz free run clock for suspend mode.
  - External crystal Oscillator
    - One Operating Frequency Range of Oscillator/crystal is 32k~16 MHz.
    - One RC type up to 10MHz
  - Optional external ceramic resonator or internal clock mode for MCU clock.
- **10+2 I/O ports**
  - High current dive on any GPIO pin :15mA pin current drive and sink.
  - Each GPIO pin supports high-impedance input, internal pull-ups, open drains output, or CMOS outputs.
  - External interrupt on all GPIO pin.
- **5+1 Channel 12-bit ADC.**
  - Optional Continues or Trigger mode to sample.
  - Support 5 channel external ADC input and a internal VDD/4 ADC input.
  - Build in AD reference voltage (VDD, 4V, 3V, 2V).
  - Support One channel DAC output.
- **Power on Manager**
  - Power on reset (POR) is 1.8V
    - Chip can work on greater than 2.0V power.
  - Three level Low Voltage Detect : LVDH(3.6V),LVDM(2.4V),LVDL(2.0V).
- **Build in PWM function.**
  - Support 4 channels PWM
- **GPIO supply 1.8V~5V interface.**

1.3 Block Diagram

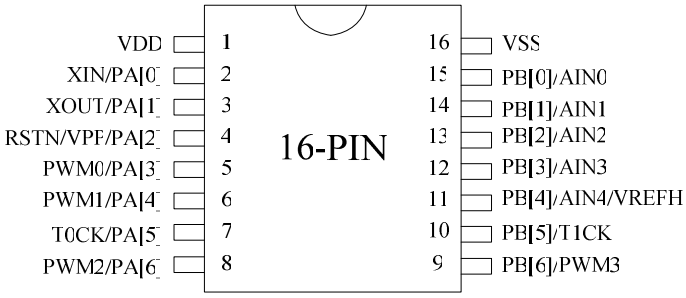


1.4 Pin Definitions



FM8PC71AA

PDIP/SOP



FM8PC71AB

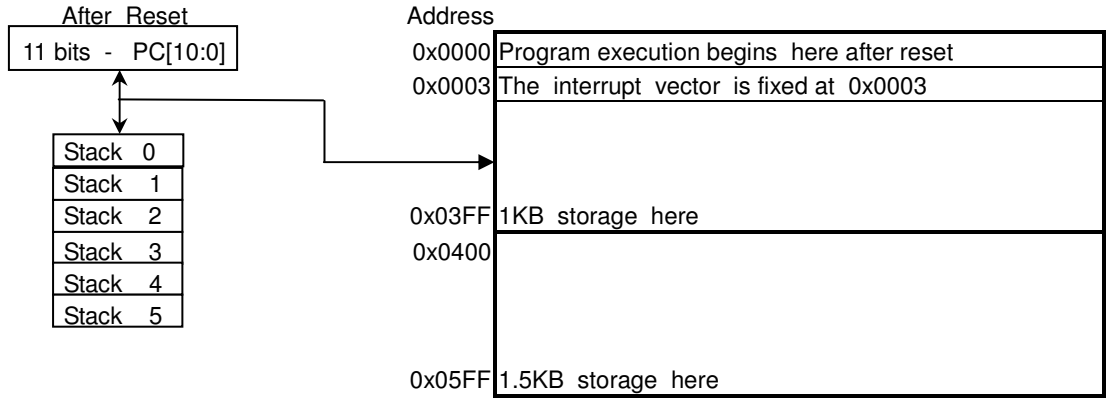
PDIP/SSOP

1.5 Pin Description

PIN Name	I/O	14-pin P	16-pin S	Description
PA[0] XIN	IO I	2	2	GPIO Port A [0]capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Up to 16Mhz ceramic resonator or external clock input when external Crystal enable.
PA[1] XOUT	IO I	3	3	GPIO Port A [1]capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Up to 16Mhz ceramic resonator or external clock output when external Crystal enable.
PA[2] VPP RSTN	I I	4	4	GPIO Port A [2] input and a resistive pull-up. Programming voltage supply, VCC for normal operation External reset pin , active low..
PA[3] PWM0	IO O	5	5	GPIO Port A [3] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM0 signal output pin when PWM0 enable.
PA[4] PWM1	IO O O	6	6	GPIO Port A [4]c apable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM1 signal output pin when PWM1 enable.
PA[5] T0CK	IO I	7	7	GPIO Port A [5] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Timer 0 or PWM0 timer or PWM2 timer external clock input pin
PA[6] PWM2	IO I	--	8	GPIO Port A [6]capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM2 signal output pin when PWM2 enable
PB[6] PWM3	IO I	--	9	GPIO Port B [6] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM3 signal output pin when PWM3 enable
PB[5] T1CK	IO I	8	10	GPIO Port B [5] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Timer 1 or PWM1 timer or OWM3 timer external clock input pin
PB[4] AIN4 VREFH	IO I	9	11	GPIO Port B [4]capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-4. External high reference voltage input of ADC

PIN Name	I/O	14-pin P	16-pin S	Description
PB[3] AIN3	IO I	10	12	GPIO Port B [3] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-3.
PB[2] AIN2	IO I	11	13	GPIO Port B [2] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-2.
PB[1] AIN1	IO O O	12	14	GPIO Port B [1] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-1.
PB[0] AIN0	IO I	13	15	GPIO Port B [0] capable of sinking up to 25mA/pin, or sinking controlled low or high programmable current. Can also source 25 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-0.
VSS	G	14	16	Ground

1.6 Program Memory Mapping



1.7 Memory And Register Mapping

Table 1.7-1 I/O Register Mapping

RAMBNK[1:0] / Address	Description(F-plane)	Address	R-Plane
00h	INDF		
01h	--		
02h	PCL		
03h	STATUS		
04h	FSR		
05h	PORTA	05h	PAPINSEL
06h	PORTB	06h	PBPINSEL
07h	PAIE		
08h	PBIE	08h	PAMODE0
09h	PACON	09h	PAMODE1
0Ah	PBCON	0Ah	PBMODE0
0Bh	INTEN	0Bh	PBMODE1
0Ch	INTFLAG	0Ch	PADRVMD0
0Dh	--	0Dh	PADRVMD1
0Eh	--		
0Fh	--	0Fh	PBDRVMD0
10h	--	10h	PBDRVMD1
11h	WDT		
12h	PCON		
13h	CLKCFG		

RAMBNK[1:0] / Address	Description(F-plane)	Address	R-Plane
14h	PWM0CON		
15h	PWM0CR		
16h	P0TMLB		
17h	P0RDLB		
18h	P0TRHB		
19h	PWM1CON		
1Ah	PWM1CR		
1Bh	P1TMLB		
1Ch	P1RDLB		
1Dh	P1TRHB		
1Eh	PWM2CON		
1Fh	PWM2CR		
20h	P2TMLB		
21h	P2RDLB		
22h	P2TRHB		
23h	PWM3CON		
24h	PWM3CR		
25h	P3TMLB		
26h	P3RDLB		
27h	P3TRHB		
28h	ADCON-1		
29h	ADCON-2		
30h	ADCHB		
31h	ADCLB		
32~34	General Purpose Registers 3 bytes		
35~3Fh(r/w)	Revered		
40h | 7Fh	SRAM 64 bytes		

Accessed by IOST/IOSTR instruction

The R-plane Registers are loaded with the contents of the ACC register by executing the IOST instruction. By executing the IOSTR instruction, user read these registers

TABLE 1.7-2: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
01h (r/w)	Revered	--							
02h (r/w)	PCL	Low order 8 bits of PC							
03h (r/w)	STATUS	--	--	--	/TO	/PD	Z	DC	C
04h (r/w)	FSR	Indirect data memory address pointer							
05h (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
06h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
07h (r/w)	PAIE	PAIE7	PAIE6	PAIE5	PAIE4	PAIE3	PAIE2	PAIE1	PAIE0
08h (r/w)	PBIE	PBIE7	PBIE6	PBIE5	PBIE4	PBIE3	PBIE2	PBIE1	PBIE0
09h (r/w)	PACON	PACON7	PACON6	PACON5	PACON4	PACON3	PACON2	PACON1	PACON0
0Ah (r/w)	PBCON	PBCON7	PBCON6	PBCON5	PBCON4	PBCON3	PBCON2	PBCON1	PBCON0
0BH(r/w)	INTEN	GIE	--	--	--	SPITXIE	SPIRXIE	T1IE	T0IE
0Ch (r/w)	INTFLAG	PBIF	PAIF	--	--	SPITXIF	SPIRXIF	T1IF	T0IF
0Dh (r/w)	Revered	--	--	--	--	--	--	--	--
0Eh (r/w)	Revered	--	--	--	--	--	--	--	--
0Fh (r/w)	Revered	--							
10h (r/w)	Revered	--	--	--	--	--	--	--	--
11h(r/w)	WDT	WDTE	WDTSL	WDTPS2	WDTPS1	WDTPS0	LVRSL	XOUTS1	XOUTS0
12h(r/w)	PCON	SUSPD	GRN_MD	LVDIS	RSTSL1	RSTSL0	LVDT36	LVDT24	LVDT20
13h(r)	CLKCFG	SELCLK2	SELCLK1	SELCLK0	CLKSW	SIRCEN	INCODS	EXOSEN	IRCEN
14h(r/w)	PWM0CON	P0INTSL	P0DT2	P0DT1	P0DT0	P0CKS2	P0CKS1	P0CKS0	--
15h(r/w)	PWM0CR	PWM0E	P0OUTS	P0TPS2	P0TPS1	P0TPS0	P0TMEN	P0TMIE	P0TMIF
16h(r/w)	P0TMLB	P0TM7	P0TM6	P0TM5	P0TM4	P0TM3	P0TM2	P0TM1	P0TM0
17h(r/w)	P0RDLB	P0TRD7	P0TRD6	P0TRD5	P0TRD4	P0TRD3	P0TRD2	P0TRD1	P0TRD0
18h(r/w)	P0TRHB	P0TM11	P0TM10	P0TM9	P0TM8	P0TRD11	P0TRD10	P0TRD9	P0TRD8
19h(r/w)	PWM1CON	P1INTSL	P1DT2	P1DT1	P1DT0	P1CKS2	P1CKS1	P1CKS0	--
1Ah(r/w)	PWM1CR	PWM1E	P1OUTS	P1TPS2	P1TPS1	P1TPS0	P1TMEN	P1TMIE	P1TMIF
1Bh(r/w)	P1TMLB	P1TM7	P1TM6	P1TM5	P1TM4	P1TM3	P1TM2	P1TM1	P1TM0
1Ch(r/w)	P1RDLB	P1TRD7	P1TRD6	P1TRD5	P1TRD4	P1TRD3	P1TRD2	P1TRD1	P1TRD0
1Dh(r/w)	P1TRHB	P1TM11	P1TM10	P1TM9	P1TM8	P1TRD11	P1TRD10	P1TRD9	P1TRD8
1Eh(r/w)	PWM2CON	P2INTSL	P2DT2	P2DT1	P2DT0	P2CKS2	P3CKS1	P3CKS0	--
1Fh(r/w)	PWM2CR	PWM2E	P2OUTS	P2TPS2	P2TPS1	P2TPS0	P2TMEN	P2TMIE	P2TMIF
20h(r/w)	P2TMLB	P2TM7	P2TM6	P2TM5	P2TM4	P2TM3	P2TM2	P2TM1	P2TM0
21h(r/w)	P2RDLB	P2TRD7	P2TRD6	P2TRD5	P2TRD4	P2TRD3	P2TRD2	P2TRD1	P2TRD0
22h (r/w)	P2TRHB	P2TM11	P2TM10	P2TM9	P2TM8	P2TRD11	P2TRD10	P2TRD9	P2TRD8
23h(r/W)	PWM3CON	P3INTSL	P3DT2	P3DT1	P3DT0	P3CKS2	P3CKS1	P3CKS0	--
24h(r/w)	PWM3CR	PWM3E	P3OUTS	P3TPS2	P3TPS1	P3TPS0	P3TMEN	P3TMIE	P3TMIF
25h(r/W)	P3TMLB	P3TM7	P3TM6	P3TM5	P3TM4	P3TM3	P3TM2	P3TM1	P3TM0
26h(r/W)	P3RDLB	P3TRD7	P3TRD6	P3TRD5	P3TRD4	P3TRD3	P3TRD2	P3TRD1	P3TRD0
27h(r/W)	P3TRHB	P3TM11	P3TM10	P3TM9	P3TM8	P3TRD11	P3TRD10	P3TRD9	P3TRD8
28h(r/w)	ADCON-1	ADCEN	ADCST	CHSL2	CHSL1	CHSL0	--	ADCSR1	ADCSR0
29h(r/w)	ADCON-2	ADCIE	ADCIF	SVERFH	ADCNT	DACOEN	ADCTMS	SELVER1	SELVER0
30h(r/w)	ADCHB	ADCB[11]	ADCB[10]	ADCB[9]	ADCB[8]	ADCB[7]	ADCB[6]	ADCB[5]	ADCB[4]
31h(r/W)	ADCLB	--	--	--	--	ADCB[3]	ADCB[2]	ADCB[1]	ADCB[0]

Legend: - = unimplemented, read as '0',

Table 1.7-3 I/O Register Summary of F-Plane

Register Name	I/O Address	Default(Reset)	Description	Fig.
INDF	00h (R/W)	8'h00	Uses contents of FSR to address data memory	P.14
Revered	01h (R/W)	8'h00	--	--
PCL	02h (R/W)	8'h00	Low bytes of Program Counter	P.15
STATUS	03h (R/W)	8'h00	Status Register	P.16
FSR	04h (R/W)	8'h00	File select Register	P.15
PORTA	05h (R/W)	8'h00	Port A data input/output	P.17
PORTB	06h (R/W)	8'h00	Port B data input/output	P.17
PAIE	07h (R/W)	8'h03	Port A Interrupt Control Register	P.19
PBIE	08h (R/W)	8'hC0	Port B Interrupt Control Register	P.19
PACON	09h (R/W)	8'h00	Port A Wake-up Control Register	P.20
PBCON	0Ah (R/W)	8'h00	Port B Wake-up Control Register	P.21
INTEN	0BH(R/W)	8'h00	Interrupt Mask Register	P.51
INTFLAG	0Ch (R/W)	8'h00	Interrupt Flag Register	P.52
Revered	0Dh (R/W)	8'h00	--	--
Revered	0Eh (R/W)	8'h00	--	--
Revered	0Fh (R/W)	8'h00	--	--
Revered	10h (R/W)	8'h00	--	--
WDT	11h(R/W)	8'h00	Watch Dog Timer	P.25
PCON	12h(R/W)	8'h00	Power Control register	P.27
CLKCFG	13h(R/W)	8'h09	Clock Configuration status	P.29
PWM0CON	14h(r/w)	8'h00	PWM0 configuration Register	P.35
PWM0CR	15h(r/w)	8'h00	PWM0 Control Register	P.36
P0TMLB	16h(r/w)	8'h00	PWM0 Timer Low byte Register	P.36
P0RDLB	17h(r/w)	8'h00	PWM0 Timer compared reload Low value Register	P.37
P0TRHB	18h(r/w)	8'h00	PWM0 Timer and reload high-Nibble byte	P.37
PWM1CON	19h(r/w)	8'h00	PWM1 configuration Register	P.38
PWM1CR	1Ah(r/w)	8'h00	PWM1 Control Register	P.39
P1TMLB	1Bh(r/w)	8'h00	PWM1 Timer Low byte Register	P.39
P1RDLB	1Ch(r/w)	8'h00	PWM1 Timer compared reload Low byte Register	P.39
P1TRHB	1Dh(r/w)	8'h00	PWM1 Timer and reload high-Nibble byte	P.40
PWM2CON	1Eh(r/w)	8'h00	PWM2 configuration Register	P.41
PWM2CR	1Fh(r/w)	8'h00	PWM2 Control Register	P.42
P2TMLB	20h(r/w)	8'h00	PWM2 Timer Low byte value Register	P.43
P2RDLB	21h(r/w)	8'h00	PWM2 Timer compared reload Low byte Register	P.43
P2TRHB	22h (r/w)	8'h00	PWM2 Timer and reload high-Nibble byte	P.43
PWM3CON	23h(r/W)	8'h00	PWM3 configuration Register	P.44
PWM3CR	24h(r/w)	8'h00	PWM3 Control Register	P.45
P3TMLB	25h(r/W)	8'h00	PWM3 Timer Low byte value Register	P.46
P3RDLB	26h(r/W)	8'h00	PWM3 Timer compared reload Low byte Register	P.46
P3TRHB	27h(r/W)	8'h00	PWM3 Timer and reload high Nibble-byte	P.46
ADCON-1	28h(r/w)	8'h00	ADC Control-1 Register	P.47
ADCON-2	29h(r/w)	8'h00	ADC Control-2 Register	P.48
ADCHB	30h(r/w)	8'h00	ADC High byte Register	P.49
ADCLB	31h(R/W)	8'h00	ADC Low nibble-byte Register	P.49

Table 1.7-4 I/O Register Summary of R-Plane (Accessed by IOST/IOSTR instruction)

Register Name	I/O Address	Default(Reset)	Description	Fig.
PAMODE0	08h (R/W)	8'h00	Port A Mode0 Control Register	23
PAMODE1	09h (R/W)	8'h00	Port A Mode1 Control Register	23
PBMODE0	0Ah (R/W)	8'h00	Port B Mode0 Control Register	23
PBMODE1	0Bh (R/W)	8'h00	Port B Mode1 Control Register	23
PADRVMD0	0Ch (R/W)	8'h00	Port A Drive High Strength Mode0 Control Register	24
PADRVMD1	0Dh (R/W)	8'h00	Port A Drive High Strength Mode1 Control Register	24
PBDRVMD0	0Fh (R/W)	8'h00	Port B Drive High Strength Mode0 Control Register	24
PBDRVMD1	10h (R/W)	8'h00	Port B Drive High Strength Mode1 Control Register	24

1.8 Table of Optional configuration

<table>
<tr><th>Config Name</th><th>Description</th><th>Default</th></tr>
<tr><td>SELXOUT[1:0]</td><td>Select IRC output Clock
<table>
<tr><td>SLEXOUT [1:0]</td><td>Freaquency</td></tr>
<tr><td>2’b11</td><td>Firc = 16Mhz</td></tr>
<tr><td>2’b10</td><td>Firc/2 = 8Mhz</td></tr>
<tr><td>2’b01</td><td>Firc/4 = 4Mhz</td></tr>
<tr><td>2’b00</td><td>Firc /8 = 2Mhz</td></tr>
</table></td><td>2b11</td></tr>
<tr><td>SLEXCLK</td><td>Select External Clock
<table>
<tr><td>SLEXCLK [1:0]</td><td>External clock source</td></tr>
<tr><td>2’b11</td><td>Use internal IRC</td></tr>
<tr><td>2’b10</td><td>Select external OSC</td></tr>
<tr><td>2’b01</td><td>Select external RC</td></tr>
<tr><td>2’b00</td><td>Select external crystal</td></tr>
</table></td><td>2’b11</td></tr>
<tr><td>SelCpuClk[2:0]</td><td>Select Fcpu = (Fosc or FIRC)/N clock
<table>
<tr><td>SelCpuClk[2:0]</td><td>N</td></tr>
<tr><td>3’b1xx</td><td>16</td></tr>
<tr><td>3’b011</td><td>8</td></tr>
<tr><td>3’b010</td><td>4</td></tr>
<tr><td>3’b001</td><td>2</td></tr>
<tr><td>3’b000</td><td>1</td></tr>
</table></td><td>3’b111</td></tr>
<tr><td>C_XTAL</td><td>Crystal buffer</td><td>4’b1111</td></tr>
<tr><td>INSWDY</td><td>Internal clock switch to external clock delay time
1 = 128us delay
0 = 4ms delay</td><td>1’b1</td></tr>
<tr><td>WDTSEL</td><td>Watch dog time out select
WDTSEL[1:0] : 2’b00 = 126 ms
2’b01 = 504 ms
2’b10 = 8 ms
2’b11 = 32 ms</td><td>2’b11</td></tr>
<tr><td>XTAL32KENB</td><td>1: 16M XTAL 0: 32Khz When SLEXCLK=2’b00</td><td>1’b1</td></tr>
<tr><td>selPor</td><td>Power on reset extend timing
SelPor[1:0] : 2’b00 = 660us
2’b01 = 4 ms
2’b10 = 8 ms
2’b11 = 16 ms</td><td>11</td></tr>
<tr><td>PROTECT</td><td>1: No protect ROM code protect = ~OTP[0](OTP[0] default = 1)
0: Protect ROM code</td><td>1→ no protect</td></tr>
</table>

【2】 Macro-Controller UNIT

2.1 Indirect Addressing Define

The INDF Register is not a physical register .Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly(FSR="0") will read 8'h00.Writing to the INDF register indirectly results in a no-operation.
The bits 6~0 of FSR register can be select up to 128 registers by accessed.(address 00~7fh).

Address 00H : Indirect Addressing Register (INDF)

Bits	7	6	5	4	3	2	1	0
Name	Uses contents of FSR to address data memory							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Address 04H :File select Register(FSR)

Bits	7	6	5	4	3	2	1	0
Name	File select register to define address in indirect addressing mode							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Example : How to used instruction at Indirect addressing
(1) Write AA data to Register (address=8'h50h)

```
MOVIA    80h
MOVAR    FSR        ;  Register address pointer is 80h
MOVIA    AAh
MOVAR    INDF       ; Move  data = AAh to address = 80h register
```

(2)Read register(50h) to ACC

```
MOVIA    80h
MOVAR    FSR        ;  Register address pointer is 80h
MOVR     INDF,A     ; Move  contents of register(80h) to ACC
```

2.2 Program Counter least significant 8 bits

A special computed GOTO is accomplished by adding an offset to the program counter (ADDAR PCR,R). When doing a table read using this method, care should be taken if the table location crosses a PCL memory boundary(256 word block).

Address 02H: Low bytes of Program Counter(PCL)

Bits	7	6	5	4	3	2	1	0
Name	Uses contents of FSR to address data memory							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Example : Create table

```
            MOVR   TABLECNT,A
             CALL    TABLE1
              .
              .
TABLE1    : ADDAR    PCL,R        ;  PCL = TABLECNT
             RETIA      00h        ; PC={ PC[10:8],PC[7:0] = PCL+ PC[7:0]}  → When  TABLECNT=0
             RETIA      01H        ; PC={ PC[10:8],PC[7:0] = PCL+ PC[7:0]}  → When TABLECNT=1
             RETIA      02H        ; PC={ PC[10:8],PC[7:0] = PCL+ PC[7:0]}  → When TABLECNT=2
             RETIA      02H        ; PC={ PC[10:8],PC[7:0] = PCL+ PC[7:0]}  → When TABLECNT=3
```

2.3 Status Register

This register contains the arithmetic status of the ALU, the RESET status.
If the STAUTS Register the destination for an instruction the affects the Z,DC or C bits, then the write to these three bits disabled. These bits are set or cleared according to the logic. Furthermore, the /TO and /PD bits are not writable.

Address 03H: Status Register(STATUS)

Bits	7	6	5	4	3	2	1	0
Name	Revered	Revered	Revered	/TO	/PD	Z	DC	C
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[4] : /TO
WDT overflow flag bit.
1 = After power on or by the CLRWDT or SLEEP instruction.
0 = A watch-dog time overflow.

Bit[3] : /PD
Power down flag flag.
1 = After power on or by the CLRWDT instruction.
0 = By the SLEEP instruction.

Bit[2] : Z
Zero flag
1 = The result of a logic operation is zero.
0 = The result of a logic operation is not zero.

Bit[1] : DC
Decimal carry flag or decimal/borrow flag
ADDAR, ADDIA
1 = A carry from the 4th low order bit of the result occurred.
0 = A carry from the 4th low order bit of the result did not occurred.
SUBAR,SUBIA
1 = A borrow from the 4th low order bit of the result did not occurred.
0 = A borrow from the 4th low order bit of the result occurred.

Bit[0] : C
Carry flag or borrow flag.
ADDAR, ADDIA, RLR
1 = A carry occurred.
0 = A Carry did not occurred.
SUBAR, ADDIA, RRR
1 = A borrow did not occurred.
0 = A borrow occurred.

2.4 General Purpose I/O ports

Ports A are 8 bits I/O register. Ports B are 8 bits I/O register ,each bit can also selected as an external interrupt source for the microcontroller.

***Figure* 2-4.1** shows a diagram of a GPIO port pin.

Refer **TABLE 2.4.3-1** and **TABLE 2.4.5-1** , each pin can be independently configured as high-impedance inputs, inputs with internal pull-ups, open drain outputs, or traditional output s with selectable drive strength.

After reset, all GPIO data and controlled mode register is cleared, so the GPIO pins are as input mode.

2.4.1 PortA, PortB data define

Address 05H : Port A(PORTA)

Bits	7	6	5	4	3	2	1	0
Name	PORTA[6:0] data input/ouput							
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0]: PA[7:0]

1 = Port pin is logic HIGH

0 = Port pin is logic LOW

Address 06H : Port B(PORTB)

Bits	7	6	5	4	3	2	1	0
Name	PORTB[6:0] data input/ouput							
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0]: PB[7:0]

1 = Port pin is logic HIGH

0 = Port pin is logic LOW

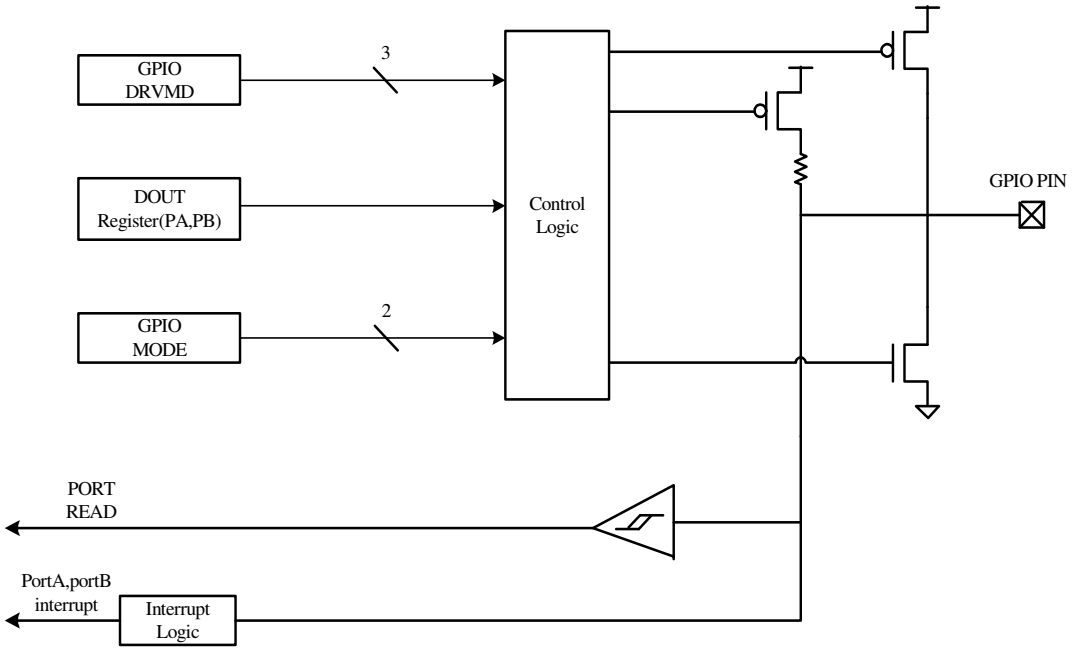


Figure 2.4-1 Block diagram of GPIO Port

2.4.2 PortA, PortB Interrupt define

Address 07H : Port A Interrupt Control Register (PAIE)

Bits	7	6	5	4	3	2	1	0
Name	--	PAIE6	PAIE5	PAIE4	PAIE3	PAIE2	PAIE1	PAIE0
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[6] : PAIE6
PA[6] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[5] : PAIE5
PA[5] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[4] : PAIE4
PA[4] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[3] : PAIE3
PA[3] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[2] : PAIE2
PA[2] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[1] : PAIE1
PA[1] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[0] : PAIE0
PA[0] interrupt enable bit.
1 = Enable.
0 = Disable.

Address 08H : Port B Interrupt Control Register (PBIE)

Bits	7	6	5	4	3	2	1	0
Name	--	PBIE6	PBIE5	PBIE4	PBIE3	PBIE2	PBIE1	PBIE0
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[6] : PBIE6
PB[6] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[5] : PBIE5
PB[5] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[4] : PBIE4

PB[4] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[3] : PBIE3
PB[3] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[2] : PBIE2
PB[2] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[1] : PBIE1
PB[1] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[0] : PBIE0
PB[0] interrupt enable bit.
1 = Enable.
0 = Disable.

Address 09H : Port A Wake-up Control Register (PACON)

Bits	7	6	5	4	3	2	1	0
Name	PACON7	PACON6	PACON5	PACON4	PACON3	PACON2	PACON1	PACON0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[6] : PACON6
PA[6] control bit.
1 = PA[6] Pin-changed to interrupt.
0 = PA[6] falling edge to interrupt.

Bit[5] : PACON5
PA[5] control bit.
1 = PA[5] Pin-changed to interrupt.
0 = PA[5] falling edge to interrupt.

Bit[4] : PACON4
PA[4] control bit.
1 = PA[4] Pin-changed to interrupt.
0 = PA[4] falling edge to interrupt.

Bit[3] : PACON3
PA[3] control bit.
1 = PA[3] Pin-changed to interrupt.
0 = PA[3] falling edge to interrupt.

Bit[2] : PACON2
PA[2] control bit.
1 = PA[2] Pin-changed to interrupt.
0 = PA[2] falling edge to interrupt.

Bit[1] : PACON1
PB[1] control bit.
1 = PA[1] Pin-changed to interrupt.
0 = PA[1] falling edge to interrupt.

Bit[0] : PACON0

PA[0] control bit.

1 = PA[0] Pin-changed to interrupt.

0 = PA[0] falling edge to interrupt

Address 0AH : Port B Wake-up Control Register (PBCON)

Bits	7	6	5	4	3	2	1	0
Name	PBCON7	PBCON6	PBCON5	PBCON4	PBCON3	PBCON2	PBCON1	PBCON0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[6] : PBCON6

PB[6] control bit.

1 = PB[6] Pin-changed to interrupt.

0 = PB[6] falling edge to interrupt.

Bit[5] : PBCON5

PB[5] control bit.

1 = PB[5] Pin-changed to interrupt.

0 = PB[5] falling edge to interrupt.

Bit[4] : PBCON4

PB[4] control bit.

1 = PB[4] Pin-changed to interrupt.

0 = PB[4] falling edge to interrupt.

Bit[3] : PBCON3

PB[3] control bit.

1 = PB[3] Pin-changed to interrupt.

0 = PB[3] falling edge to interrupt.

Bit[2] : PBCON2

PB[2] control bit.

1 = PB[2] Pin-changed to interrupt.

0 = PB[2] falling edge to interrupt.

Bit[1] : PBCON1

PB[1] control bit.

1 = PB[1] Pin-changed to interrupt.

0 = PB[1] falling edge to interrupt.

Bit[0] : PBCON0

PB[0] control bit.

1 = PB[0] Pin-changed to interrupt.

0 = PB[0] falling edge to interrupt

2.4.3 PortA, PortB Mode define

08H : Port A Mode0 Control Register(PAMODE0)

Bits	7	6	5	4	3	2	1	0
Name	--	PAM0-6	PAM0-5	PAM0-4	PAM0-3	PAM0-2	PAM0-1	PAM0-0
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PA [7:0] Mode0

1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 0 is logic LOW

09H : Port A Mode1 Control Register(PAMODE1)

Bits	7	6	5	4	3	2	1	0
Name	--	PAM1-6	PAM1-5	PAM1-4	PAM1-3	PAM1-2	PAM1-1	PAM1-0
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PA [7:0] Mode 1

1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 0 is logic LOW

0AH : Port b Mode1 Control Register(PBMODE0)

Bits	7	6	5	4	3	2	1	0
Name	--	PBM0-6	PBM0-5	PBM0-4	PBM0-3	PBM0-2	PBM0-1	PAM0-0
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PB [7:0] Mode 0

1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 0 is logic LOW

0BH : Port B Mode1 Control Register(PBMODE1)

Bits	7	6	5	4	3	2	1	0
Name	--	PBM1-6	PBM1-5	PBM1-4	PBM1-3	PBM1-2	PBM1-1	PBM1-0
Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PB [7:0] Mode 1

1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 0 is logic LOW

Each pin of PORTA,PORTB mode is define by as follows **TABLE 2.4.3-1 :**

TABLE 2.4.3-1 Port A and B Output control truth Table

Data register	Mode1	Mode0	Output Drive Strength
1	0	0	HI-z(Input mode)
0			
1	0	1	Normal Drive(Refer **TABLE 2.4.3-2)**
0			Sink (8mA)
1	1	0	Resistive(100KΩ)
0			Sink (2mA)
1	1	1	Normal Drive(Refer **TABLE 2.4.3-2)**
0			Sink (20mA)

2.4.4 PortA, PortB Drive define

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ch (w)	PADRVMD0	Port A Drive High Strength Mode Control Register							
0Dh (w)	PADRVMD1								
0Fh (w)	PBDRVMD0	Port B Drive High Strength Mode Control Register							
10h(w)	PBDRVMD1								

Accessed by IOST/IOSTR instruction

Each pin of Port A , B drive high is define by as follows **Table TABLE 2.4.3-2**

TABLE TABLE 2.4.3-2 PortA and B Output Drive Strength Truth Table

PADRVMD1	PADRVMD0	Output Drive Current
0	0	Drive high 20mA
0	1	Drive high 8mA
1	0	Drive high 2mA
1	1	Non Drive high

2.5 Watchdog Timer(WDT)

The Watchdog Timer (WDT) is a free running on chip RC oscillator which dose not require any external components. So the WDT will still run into SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause base on Configuration option to the device reset .

Configuration WDTSEL[1:0]	VDD=5V SIRC = 32Khz,WDT Time out	VDD=3V SIRC = 16Khz
2'b11	18 ms	18X2 ms
2'b10	4.5 ms	4.5X2 ms
2'b01	288 ms	288X2 ms
2'b00	72 ms	72X2 ms

The CLRWDT instruction clears the WDT , if assigned to the WDT, and prevents it from timing out and generating a device reset.
The WDT can be disabled by clearing the control bit WDTE(08h-7). The WDT has a normal time-out period of 18ms(without precaler). When the SLEEP instruction executes , the WDT and the prescaler will be reset.
The prescaler of WDT refers **Table2.5-1**.
The block diagram of WDT shows in ***Figure* 2.5-2**.

Address 11h Watchdog Timer(WDT)

Bits	7	6	5	4	3	2	1	0
Name	WDTE	WDTSL	WDTPS[2:0]			LVRSL	XOUTS[1]	XOUTS[0]
Read/Write	R/W	R/W	R/W			R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit[7] : WDTE
Watch-Dog timer enable.
1 = Enable.
0 = Disable.
Bit[6] : WDTSL
Watch-dog timer out select .
1 = If Watch-dog timer out ,the Device be reset.(PC = 0000h)
0 = If Watch-dog timer out ,Device be wake up and PC = PC+1.(SUSPEN bit in 12h register be clear)

Bit[5:3] : WDTPS[2:0]
WDT Prescaler, Please refer **Table 2.5-1**.

WDTPS[2:0]	WDT time out
3'b000	18ms*1 = 18ms
3'b001	18ms*2 = 36ms
3'b010	18ms*4 = 72ms
3'b011	18ms*8 = 144ms
3'b100	18ms*16 = 288ms
3'b101	18ms*32 = 572ms
3'b110	18ms*64 = 1152ms
3'b111	18ms*128 = 2304ms

TABLE 2.6-1 WDT Prescaler

Bit[2] : LVRSL

LVR select .

1 = When system is in Power_down(Suspend) mode , LVR will be clear SUSPEND bit .

0 = When system is in Power_down(Suspend) mode , LVR will be reset system chip.

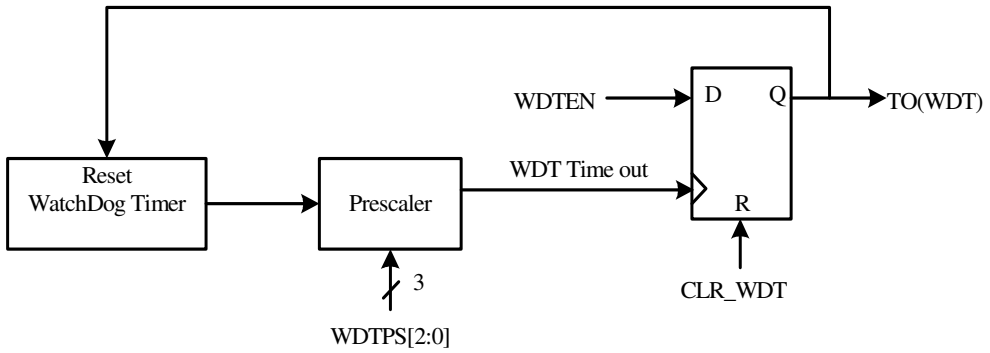


Figure **2.5-2 Block Diagram of WDT**

【3】 Power and Reset Management

There are Four cases of reset on USB controller chip. These cases of reset occurrence are listed below.

1. Power On Reset
   - ◆ POR (VDD ≤ 1.8V)
2. Brown out reset
   - ◆ LVDT20 (VDD ≤ V_{LVR1} ==2.4V for > 100ns)
   - ◆ LVDT24 (VDD ≤ V_{LVR2} ==2.0V for > 100ns)
3. Watchdog Reset
   - ◆ WDR (Watch Dog time out)
4. External Reset
   - ◆ EXTR (Low active)

If the POR,WDR, LVDT20 , LVDT24 or EXR occurs, the chip will enter reset status. The following events take place on reset status.

- ◆ All registers are reset to their default values expect status registers.
- ◆ The status register (03h) is reset to their default value only for PORN .
- ◆ After reset status, program counter begins at address 0x0000.

PORN is asserted when VDD voltage to the device is upper approximately 1.8V(see *Figure* 3.0-1).

Address 12H : Power Control Register (PCON)

Bits	7	6	5	4	3	2	1	0
Name	SUSPEND	GREEN_MD	LVDIS	RSTSL[1:0]		LVDT36	LVDT24	LVDT20
Read/Write	R/W	R/W	R/W	R/w	R/W	R	R	R
Default	0	0	0	0	0	0	0	0

Bit][7] : SUSPEND

F/W force System Chip to go into suspend mode.

1 = suspend mode.

0 = The other operation mode.

Bit][6:5] : GREEN_MD,LVDIS

{ GREEN_MD,LVDIS}	Description
2'b00	Normal Mode(SUSPEND=0) , and All LVD36,LVDT24,LVDT20 circuit are enable
2'b01	First switch Fcpu clock is Fsirc. Slow Mode(SUSPEND=0), and All LVD36,LVDT24,LVDT20 circuit are disable Fcpu enable(Fcpu = Fsirc),
2'b10	Green Mode(SUSPEND=0) , and All LVD36,LVDT24,LVDT20 circuit are enable Fcpu Disable.
2'b11	Green Mode(SUSPEND=0) , and All LVD36,LVDT24,LVDT20 circuit are disable Fcpu Disable.

Bit[4:3] : RST[1:0]

RSTSL[1:0]	Description
2'b00	POR,WDR can reset system chip.
2'b01	POR,WDR, LVDT20 (VDD<= 2.0V) can reset system chip
2'b10	POR,WDR ,LVDT24 (VDD<= 2.4V) can reset system chip
2'b11	POR,WDR ,EXR can reset system chip.

Bit[2] : LVDT36

Low Voltage(3.6V) detect signal.(when LVDEN == 2'b11,2'b00).

1 = VDD voltage > 3.6V.

0 = VDD voltage <= 3.6 V

Bit[1] : LVR24

Low Voltage(2.4V) detect signal.(when LVDEN == 2'b10,2'b00).

1 = VDD voltage > 2.4V.

0 = VDD voltage <=2.4 V

Bit[1] : LVR20

Low Voltage(2.0V) detect signal.(when LVDEN == 2'b01,2b00).

1 = VDD voltage > 2.0V.

0 = VDD voltage <= 2.0 V

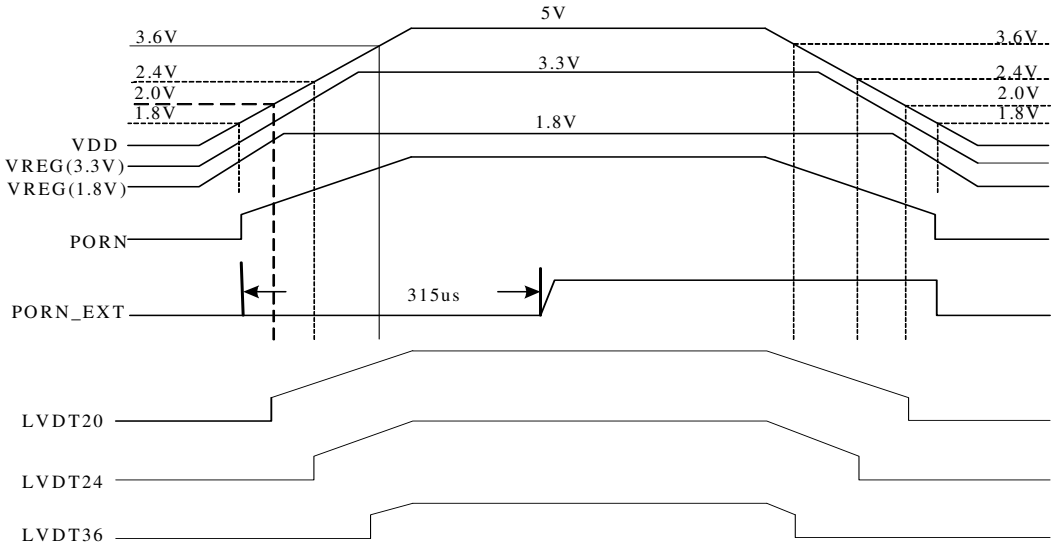


***Figure* 3.0-1 Power on Reset and LVD20,LVDT24,LVDT36 Timing**

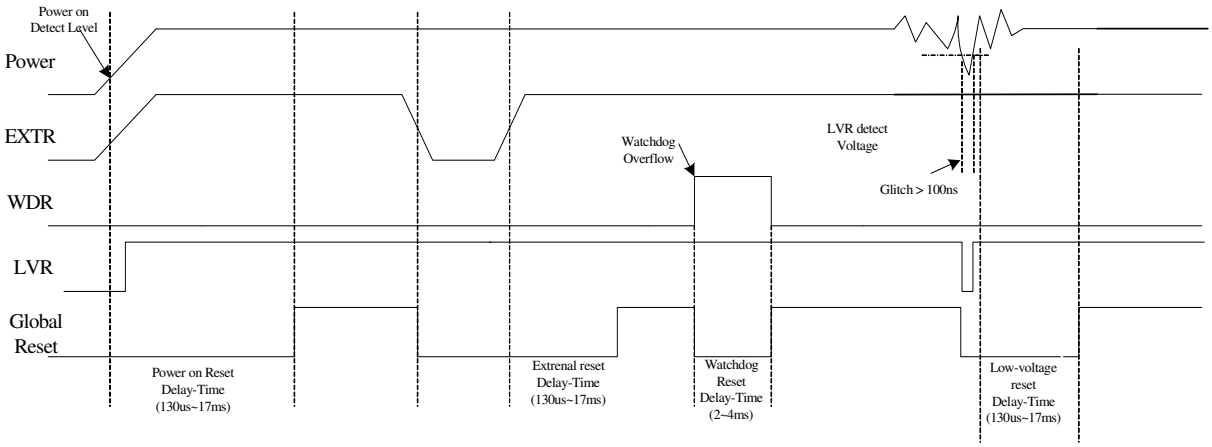


***Figure* 3.0-2 Global Timing**

【4】 Clock Control

Address 1AH : Clock configuration (CLKCFG)

Bits	7	6	5	4	3	2	1	0
Name	SELCLK[2:0]			CLKSW	SIRCEN	INCODS	EXOSEN	IRCEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	0	0	1

Bit[7:5] : SELCLK[2:0]

Select MCU switch-clock .

SELCLK[2:0]	Select clock(Fsel)
3'b000	(FOSC or FIRC)/1
3'b001	(FOSC or FIRC)/2
3'b010	(FOSC or FIRC)/4
3'b011	(FOSC or FIRC)/8
3'b100	(FOSC or FIRC)/16
3'b101	FSIRC

Bit[3] : CLKSW

CPU clock switch

1 = CPU clock start to switch from F_{fig} clock to F_{sel} clock.

0 = CPU clock start to switch from F_{sel} clock to F_{fig} clock.

Bit[3] : SIRCEN

Enable Slow IRC clock(32KHz).

1 = Enable slow IRC clock.

0 = Disable slow IRC clock.

Bit[2] : INCODS

Internal clock output disable.

1 = Disable internal IRC clock output. XOUT pin will dive high.

0 = Enable internal IRC clock output. The IRC clock is driven output to XOUT pin.

Bit[1] : EXOSEN

External Oscillator Enable.

1 = Enable the external oscillator . The Fcpu clock is switch to external clock(Fosc) from FIRC clock.

0 = Disable Oscillator Enable.

Bit[0] : IRCEN

Internal clock enable.

1 = Enable internal clock

0 = Disable internal clock.

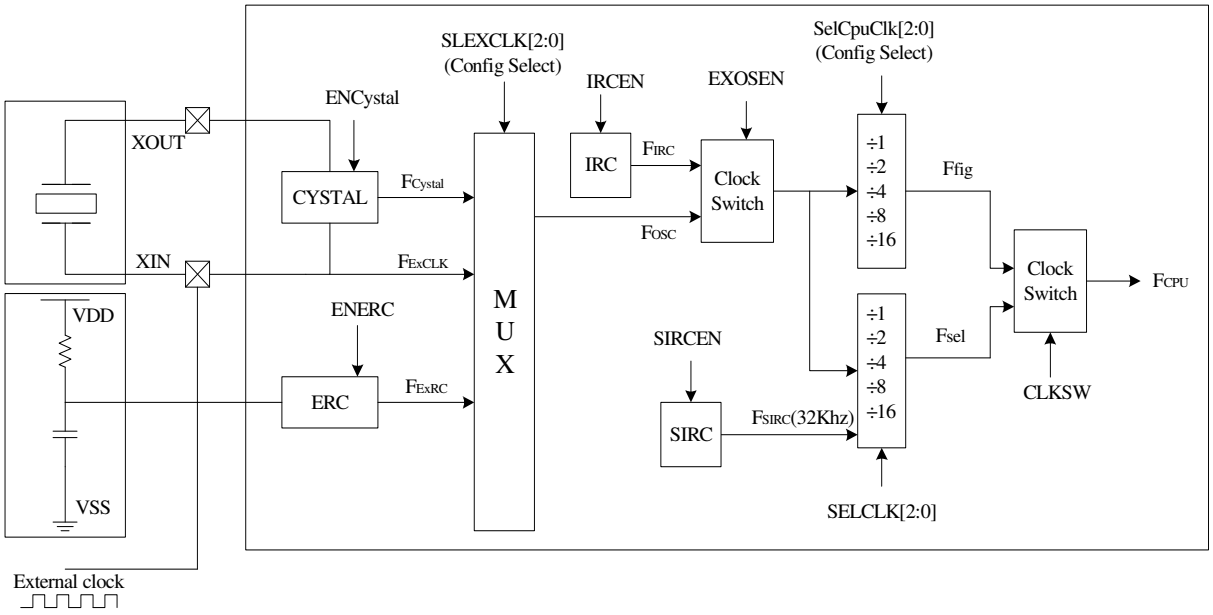


***Figure* 4.0-1 Clock Switch Block diagram**

Note : (1) ENCystal = (SLEXCLK[1:0] == 2'b00)&EXOSEN
(2) ENERC = (SLEXCLK[1:0] == 2'b01)&EXOSEN

Example : Clock Switch demo code(MCU clock is 16Mhz when selCpuClk == 3'b000)
Switch MCU clock from Ffig to Fsel, and then need return to default clock and then switch to 58Khz

```
BCR     CLKCFG , SELCLK2_B
BCR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B
MOVAR   CLKCFG                  // Select clock is  Fsel  (Fosc,FIRC/2)
BSR   PCON,CLKSW                // Fcpu is switch to Fsel

.
.
BCR   PCON, CLKSW               //  Fcpu switch to Ffig.
BSR     CLKCFG , SELCLK2_B
BCR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B      // Select clock is  Fsel  (FSIRC)

BSR   PCON,CLKSW   ; Fcpu is switch to  FSIRC 32KHz(Now Fcpu = 32Khz)
```

【5】 System Operating Mode

5.1 Overview

The FM8PC71A support a versatile low-power operation mode as bellows:

1. Normal Mode.
2. Slow Mode.
3. Green Mode.
4. Suspend Mode

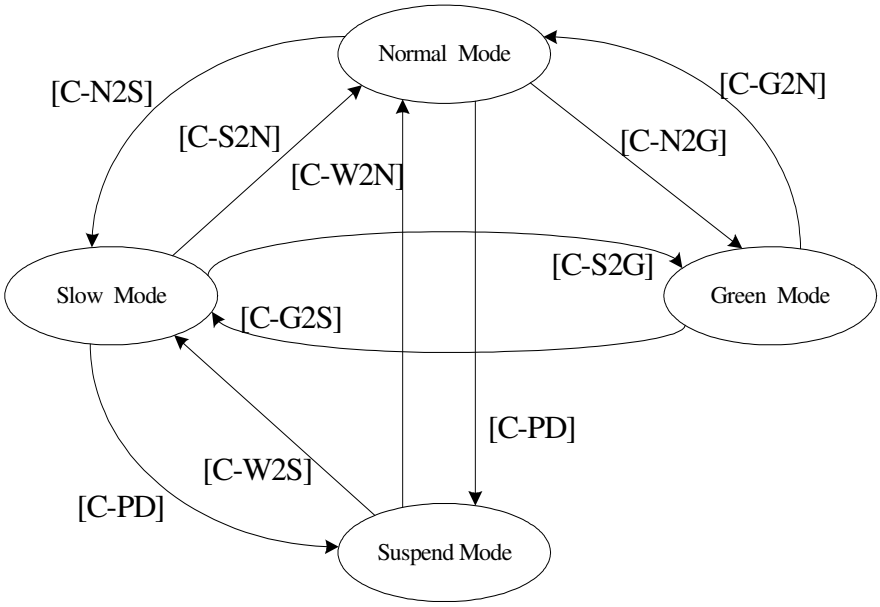


***Figure* 5.1-1 System Switch Mode Block diagram**

Condition Description for System switch mode :

[C-PD] : Normal mode or Slow mode into Power down condition.
Set SUSPEND (Reg.12h.7) bit to 1

Example:
BSR PCON, SUSPEND_B

[C-W2N] : Suspend mode wakeup to Normal mode condition.
(1) PA, PB wakeup interrupt.
(2) LVR or external Reset occurs.

Note : If system is from Normal mode to suspend mode, the system will be from suspend mode to normal mode when wakeup interrupt occurs.

[C-W2S] : Suspend mode wakeup to Slow mode condition.
(1) PA, PB wakeup interrupt.
(2) LVR or external Reset occurs.

Note : If system is from Slow mode to suspend mode, the system will be from suspend mode to Slow mode when wakeup interrupt occurs.

[C-N2S] : Normal mode into Slow mode condition.
First, the firmware needs to switch CPU clock, the CPU clock will be from FIRC/FOSC to FSIRC.
Next, set LVDIS (Reg.12h.5) bit to 1

Example code:

```
BSR    CLKCFG, SELCLK2_B          // set Fcpu = FSIRC (SELCLK=3'b101)
BCR    CLKCFG, SELCLK1_B
BSR    CLKCFG, SELCLK0_B
BSR    CLKCFG, CLKSW_B            // switch CPU clock
NOP

BSR    PCON, LVDIS_B
```

[C-S2N] : Slow mode into normal mode condition.
When the firmware switches CPU clock from FSIRC to FIRC/FOSC and sets LVDIS (Reg.12h.5) bit to 0.

Example code:

```
BSR    CLKCFG, CLKSW_B            // switch CPU clock
BSR    PCON, LVDIS_B
```

[C-N2G] : Normal mode into Green mode condition.
Green mode is sort into two types. Their difference is one disables all LVD36, LVD24, LVD20 and internal high IRC, and another not.

Example code for enabling all low voltage detect and internal high IRC:

```
BSR    PCON,GREEN_MD_B        //set GREEN_MD bit to 1
```

Example code for disabling all low voltage detect and internal high IRC :

```
MOVIA    0b01100000           //set GREEN_MD and LVDIS bit to 1 at the same time
MOVAR   PCON
```

[C-G2N] : Green mode into normal mode condition.
(1) PA,PB wakeup interrupt.
(2) LVR or external Reset occurs.
(3) WDT time out interrupt.
(4) 4 timers time out interrupt.

[C-S2G] : Slow mode into Green mode condition.
Slow mode only can be changed into the Green mode that disable all low voltage detect, because Slow mode always disable low voltage detect. Set GREEN_MD (Reg.12h.6) bit to 1 and enter Green mode.

Example:

```
BSR    PCON, GREEN_MD_B
```

[C-G2S] : Green mode into Slow mode condition.

(1) PA,PB wakeup interrupt.
(2) LVR or external Reset occurs.
(3) WDT time out interrupt.
(4) 4 timers time out interrupt.

Note : If system is from Slow mode to Green mode, the system will be from Green mode to Slow mode when wakeup interrupt occurs.

Operating Mode Description

MODE / Module	Normal Mode	Slow Mode	Green Mode	Suspend Mode (Power down Mode)
FOSC	Running (EXOSEN =1)	Disable or enable (by EXOSEN)	Disable (EXOSEN = 0 or 1)	Disable (EXOSEN = 0 or 1)
FIRC	Running (IRCEN = 1)	Disable or enable (by IRCEN)	Disable (IRCEN = 0 or 1)	Disable (IRCEN = 0 or 1)
FSIRC	Running (SIRCEN = 1)	Running (SIRCEN = 1)	Running (SIRCEN = 1)	Disable (SIRCEN = 0)
WDT	Running (WDTE = 1, WDTSL=0)	Running (WDTE = 1, WDTSL=0)	Running (WDTE = 1, WDTSL=1)	Disable (WDTE = 0, WDTSL=0)
Internal Interrupt	All enable	All enable	All enable	All enable
External Interrupt	All enable	All enable	All enable	All enable
Wakeup even	--	--	All PA,PB interrupt Timer, WDT time output , Reset	All PA,PB interrupt Reset
SUSPEND bit	0	0	0	1
{Green,LVDIS} (In Reg-12h)	2'b00	2'b01	2'b10,2'b11	2'bxx
PC of MCU	Work	Work	Stop	Stop
Clock of MCU	FOSC or FIRC	FSIRC	Non clock	Non clock

【6】 PWM Description

6.0 PWM Overview

The PWM0, PWM1,PWM2 and PW3 modules are pulse modulator combined with 12-bit generator. The FM8PC71A supports four channels PWM0(PA[3]) , PWM1(PA[4]) , PWM2(PA[6])and PWM3(PA[7]) output. The PWM output timing is as follow **Figure 8-1**.

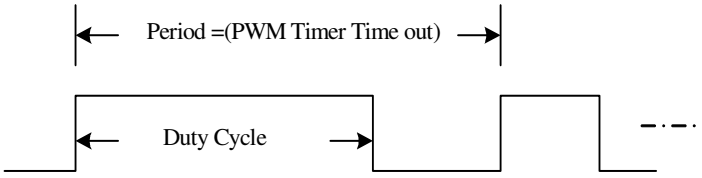


Figure 6-1 PWM Timing

Duty cycle is define by as following:

Duty Cycle = (TMRLD == PWM counter);

Period calibrated :

(A) As PWM mode : (PWMXEN=1,PXTMEN=1):

Period = (PWM counter == $2^{Timer-bits}$) * (T_{p0ck})

Example : **P0DT[2:0] = 3'b001 (select 4-bit counter) and P0CKS[2:0] = 3'b001**

Period = 2^4 * 1/2 * 1/ F_{IRC} = 16 * 1/2 * 62.5ns = 500 ns

(B) As Timer mode : (PWMXEN=0,PXTMEN=1):

Period = (PWM counter == TMRLD) * (T_{p0ck})

Example : **P0DT[2:0] = 3'b001 (select 4-bit counter) , P0CKS[2:0] = 3'b001 and TMRLD=4**

Period = 4 * 1/2 * 1/ F_{IRC} = 4 * 1/2 * 62.5ns = 250 ns

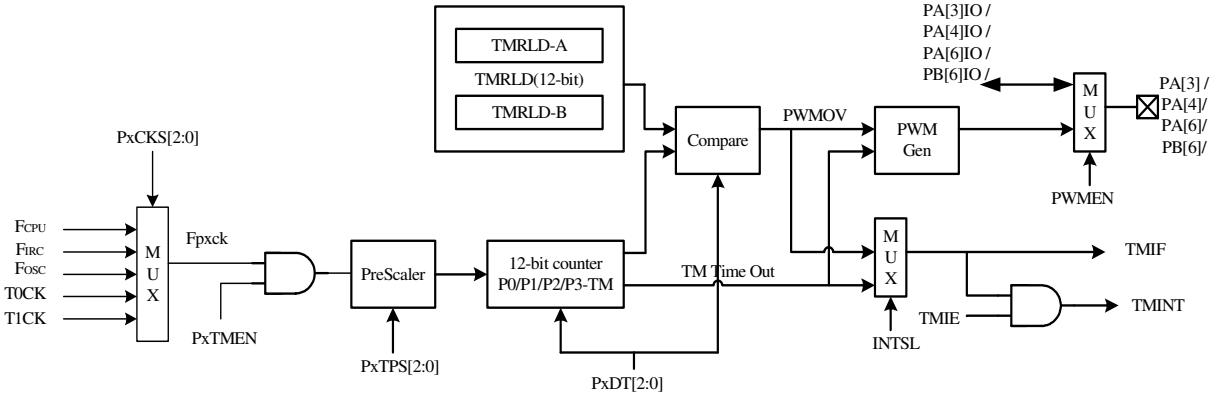


Figure 6-2 PWM Block diagram

6.1 PWM0 Register

Address 14H: PWM0 configuration Register(PWM0CON)

Bits	7	6	5	4	3	2	1	0
Name	P0INTSL	P0DT[2:0]			P0CKS[2:0]			Revered
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P0INTSL

PWM0 interrupt selection.

1 = Select interrupt for PWM0 overflow.

0 = Select interrupt for PWM0 timer time out.

Bit[6:4] :P0DT[2:0]

PWM0 Duty Range.

P0DT[[2:0],	PWM0 Duty Range		PWM0 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-3 PWM0 Duty Range

Bit[3:1] : P0CKS

PWM0 Timer clock select.

P0CKS[2:0]	Clock select (F_{p0ck})
3'b000	F_{CPU}
3'b001	F_{IRC} (16Mhz)
3'b010	F_{OSC}
3'b011	T0CK(External clock)
3'b100	T1CK(External clock)

Bit[1:0] : Revered

Address 15H: PWM0 Control Register (PWM0CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM0EN	P0OUTS	P0TPS[2:0]			P0TMEN	P0TMIE	P0TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM0EN

PWM0 module enable.

1 = Enable.

0 = Disable.

Bit[6] : P0OUTS

PWM0 Duty Cycle pulse output select.

1 = PWM0 Duty Cycle pulse output is low.

0 = PWM0 Duty Cycle pulse output is high.

Bit[5:3] : P0TPS[2:0]

PWM0 Timer prescaler, as follow **Table 8-4:**

P0CKSL [2:0]	PWM0 MODE (T_{p0ck})
3'b000	PWM0 Timer clock select is F_{p0ck}
3'b001	PWM0 Timer clock select is F_{p0ck} /2
3'b010	PWM0 Timer clock select is F_{p0ck} /4
3'b011	PWM0 Timer clock select is F_{p0ck} /8
3'b100	PWM0 Timer clock select is F_{p0ck} /16
3'b101	PWM0 Timer clock select is F_{p0ck} /32
3'b110	PWM0 Timer clock select is F_{p0ck} /64
3'b111	PWM0 Timer clock select is F_{p0ck} /128

Table 8-4 PWM0 Timer clock select

Bit[2] : P0TMEN

PWM0 Timer enable bit.

1 = Enable.

0 = Disable.

Bit[1] : P0TMIE

PWM0 Timer overflow interrupt bit.

1 = Enable interrupt.

0 = Disable interrupt.

Bit[0] : P0TMIF

PWM0 Timer overflow flag bit.

1 = PWM0 Timer overflow has occurred, write 0 clear flag.

0 = PWM0 Timer overflow has not occurred yet.

Address 16H: PWM0 Timer Low byte value Register (P0TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P0TM[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TM[7:0]

PWM0 Timer Low byte

Address 17H: PWM0 Timer compared or overflow reload Low byte value Register (P0RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P0TMRLD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TMRLD[7:0]

PWM0 Timer compared or overflow reload Low byte

Address 18H: PWM0 Timer and Reload High-nibble bits Register(P0TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P0TM [11:8]				P0TMRLD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P0TM[11:8]

PWM0 Timer high-nibble bits

Bit[3:0] : P0TMRLD[11:8]

PWM0 Timer compared or overflow reload high-nibble bits.

6.2 PWM1 Registers

Address 19H: PWM1 configuration Register(PWM1CON)

Bits	7	6	5	4	3	2	1	0
Name	P1INTSL	P1DT[2:0]			P1CKS[1:0]			Revered
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P1INTSL

PWM1 interrupt selection.

1 = Select interrupt for PWM1 overflow.

0 = Select interrupt for PWM1 timer time out.

Bit[6:4] :P0DT[2:0]

PWM1 Duty Range.

P1DT[[2:0],	PWM1 Duty Range		PWM1 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-3 PWM1 Duty Range

Bit[3:1] : P1CKS[2:0]

PWM1 Timer clock select.

P1CKS[2:0]	Clock select (F_{p1ck})
3'b000	F_{CPU}
3'b001	F_{IRC} (16Mhz)
3'b010	F_{OSC}
3'b011	T0CK(External clock)
3'b100	T1CK(External clock)

Bit[0] : Revered

Address 1AH: PWM1 Control Register (PWM1CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM1EN	P1OUTS	P1TPS[2:0]			P1TMEN	P1TMIE	P1TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM1EN

PWM1 module enable.

1 = Enable.

0 = Disable.

Bit[6] : P1OUTS

PWM1 Duty Cycle pulse output select.

1 = PWM1 Duty Cycle pulse output is low.

0 = PWM1 Duty Cycle pulse output is high.

Bit[5:3] : P1TPS[2:0]

PWM1 Timer prescaler , as follow **Table 6-5:**

P1CKSL [2:0]	PWM1 MODE
3'b000	PWM1 Timer clock select is F_{p1ck}
3'b001	PWM1 Timer clock select is F_{p1ck} /2
3'b010	PWM1 Timer clock select is F_{p1ck} /4
3'b011	PWM1 Timer clock select is F_{p1ck} /8
3'b100	PWM1 Timer clock select is F_{p1ck} /16
3'b101	PWM1 Timer clock select is F_{p1ck} /32
3'b110	PWM1 Timer clock select is F_{p1ck} /64
3'b111	PWM1 Timer clock select is F_{p1ck} /128

Table 6-4 PWM1 Timer clock select

Bit[2] : P1TMEN

PWM1 Timer enable bit.

1 = Enable.

0 = Disable.

Bit[1] : P1TMIE

PWM1 Timer overflow interrupt bit.

1 = Enable interrupt.

0 = Disable interrupt.

Bit[0] : P1TMIF

PWM1 Timer overflow flag bit.

1 = PWM1 Timer overflow has occurred, write 0 clear flag.

0 = PWM1 Timer overflow has not occurred yet.

Address 1BH: PWM1 Timer Low byte value Register (P1TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P1TM[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TM[7:0]

PWM1 Timer Low byte

Address 1CH: PWM1 Timer compared or overflow reload Low byte value Register (P1RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P1TMRLD[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P10TMRLD[7:0]

PWM1 Timer compared or overflow reload Low byte

Address 1DH: PWM1 Timer and High-nibble bits Register(P1TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P1TM [11:8]				P1TMRLD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P1TM[11:8]

PWM1 Timer high-nibble bits

Bit[3:0] : P1TMRLD[11:8]

PWM1 Timer compared or overflow reload high-nibble bits.

6.3 PWM2 Registers

Address 1EH: PWM2 configuration Register(PWM2CON)

Bits	7	6	5	4	3	2	1	0
Name	P2INTSL	P2DT[2:0]			P2CKS[1:0]			Revered
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P2INTSL

PWM2 interrupt selection.

1 = Select interrupt for PWM2 overflow.

0 = Select interrupt for PWM2 timer time out.

Bit[6:4] :P2DT[2:0]

PWM2 Duty Range.

P2DT[[2:0],	PWM2 Duty Range		PWM2 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-5 PWM2 Duty Range

Bit[3:1] : P2CKS[2:0]

PWM2 Timer clock select.

P2CKS[2:0]	Clock select (F_{p2ck})
3'b000	F_{CPU}
3'b001	F_{IRC} (16Mhz)
3'b010	F_{OSC}
3'b011	T0CK(External clock)
3'b100	T1CK(External clock)

Bit[0] : Revered

Address 1FH: PWM2 Control Register (PWM2CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM2EN	P2OUTS	P2CKSL[2:0]			P2TMEN	P2TMIE	P2TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM2EN

PWM1 module enable.

1 = Enable.

0 = Disable.

Bit[6] : P2OUTS

PWM1 Duty Cycle pulse output select.

1 = PWM2 Duty Cycle pulse output is low.

0 = PWM2 Duty Cycle pulse output is high.

Bit[5:3] : P2CLKS[2:0]

PWM2 Timer prescaler, as follow **Table 6-5:**

P2CKSL [2:0]	PWM1 MODE
3'b000	PWM2 Timer clock select is F_{p2ck}
3'b001	PWM2 Timer clock select is F_{p2ck} /2
3'b010	PWM2 Timer clock select is F_{p2ck} /4
3'b011	PWM2 Timer clock select is F_{p2ck} /8
3'b100	PWM2 Timer clock select is F_{p2ck} /16
3'b101	PWM2 Timer clock select is F_{p2ck} /32
3'b110	PWM2 Timer clock select is F_{p2ck} /64
3'b111	PWM2 Timer clock select is F_{p2ck} /128

Table 6-6 PWM2 Timer clock select

Bit[2] : P2TMEN

PWM2 Timer enable bit.

1 = Enable.

0 = Disable.

Bit[1] : P2TMIE

PWM1 Timer overflow interrupt bit.

1 = Enable interrupt.

0 = Disable interrupt.

Bit[0] : P2TMIF

PWM1 Timer overflow flag bit.

1 = PWM1 Timer overflow has occurred, write 0 clear flag.

0 = PWM1 Timer overflow has not occurred yet.

Address 20H: PWM2 Timer Low byte value Register (P2TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P2TM[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P2TM[7:0]

PWM2 Timer Low byte

Address 21H: PWM2 Timer compared or overflow reload Low byte value Register (P2RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P2TMRLD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P2TMRLD[7:0]

PWM2 Timer compared or overflow reload Low byte

Address 22H: PWM2 Timer and reload High-nibble bits Register(P2TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P2TM [11:8]				P2TMRLD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P2TM[11:8]

PWM2 Timer high-nibble bits

Bit[3:0] : P2TMRLD[11:8]

PWM2 Timer compared or overflow reload high-nibble bits.

6.3 PWM3 Registers

Address 23H: PWM3 configuration Register(PWM3CON)

Bits	7	6	5	4	3	2	1	0
Name	P3INTSL	P3DT[2:0]			P3CKS[1:0]			Revered
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P3INTSL

PWM3 interrupt selection.

1 = Select interrupt for PWM3 overflow.

0 = Select interrupt for PWM3 timer time out.

Bit[6:4] :P3DT[2:0]

PWM3 Duty Range.

P1DT[[2:0],	PWM3 Duty Range		PWM3 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-7 PWM3 Duty Range

Bit[3:1] : P3CKS[2:0]

PWM3 Timer clock select.

P3CKS[2:0]	Clock select (F_{p3ck})
3'b000	F_{CPU}
3'b001	F_{IRC} (16Mhz)
3'b010	F_{OSC}
3'b011	T0CK(External clock)
3'b100	T1CK(External clock)

Bit[0] : Revered

Address 24H: PWM3 Control Register (PWM3CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM3EN	P3OUTS	P3CKSL[2:0]			P3TMEN	P3TMIE	P3TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR

Bit[7] : PWM3EN

PWM3 module enable.

1 = Enable.

0 = Disable.

Bit[6] : P1OUTS

PWM3 Duty Cycle pulse output select.

1 = PWM3 Duty Cycle pulse output is low.

0 = PWM3 Duty Cycle pulse output is high.

Bit[5:3] : P3CLKS[2:0]

PWM3 Timer prescaler, as follow **Table 6-5:**

P1CKSL [2:0]	PWM1 MODE
3'b000	PWM3 Timer clock select is F_{p3ck}
3'b001	PWM3 Timer clock select is F_{p3ck} /2
3'b010	PWM3 Timer clock select is F_{p3ck} /4
3'b011	PWM3 Timer clock select is F_{p3ck} /8
3'b100	PWM3 Timer clock select is F_{p3ck} /16
3'b101	PWM3 Timer clock select is F_{p3ck} /32
3'b110	PWM3 Timer clock select is F_{p3ck} /64
3'b111	PWM3 Timer clock select is F_{p3ck} /128

Table 6-4 PWM0 Timer clock select

Bit[2] : P3TMEN

PWM3 Timer enable bit.

1 = Enable.

0 = Disable.

Bit[1] : P3TMIE

PWM3 Timer overflow interrupt bit.

1 = Enable interrupt.

0 = Disable interrupt.

Bit[0] : P3TMIF

PWM3 Timer overflow flag bit.

1 = PWM3 Timer overflow has occurred, write 0 clear flag.

0 = PWM3 Timer overflow has not occurred yet.

Address 25H: PWM3Timer Low byte value Register (P3TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P1TM[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TM[7:0]

PWM1 Timer Low byte

Address 26H: PWM3 Timer compared or overflow reload Low byte value Register (P3RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P1TMRLD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P3TMRLD[7:0]

PWM3 Timer compared or overflow reload Low byte

Address 27H: PWM3 Timer and reload High-nibble bits Register(P3TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P3TM [11:8]				P3TMRLD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P3TM[11:8]

PWM3 Timer high-nibble bits

Bit[3:0] : P3TMRLD[11:8]

PWM3 Timer compared or overflow reload high-nibble bits.

6.4 PWM code Example

```
// pwm clock source F0ck = Fcpu(4MHz)
        BCR     PWM0CON,P0CKS2_B
        BCR     PWM0CON,P0CKS1_B
        BCR     PWM0CON,P0CKS0_B
 // pwm clock source F0ck/32 Hz
        BSR     PWM0CR,P0TPS2_B             ; F0ck = 4/32 Mhz = 125 Khz ;
        BCR     PWM0CR,P0TPS1_B
        BSR     PWM0CR,P0TPS0_B
```

(A) **4~8-bits PWM**

```
 // pwm duty range  6bits( Rang  0~63)
        BCR     PWM0CON,P0DT2_B
        BSR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B

        MOVIA   00fh                ;  Load initial value 7~0 bits
        MOVAR   P0RDLB              ; Duty Cycle = 15 (1/F0ck) clock s

 // enable pwm
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B            ; First Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B
```

(B) **9~12-bits PWM**

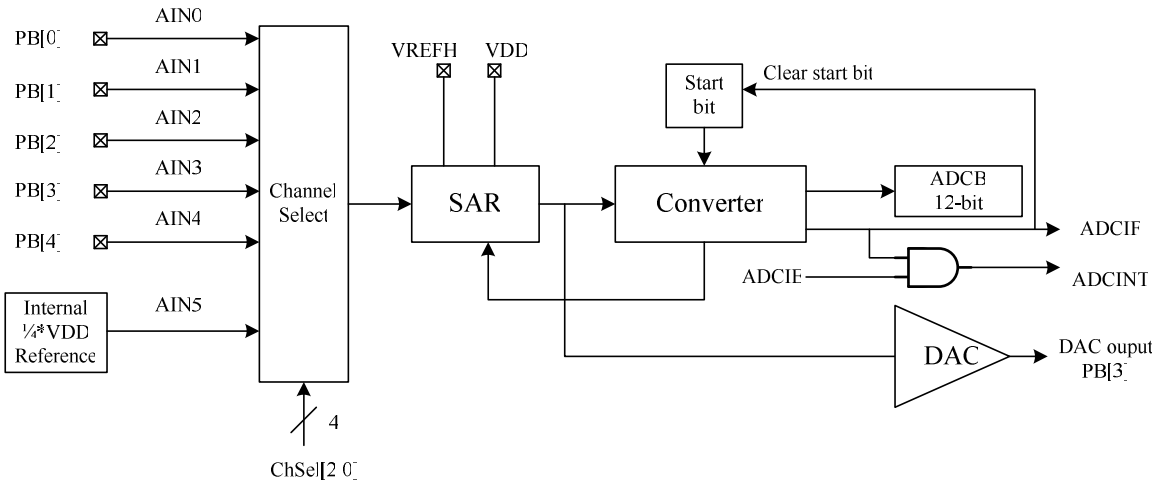
```
 // pwm duty range  12bits( Rang  0~4095)
        BSR     PWM0CON,P0DT2_B
        BSR     PWM0CON,P0DT1_B
        BSR     PWM0CON,P0DT0_B

        MOVIA   00fh                ;  Load initial value Low byte 7~0 bits
        MOVAR   P0RDLB              ;
        MOVIA   00h                 ;  Load initial value High byte 12~9 bits
        MOVAR   P0RDHB              ;  Duty Cycle = 15 (1/F0ck) clock s

 // enable pwm
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B            ; First Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B
```

【7】 5+1 Channel Analog to Digital (ADC)

Build In ADC module supports 5 channel(PB[0]~PB[4]) and one internal channel ¼ VDD reference that can be use for auxiliary input and battery monitor. The ADC module converts an input voltage to a 12-bit digital code.



9.1 ADC Registers

Address 28H: ADC Control –1 Register(ADCON-1)

Bits	7	6	5	4	3	2	1	0
Name	ADCEN	ADCST	CHSEL[2:0]			Revered	ADCSR[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : ADCEN

ADC module enable bit.

1 = Enable ADC.

0 = Disable ADC.

Bit[6] : ADCST

1 = Start to ADC sample, when ADC conversion has been completed, this start be clear to 0 by H/W.

0 = Stop.

Bit[5:2] : CHSEL[2:0]

ADC input channel select bit, as follows **Table9-1**

CHSEL[2:0]	Input Channel
3'b000	PB[0] (AIN0)
3'b001	PB[1] (AIN1)
3'b010	PB[2] (AIN2)
3'b011	PB[3] (AIN3)
3'b100	PB[4] (AIN4)
3'b101	Internal VDD/4 (AIN5)

Table 9-1 ADC input channel select

Bit[1:0] : ADCSR[1:0]

ADC clock selection.

2'b00 : ADC clock is Fcpu/8.

2'b01 : ADC clock is Fcpu/4.

2'b10 : ADC clock is Fcpu/2.

2'b11 : ADC clock is Fcpu.

Address 29H: ADC Control-2 Register(ADCON-2)

Bits	7	6	5	4	3	2	1	0
Name	ADCIE	ADCIF	SVREFH	ADCNT	DACOEN	ADCTMS	SELVER[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : ADCIE

ADC interrupt Enable bit .

1 = Enable.

0 = Disable.

Bit[6] : ADCIF

ADC conversion has been completed interrupt flag.

1 = ADC conversion has been completed, write 0 clear flag.

0 = ADC conversion has been not completed yet.

Bit[5] : SVREFH

Select VREFH from external or internal voltage.

1 = External voltage(VREFH == PB[4] pin).

0 = Internal voltage(VREFH == Internal reference voltage Table9-2).

Bit[4] : ADCNT

ADC sample mode.

1 = ADC continues mode.

0 = Trigger mode base on ADCST bit.

Bit[3] : DACOEN

DAC output enable.(and Reg-29h ADCTEST =1)

1 = Enable output.(DAC output to AIN3,PB[3])

0 = Disable output .

Bit[3] : ADCTMS

ADC convert Timing.

1 = Fixed convert timing.

0 = Non-Fixed convert timing.

Bit[1:0] : SELVER[1:0]

ADC internal VERFH voltage selection.

SELVER[1:0]	VREFH
2'b00	VDD
2'b01	4V
2'b10	3V
2'b11	2V

Table 9-2 ADC internal VERFH voltage selection

Address 3CH: ADC High byte Register(ADCHB)

Bits	7	6	5	4	3	2	1	0
Name	ADCB[11:4]/DACB[7:0]							
Read/Write	R/W	R /W	R /W	R /W	R /W	R /W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : ADCB[11:4] read only

ADC High data byte of ADCB[11:0] buffer

Bit[7:0] : DACB[7:0] Write only

DAC High data byte of DACB[11:0] buffer

Address 3DH: ADC Low byte Register(ADCLB)

Bits	7~4	3~0
Name	Revered	ADCB[3:0]/DACB[3:0]
Read/Write	--	R/W
Default	0	0

Bit[3:0] : ADCB[3:0] read only

ADC Low data byte of ADCB[11:0] buffer.

Bit[3:0] : DACB[11:8] Write only

DAC Low data byte of DACB[11:0] buffer

Address 28H: ADC Control-3 Register(ADCON-3)

Bits	7	6	5	4	3	2	1	0
Name	ADCTEST	ADCFLAG	ADCLKIN	ADCMPO	--	ADC_NUB[2:0]		
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Address 29H: ADC Control-4 Register(ADCON-4)

Bits	7	6	5	4	3	2	1	0
Name	ADC_TCK[5:0]						ADC_CDAB[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

Accessed by IOST/IOSTR instruction

Bit[7:3] : ADC_TCK [5:0]

ADCTCK[2:0]
Adjust FSM_CLK raising edge to falling edge timing(T1)
ADCTCK[5:3]
Adjust FSM_CLK falling edge to Flag raising edge timing(T2)
ADCTCK[1:0]
Adjust Flag raising edge to FSM_CLK raising edge timing(T3).

ADCTCK[1:0]	cycles of ADC clock(T1)
2'b00	1 cycles
2'b01	2 cycles
2'b10	3 cycles
2'b11	4 cycles

ADCTCK[3:2]	cycles of ADC clock(T2)
2'b00	1 cycles
2'b01	2 cycles
2'b10	3 cycles
2'b11	4 cycles

ADCTCK[5:4]	cycles of ADC clock(T3)
2'b00	1 cycles
2'b01	2 cycles
2'b10	3 cycles
2'b11	4 cycles

Bit[2:0] : ADC_NUB [2:0]

ADC output bit number (N bit).

ADC[2:0]	ADC resolution
3'b000	12bits
3'b001	11 bits
3'b010	10 bits
3'b011	9 bits
3'b100	8 bits
3'b101	7 bits

ADC Converting time

$$\text{ADC Conversion time} = (1/\text{ADC clock}) * [(T1 + T2 + T3) * ((\text{N bit} + 1) + 1)] \quad \text{sec}$$

【8】 Interrupt

The FM8PC71A has interrupt as following:

1. PWM0 Timer interrupt.
2. PWM1 Timer interrupt.
3. PWM2 Timer interrupt.
4. PWM3 Timer interrupt.
5. GPIO(PORTB0~6) and GPIO(PORTA0~6) external interrupt.
6. ADC sample completed interrupt.

The FM8PC71A reset vector is fixed at 0x0000h and
the interrupt vector is at 0x0003h.
A global interrupt enable bit, GIE(Reg.0Bh-7), enable(if set) all un-masked interrupts or disables(if cleared) all interrupts. Individual interrupts can be enable/disable through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.
The interrupt priority is decided by customer firmware control.

13.1 Interrupt Registers

Address 0BH : Interrupt Mask Register(INTEN)

Bits	7	6	5	4	3	2	1	0
Name	GIE	Revered	Revered	Revered	Revered	Revered	T1IE	T0IE
Read/Write	R/W	--	--	--	--	--	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : GIE
Global Interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[1] : T1IE
Timer1 Interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[0] :T0IE
Timer0 Interrupt enable bit.
1 = Enable.
0 = Disable

Address 0CH : Interrupt Flag Register(INTFLAG)

Bits	7	6	5	4	3	2	1	0
Name	PBIF	PAIF	--	--	--	--	T1IF	T0IF
Read/Write	R/W	R/W	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] :PBIF

Port B interrupt flag, write 0 clear flag.

1 = Interrupt occurrence of PortB.

Bit[6] :PAIF

Port A interrupt flag, write 0 clear flag.

1 = Interrupt occurrence of PorA.

Bit[5:2] :Revered

Bit[1] :T1IF

Timer1 Interrupt flag, write 0 clear flag.

1 = Interrupt occurrence of Timer1 .

Bit[0] :T0IF

Timer0 Interrupt flag, write 0 clear flag.

1 = Interrupt occurrence of Timer0 .

【9】 Instruction Set

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	**R, bit**	Clear bit in R	0 → R<b>	1	-
BSR	**R, bit**	Set bit in R	1 → R<b>	1	-
BTRSC	**R, bit**	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2 (1)	-
BTRSS	**R, bit**	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2 (1)	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
CLRA		Clear ACC	00h → ACC	1	Z
IOST	**R**	Load R-plane register	ACC → R-plane register	1	-
IOSTR	**R**	Read R-plane register	R-plane register → ACC		
CLRR	**R**	Clear R	00h → R	1	Z
MOVAR	**R**	Move ACC to R	ACC → R	1	-
MOVR	**R, d**	Move R	R → dest	1	Z
DECR	**R, d**	Decrement R	R - 1 → dest	1	Z
DECRSZ	**R, d**	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2 (1)	-
INCR	**R, d**	Increment R	R + 1 → dest	1	Z
INCRSZ	**R, d**	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2 (1)	-
ADDAR	**R, d**	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	**R, d**	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ANDAR	**R, d**	AND ACC with R	ACC and R → dest	1	Z
IORAR	**R, d**	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	**R, d**	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	**R, d**	Complement R	$\overline{R}$ → dest	1	Z
RLR	**R, d**	Rotate left f through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	**R, d**	Rotate right f through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	**R, d**	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	**I**	Move Immediate to ACC	I → ACC	1	-

Mnemonic, Operands	Description	Operation	Cycles	Status Affected
ADDIA I	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA I	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA I	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA I	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA I	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA I	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL I	Call subroutine	PC + 1 → Top of Stack, I → PC	2	-
GOTO I	Unconditional branch	I → PC	2	-

Note: 1. 2 cycles for skip, else 1 cycle

2. bit : Bit address within an 8-bit register R
   R : Register address (00h to 7Fh)
   I : Immediate data
   ACC : Accumulator
   d : Destination select;
   =0 (store result in ACC)
   =1 (store result in file register R)
   dest : Destination
   PC : Program Counter
   PCHBUF : High Byte Buffer of Program Counter
   WDT : Watchdog Timer Counter
   GIE : Global interrupt enable bit
   $\overline{TO}$: Time-out bit
   $\overline{PD}$: Power-down bit
   C : Carry bit
   DC : Digital carry bit
   Z : Zero bit

10. Absolute Maximum Ratings

Parameter	Conditions	Values		Unit
		min.	max.	
Ambient Operating Temperature	-	-40	85	℃
Storage Temperature	-	-40	150	℃
DC Supply Voltage	-	2.4	5.5	V
Supply Current	-	-	-	mA

11. DC Characteristics (Operating Temperature = 0 to70 ℃)

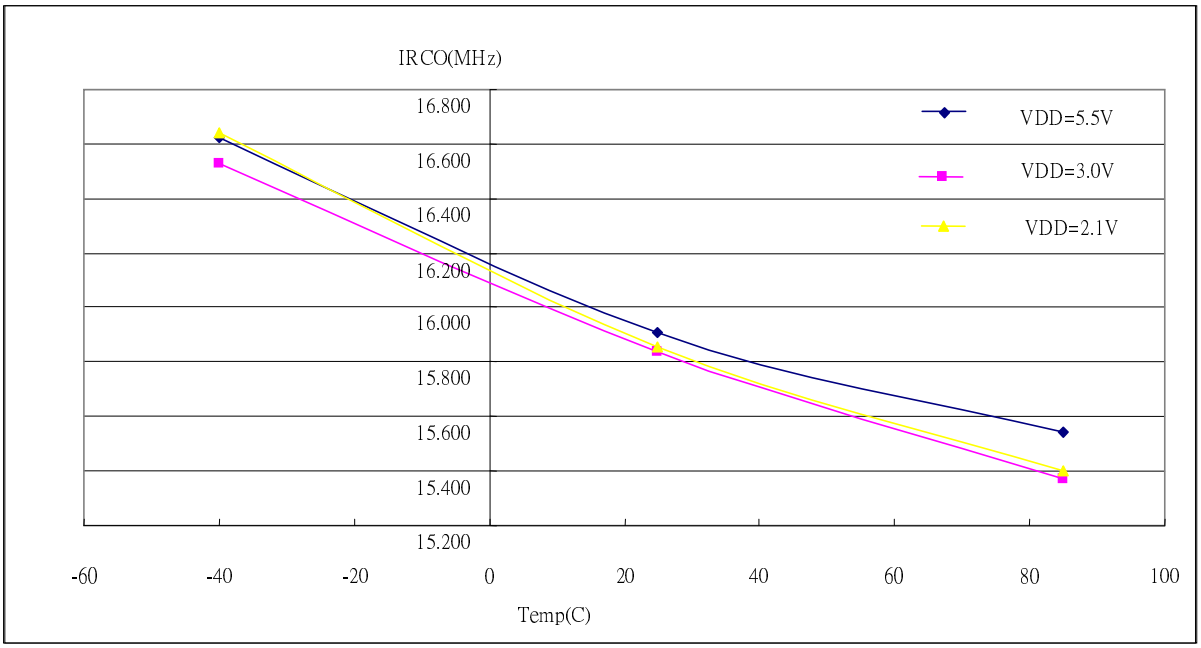
11.1 General

Symbol	Parameter	Conditions	Values			Unit
			MIN.	TYP.	MAX	
VDD	Operating Voltage	--	2.2	5.0	5.5	V
I_{dd1}	**Normal Mode** Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=16MHz		4.8		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vddc=3V,No GPIO loading IRC Operating, FCPU=16MHz		2.5		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=1MHz		1.11		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vddc=3V,No GPIO loading IRC Operating, FCPU=1MHz		0.86		mA
I_{dd2}	**Slow Mode** Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading SIRC Operating, FCPU=32KHz		0.3		mA
	Slow Mode Operating Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading SIRC Operating, FCPU=16KHz		0.09		mA
I_{dd3}	**Green Mode** Operating Current (watch Dog Enable) Typical = (Disable ADC)	Vdd=5V,No GPIO loading WDT = 18ms SIRC Operating ,FCPU=Disable		17		uA
	Green Mode Operating Current (watch Dog Enable) Typical = (Disable ADC)	Vdd=3V,No GPIO loading WDT = 18ms SIRC Operating ,FCPU=disable		12		uA
I_{dd4}	**Suspend Mode** Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading 25 ℃		0.15		uA
	Suspend Mode Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading 25 ℃		0.01		uA
	Suspend Mode Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading -40 ℃~70 ℃				
	Suspend Mode Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading -40 ℃~70 ℃				

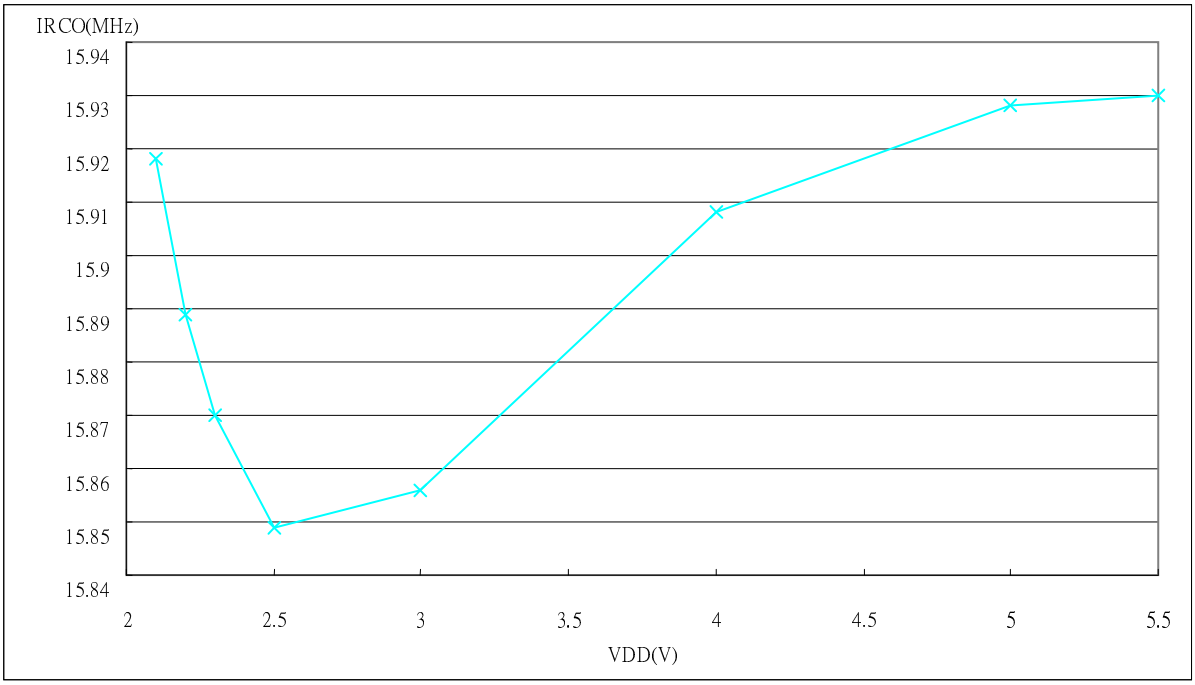
Symbol	Parameter	Conditions	Values			Unit
			MIN.	TYP.	MAX	
V_{LVDT}	Low Voltage Detect	VDT36			3.6	V
		VDT24			2.4	V
		VDT20 (VDD from 0V to 5V)			2.0	V
		VDT20 (VDD from 5V to 0V)			2.0	V
V_{POR}	Power on Reset	VDD from 0V to 5V			1.8V	V
		VDD from 5V to 0V			1.8	V
F_{CPU}	MCU clock frequency	25 ℃, VDD >= 3.6V			16	Mhz
		25 ℃, 2V < VDD < 3.6V			16	Mhz
F_{IRC}	Internal high RC frequency	VDD=5V, 25 ℃, F_{CPU} =16Mhz			16	MHz
		VDD=2.2~5V, F_{CPU} =1~16Mhz			16	MHz
F_{SIRC}	Internal Slow RC frequency	VDD=5V, 25 ℃			32	KHz
T_{POREXT}	Power on reset Timing	SELPOR = 2'b11 (16ms) VDD =5V	13		14	mS
		SELPOR = 2'b11 (16ms) VDD =3V	23		27	mS
$C_{cyrstal}$	External crystal capacitance	Fcrystal = 16Mhz (XIN pin connect, XOUT no connect)		33		pF
		Fcrystal = 32Khz (XIN,XOUT pin connect)		33		

11.2 Internal High RC 16MHZ characteristic

(A) Temperature characteristic



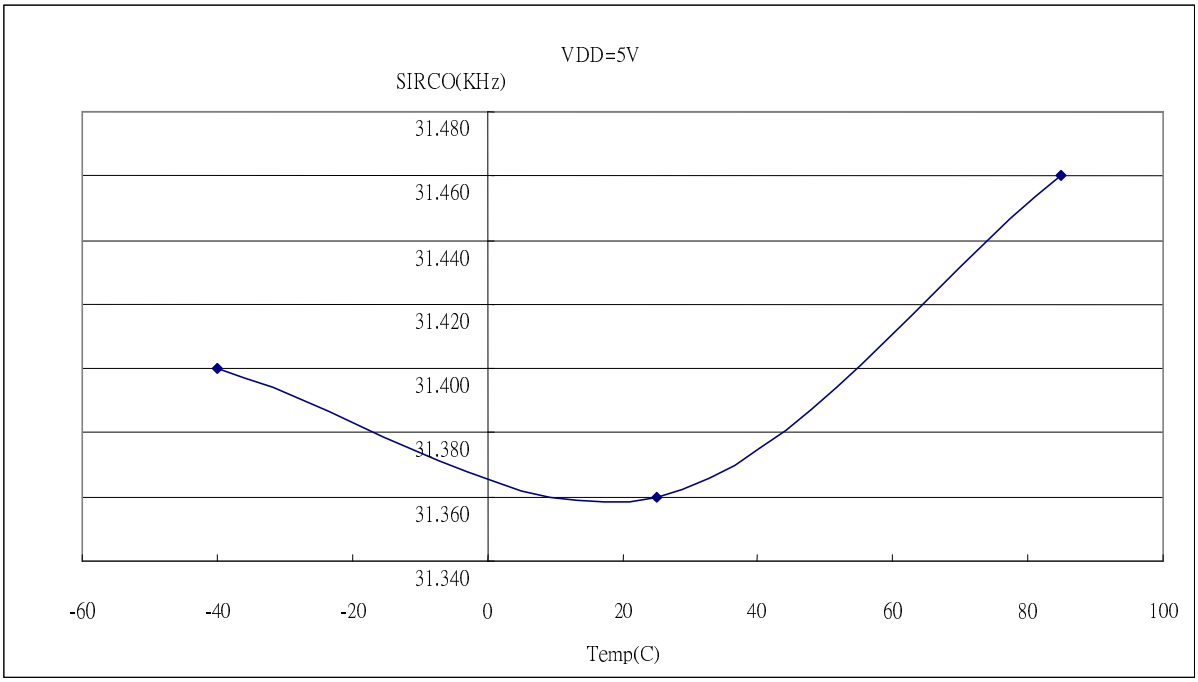
(B) Power Voltage characteristic



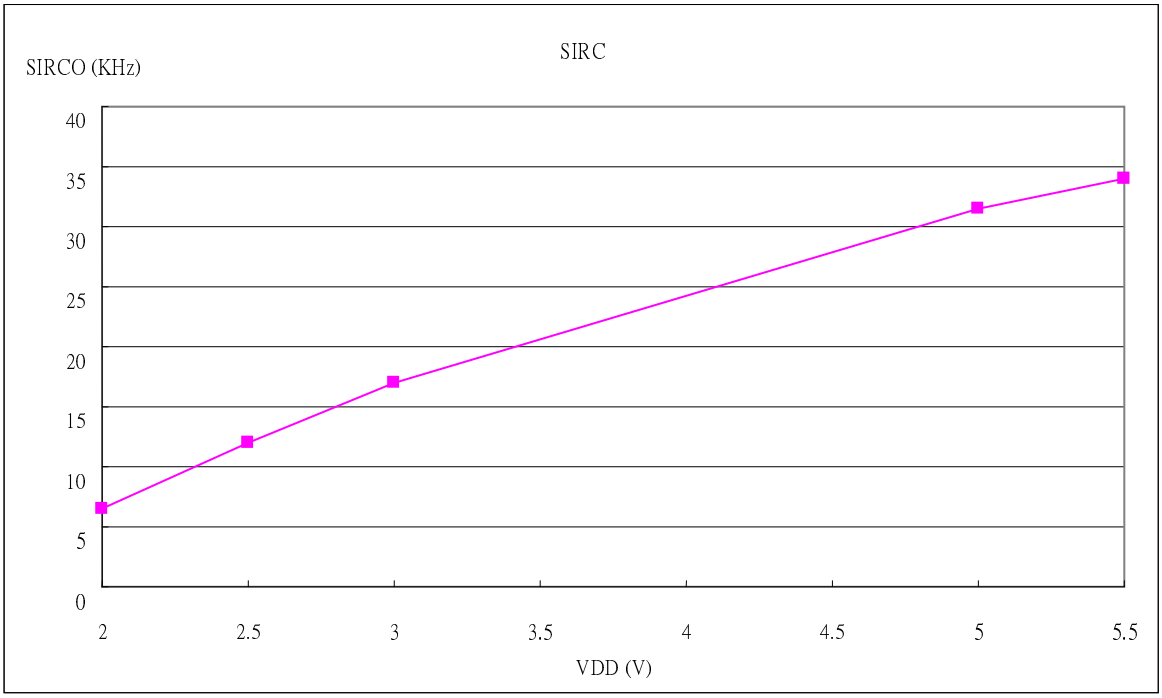
Note: Temperature = 25 ℃

11.4 Internal slow RC 32KHz characteristic

(A) Temperature characteristic



(B) Power Voltage characteristic



Note: Temperature = 25 ℃

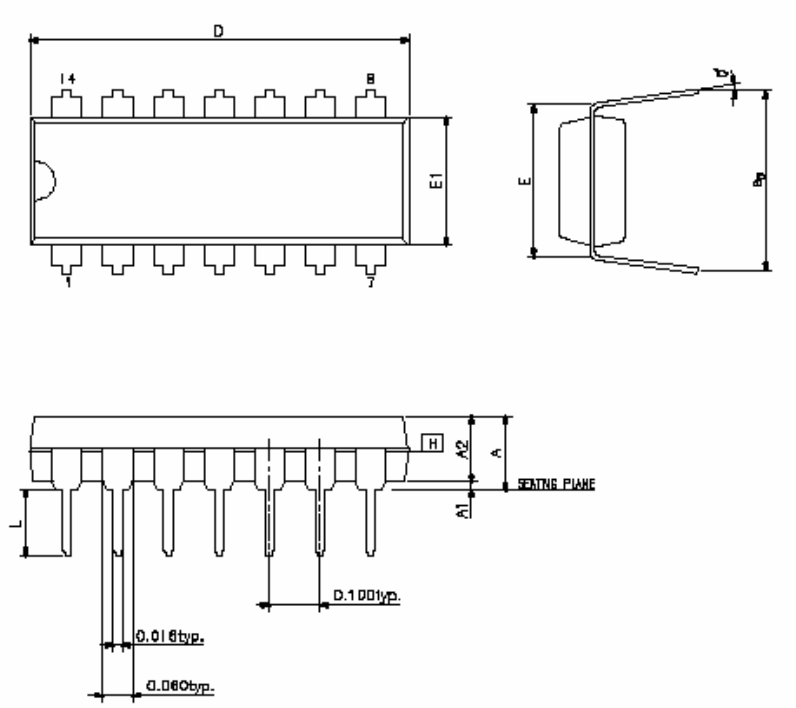
11.5 GPIO Interface

Symbol	Parameter	Conditions	Values		Unit
			min.	max.	
V_{up1}	GPIO Pull-up Resistor	VDD=5V	90	100	KΩ
V_{up2}	GPIO Pull-up Resistor	VDD=3V	90	100	KΩ
V_{OL}	Output Low Voltage(High drive)	VDD=5V~2V, I_{OL}=20,8,2mA	-	0.4	V
V_{OH}	Output High Voltage1	VDD=5~3V, I_{OH}=20mA VDD=2V, I_{OH}=11mA	VDD-0.4V	-	V
V_{IL}	Input Low Voltage	VDD=5V(All GPIO input)	1.5		V
		VDD=4V(All GPIO input)	1.2		V
		VDD=3V(All GPIO input)	0.8		V
		VDD=2V(All GPIO input)	0.6		V
V_{IH}	Input High Voltage	VDD=5V(All GPIO input)	3.6		V
		VDD=4V(All GPIO input)	2.9		V
		VDD=3V(All GPIO input)	2.1		V
		VDD=2V(All GPIO input)	1.4		V
V_{IL2}	Input Low Voltage	Reset Pin			V

11.6 ADC specification

Symbol	Parameter	Conditions	Values			Unit
			min.	Typ.	max.	
ADCSR	ADC sample Rate	-			32	KHz
DNL	Differential Nonlinearity	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V F_{ADCSR}=64K			±0.65	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V F_{ADCSR}=64K			±0.23	LSB
INL	Integral Nonlinearity	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V F_{ADCSR}=64K			±2.5	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V F_{ADCSR}=64K			±1.0	LSB
GR	Gain Error	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V F_{ADCSR}=64K			--	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V F_{ADCSR}=64K			--	LSB
ADCRL	ADC Resolution Typical = bit	VDD=5.0V, VREFH = 3.3V F_{ADCSR}=64K	8	10	12	bit
			-		-	
					-	

■ 14- LEAD (300mil) DIP



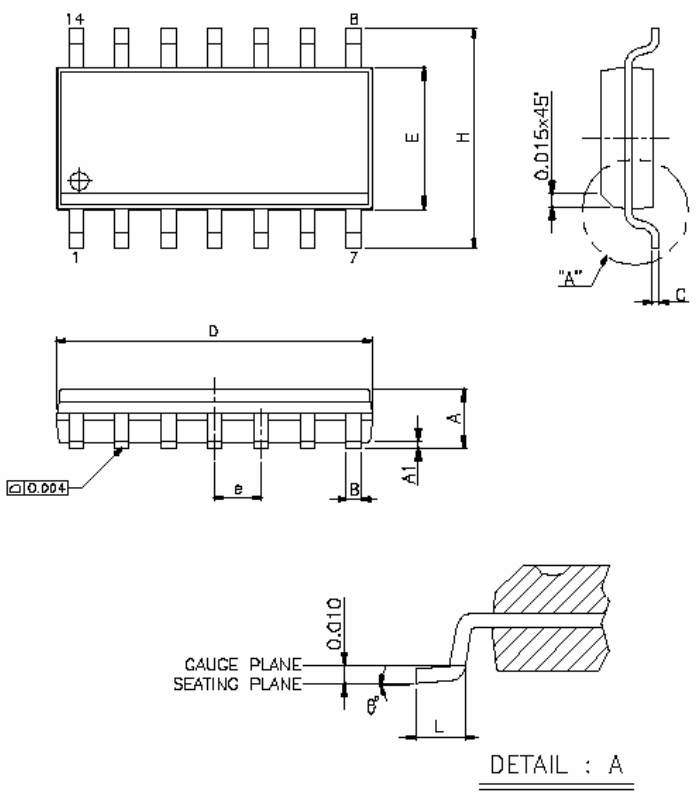
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 AA
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

■ 14- LEAD (150mil) SOP

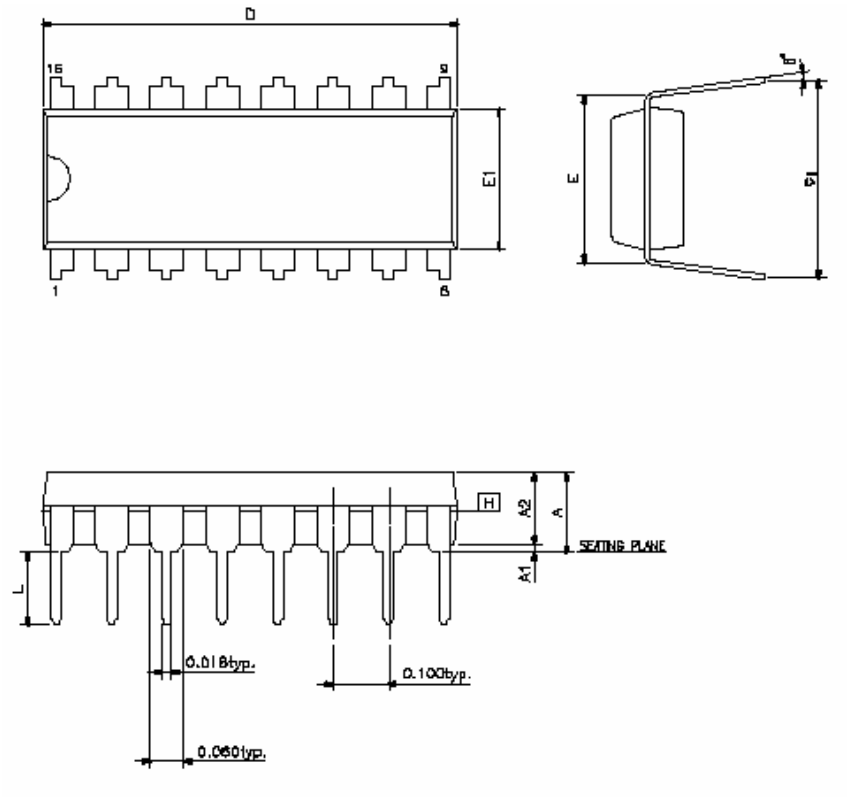


SYMBOLS	MIN.	NOM.	MAX.
A	0.058	0.064	0.068
A1	0.004	–	0.010
B	0.013	0.016	0.020
C	0.0075	0.008	0.0098
D	0.336	0.341	0.344
E	0.150	0.154	0.157
e	–	0.050	–
H	0.228	0.236	0.244
L	0.015	0.025	0.050
θ°	0°	–	8°

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-012 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

■ 16- LEAD (300mil) DIP



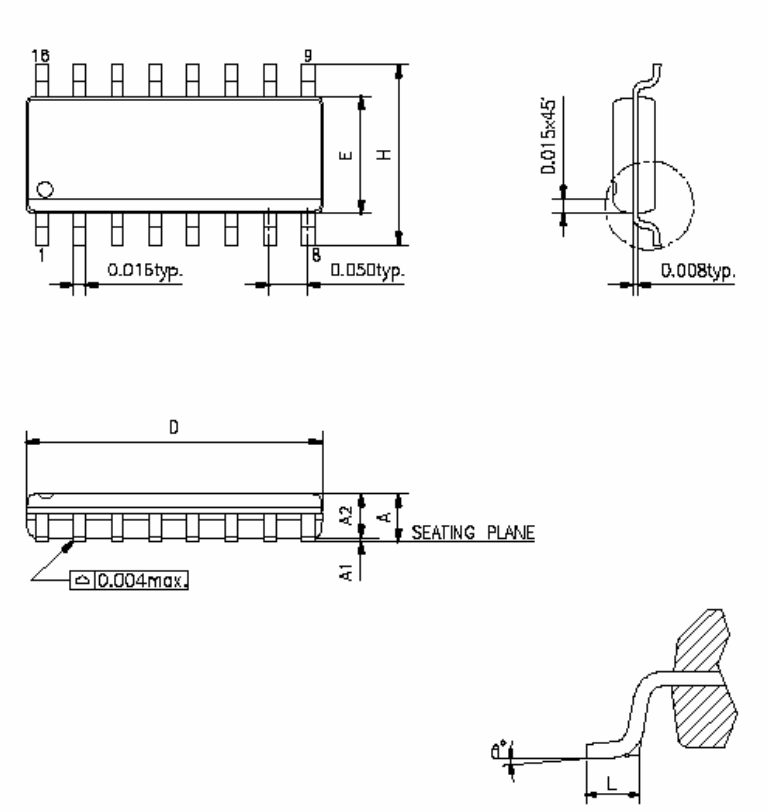
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 BB
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

■ 16- LEAD (150mil) SOP



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	0.049	0.065
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AC.
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训推荐课程列表： http://www.edatop.com/peixun/tuijian/

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

课程网址：http://www.edatop.com/peixun/rfe/110.html

手机天线设计培训视频课程

该套课程全面讲授了当前手机天线相关设计技术，内容涵盖了早期的外置螺旋手机天线设计，最常用的几种手机内置天线类型——如 monopole 天线、PIFA 天线、Loop 天线和 FICA 天线的设计，以及当前高端智能手机中较常用的金属边框和全金属外壳手机天线的设计；通过该套课程的学习，可以帮助您快速、全面、系统地学习、了解和掌握各种类型的手机天线设计，以及天线及其匹配电路的设计和调试...

课程网址： http://www.edatop.com/peixun/antenna/133.html

WiFi 和蓝牙天线设计培训课程

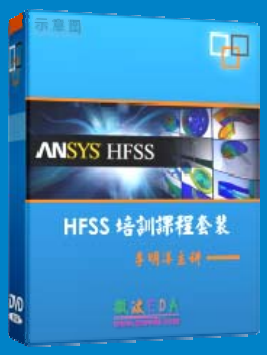
该套课程是李明洋老师应邀给惠普 (HP)公司工程师讲授的 3 天员工内训课程录像，课程内容是李明洋老师十多年工作经验积累和总结，主要讲解了 WiFi 天线设计、HFSS 天线设计软件的使用，匹配电路设计调试、矢量网络分析仪的使用操作、WiFi 射频电路和 PCB Layout 知识，以及 EMC 问题的分析解决思路等内容。对于正在从事射频设计和天线设计领域工作的您，绝对值得拥有和学习！…

课程网址：http://www.edatop.com/peixun/antenna/134.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

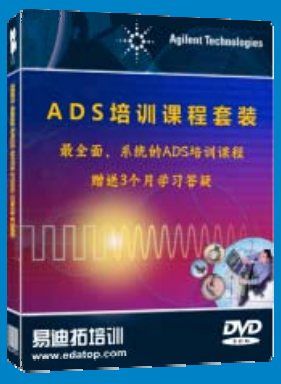


HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

ADS 学习培训课程套装



该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com