Appendix RF Manual 7th edition

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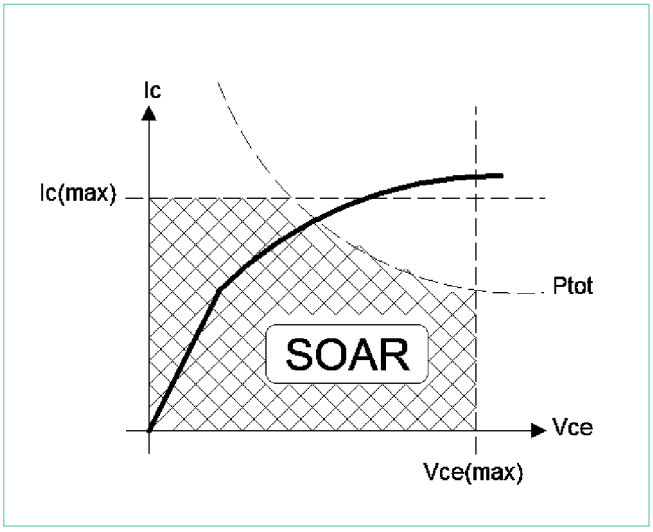
Contents

1. Thermal design considerations for SMD discretes

1.1 Introduction

A semiconductor device has several electrically and thermally limiting parameters given by the data sheet. To the right is shown the Safe Operating ARea (SOAR). The SOAR limits the static bias setting and the dynamic operating point.



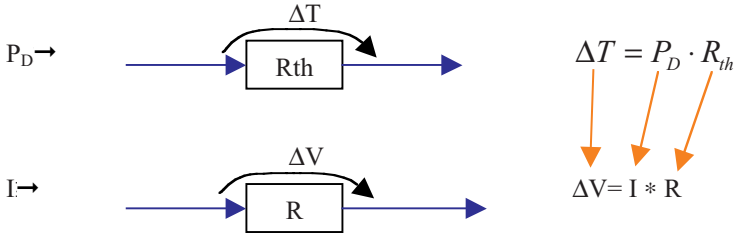
A current overload crossing the $I_{C(max)}$ boarder may burn out the power conducting channel or melt the bond wires. Crossing the $V_{CE(max)}$ border may cause junction breakdown or flashover. Crossing the hyperbolic power dissipation border P_{tot} will end in thermal and/or electrical over stress (EOS) causing partial burn outs in the die (crystal) active areas. Some devices allow the limit to be crossed in pulsed operation. Crossing the border for a long time can cause reliability problems, though, with reduction of lifetime and permanent non-repairable damage to the device. This chapter will primarily discuss the thermal limit specified by the maximum semiconductor junction temperature T_j, total power dissipation P_{tot} and thermal resistance R_{th}.

Typically, data sheets give the thermal resistance in order of primary heat sinking from junction to the case surrounded by ambient. With smaller and smaller SMD packages, cooling by radiation to the ambient is rapidly dropping. Power dissipation sinking effects that could be ignored for leaded and large-scale SMD packages therefore become important for very small packages.

1.1.1 Definitions

Thermal conductivity from a hot to a cold point: $T_{Cold} = T_{Hot} - \left(R_{th(H-C)} \cdot P_D\right)$

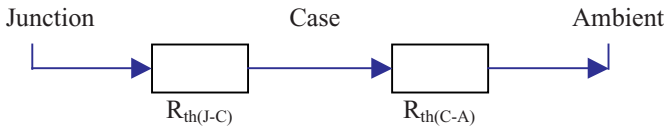
Simplified: $R_{th} = \frac{\Delta T}{P_D}$ compared to Ohm's law: $R = \frac{V}{I}$



Series cascaded R_{th}'s can be added. For parallel-cascaded Rth's, the conductivities are added (valid at common temperature gradients).

T_j: typ. 150°C to 175°C for Si, (see data sheet for details)
T_A: Ambient temperature / [°C]
T_S: Solder point temperature / [°C]
P_D: Power dissipation / [W]
P_{tot}: Limiting total power dissipation / [W]

1.1.2 SMD with primary heat sinking to ambient

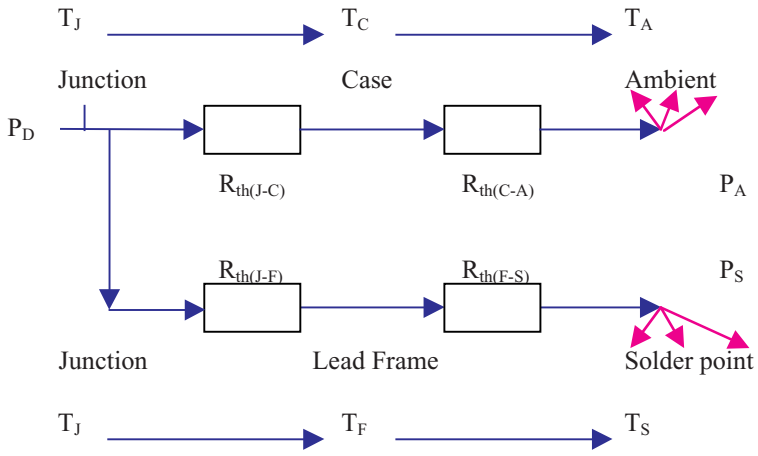


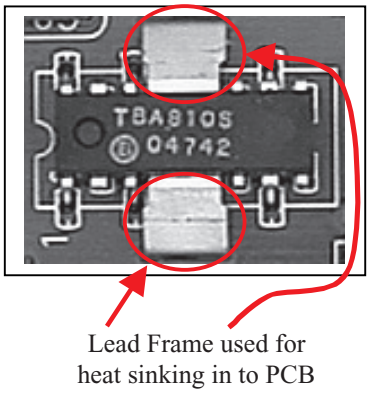
$$T_j = T_A + \left(R_{th(J-A)} \cdot P_D\right)$$

The data sheet gives the limiting junction temperature T_j generated in the active semiconductor area of the die (crystal). The resulting power dissipation is radiated into the case (package), which has a limited thermal conductivity $R_{th(J-C)}$. The thermally loaded package radiates the heat into the ambient with a certain efficiency or thermal conductivity $R_{th(C-A)}$. Typically, data sheets give $R_{th(J-A)}=R_{th(J-C)}+R_{th(C-A)}$. The radiated power from the case to the ambient is a function of the air contacting the device's surface, how the air circulates, ambient temperature T_A and several more factors. Heatsinks can improve thermal conductivity to the air by increasing the surface contacting the air (decreasing $R_{th(C-A)}$) and by causing thermal air currents like the drawing effect in a chimney.

1.1.3 SMD with heat sinking to ambient and into solder leads (lead frame = Ts)

The lead frame and solder leads do not have thermal junctions (see package of TBA810 audio power amplifier).





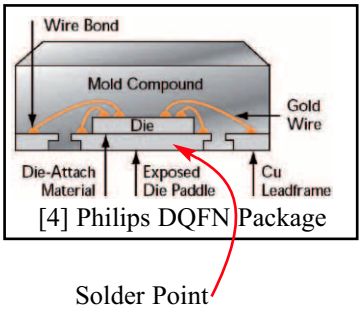
For small SMD packages, a measurable amount of thermal power sinks via the leads into the solder point. From there, the heat is radiated into the PCB lines and substrate. Because of this, the definition of the thermal resistance from the case to the air, $R_{th(J-A)}$, becomes less important for SMD packages which have only small surfaces in contact with air. There, the thermal resistance from the case to the solder point $R_{th(C-S)}$. becomes much more dominant. Philips therefore uses $R_{th(J-S)}$ for transistors like the ***PMBFJ620*** in the SOT363 package.

(1) $P_D = P_A + P_S$

P_D = Total sum of the thermal power sinking from the package

P_A = Power sinking to ambient

P_S = Power sinking to solder point



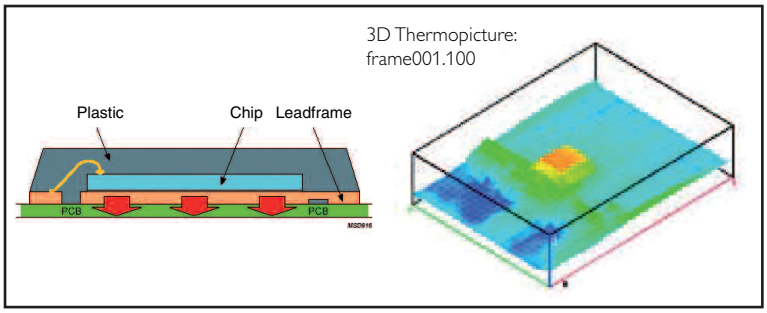
(2) $T_J - T_S = P_S * \left(R_{th(J-F)} + R_{th(F-S)}\right)$

(3) $P_S = \dfrac{T_J - T_S}{\left(R_{th(J-F)} + R_{th(F-S)}\right)}$

(4) $T_J - T_A = P_A * \left(R_{th(J-C)} + R_{th(C-A)}\right)$

(5) $P_A = \dfrac{T_J - T_A}{\left(R_{th(J-C)} + R_{th(C-A)}\right)}$

Thermal pictures, QLPAK and LFPAK package [5]



In contrast to the SO8 package, the primary thermal pathway in QLPAK and LFPAK packages is straight down through the metal leadframe of the package. This is a much more direct pathway and has a typical thermal resistance of less than 1.5 K/W similar to that found in power packages such as D-Pak and D2-Pak, and an enormous improvement to that found in SO8.

(6) $P_D = P_A + P_S = \dfrac{T_J - T_A}{\left(R_{th(J-C)} + R_{th(C-A)}\right)} + \dfrac{T_J - T_S}{\left(R_{th(J-F)} + R_{th(F-S)}\right)}$

(7) $P_D = \dfrac{\left(T_J - T_A\right)\cdot\left(R_{th(J-F)} + R_{th(F-S)}\right) + \left(T_J - T_S\right)\cdot\left(R_{th(J-C)} + R_{th(C-A)}\right)}{\left(R_{th(J-C)} + R_{th(C-A)}\right)\cdot\left(R_{th(J-F)} + R_{th(F-S)}\right)}$

(8)
$P_D \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)\cdot\left(R_{th(J-F)} + R_{th(F-S)}\right) = \left(T_J - T_A\right)\cdot\left(R_{th(J-F)} + R_{th(F-S)}\right) + \left(T_J - T_S\right)\cdot\left(R_{th(J-C)} + R_{th(C-A)}\right)$

(9) $Y = T_J \cdot \left(R_{th(J-F)} + R_{th(F-S)}\right) - T_A \cdot \left(R_{th(J-F)} + R_{th(F-S)}\right) + T_J \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right) - T_S \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)$

(10) $Y = T_J \cdot \left[\left(R_{th(J-F)} + R_{th(F-S)}\right) + \left(R_{th(J-C)} + R_{th(C-A)}\right)\right] - T_A \cdot \left(R_{th(J-F)} + R_{th(F-S)}\right) - T_S \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)$

(11) $T_J = \dfrac{P_D \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)\cdot\left(R_{th(J-F)} + R_{th(F-S)}\right) + T_A \cdot \left(R_{th(J-F)} + R_{th(F-S)}\right) + T_S \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)}{\left(R_{th(J-F)} + R_{th(F-S)}\right) + \left(R_{th(J-C)} + R_{th(C-A)}\right)}$

Substituting k

(12) $k \cdot T_J = P_D \cdot w + T_A \cdot \left(R_{th(J-F)} + R_{th(F-S)}\right) + T_S \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)$

For primary heat sinking into solder point:

(13) $\lim\limits_{\substack{R_{th(J-F)}\to 0 \\ R_{th(F-S)}\to 0}} \left(k \cdot T_J\right) = P_D \cdot w + T_S \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)$

(14) $k \cdot T_J \approx P_D \cdot w + T_S \cdot \left(R_{th(J-C)} + R_{th(C-A)}\right)$

(15) $T_J \approx P_D \cdot \dfrac{\left(R_{th(J-C)} + R_{th(C-A)}\right)\cdot\left(R_{th(J-F)} + R_{th(F-S)}\right)}{\left(R_{th(J-C)} + R_{th(C-A)}\right) + \left(R_{th(J-F)} + R_{th(F-S)}\right)} + T_S \cdot \dfrac{\left(R_{th(J-C)} + R_{th(C-A)}\right)}{\left(R_{th(J-C)} + R_{th(C-A)}\right) + \left(R_{th(J-F)} + R_{th(F-S)}\right)}$

(16) $T_J \approx P_D \cdot \dfrac{1}{\dfrac{1}{\left(R_{th(J-C)} + R_{th(C-A)}\right)} + \dfrac{1}{\left(R_{th(J-F)} + R_{th(F-S)}\right)}} + T_S \cdot \dfrac{\left(R_{th(J-C)} + R_{th(C-A)}\right)}{\left(R_{th(J-C)} + R_{th(C-A)}\right) + \left(R_{th(J-F)} + R_{th(F-S)}\right)}$

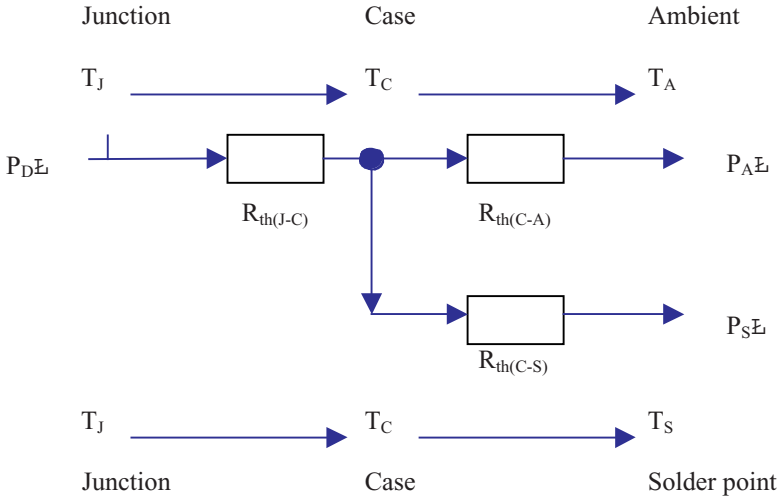
$R_{th(C-A)}$ is very large for negligible heat sinking to ambient.

(17) $\boxed{T_J \approx P_D \cdot \left(R_{th(J-F)} + R_{th(F-S)}\right) + T_S \cdot \dfrac{\left(R_{th(J-C)} + R_{th(C-A)}\right)}{\left(R_{th(J-C)} + R_{th(C-A)}\right) + \left(R_{th(J-F)} + R_{th(F-S)}\right)}}$

Equation (15) shows that, for primary heat sinking into the solder point, the influence of T_A can be neglected.

1.1.4 SMD with heat sinking into ambient and into solder leads (bond wire = Ts)

The lead frame and solder lead have thermal junctions. That means all of a device's active contacts are only available via bond-pads, and the primary heat is generated on the die's surface. Because of this, the heat sink through the silver-filled epoxy die attached to the lead-frame can be neglected.



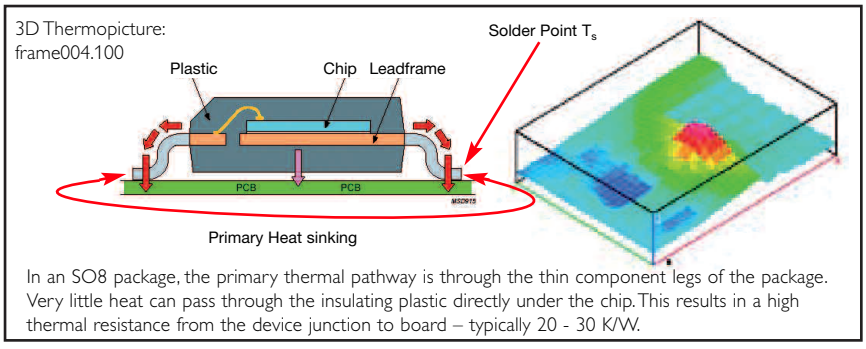
This indicates different thermal conduction streams into the ambient (P_A) and the solder-point (P_S).

(1) $P_D = P_A + P_S$

(2) $P_D = \frac{T_C - T_A}{R_{th(C-A)}} + \frac{T_C - T_S}{R_{th(C-S)}}$

(3) $P_D = \frac{T_J - T_C}{R_{th(J-C)}}$

Equation (2) can also be written:



In an SO8 package, the primary thermal pathway is through the thin component legs of the package. Very little heat can pass through the insulating plastic directly under the chip. This results in a high thermal resistance from the device junction to board – typically 20 - 30 K/W.

Thermal pictures of SO8 package [5]

(4) $P_D = \frac{(T_C - T_A)\cdot R_{th(C-S)} + (T_C - T_S)\cdot R_{th(C-A)}}{R_{th(C-A)} \cdot R_{th(C-S)}}$

(5) $P_D \cdot R_{th(C-A)} \cdot R_{th(C-S)} = T_C \cdot (R_{th(C-S)} + R_{th(C-A)}) - T_A \cdot R_{th(C-S)} - T_S \cdot R_{th(C-A)}$

(6) $T_C \cdot (R_{th(C-S)} + R_{th(C-A)}) = P_D \cdot R_{th(C-A)} \cdot R_{th(C-S)} + T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}$

(7) $T_C = \frac{P_D \cdot R_{th(C-A)} \cdot R_{th(C-S)} + T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}}{(R_{th(C-S)} + R_{th(C-A)})}$

Rewriting (3) for T_C

(8) $T_C = T_J - P_D \cdot R_{th(J-C)}$

Substituting (8) into (7)

(9) $T_J - P_D \cdot R_{th(J-C)} = \dfrac{P_D \cdot R_{th(C-A)} \cdot R_{th(C-S)} + T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

(10) $T_J = \dfrac{P_D \cdot R_{th(C-A)} \cdot R_{th(C-S)} + T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)} + P_D \cdot R_{th(J-C)}$

(11) $T_J = \dfrac{P_D \cdot R_{th(C-A)} \cdot R_{th(C-S)} + T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)} + P_D \cdot R_{th(J-C)} \cdot \left(R_{th(C-S)} + R_{th(C-A)}\right)}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

(12) $T_J = \dfrac{P_D \cdot \left[R_{th(C-A)} \cdot R_{th(C-S)} + R_{th(J-C)} \cdot \left(R_{th(C-S)} + R_{th(C-A)}\right)\right] + T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

(13) $T_J = P_D \cdot \dfrac{R_{th(C-A)} \cdot R_{th(C-S)} + R_{th(J-C)} \cdot \left(R_{th(C-S)} + R_{th(C-A)}\right)}{\left(R_{th(C-S)} + R_{th(C-A)}\right)} + \dfrac{T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

(14) $T_J = P_D \cdot \left[R_{th(J-C)} + \dfrac{R_{th(C-A)} \cdot R_{th(C-S)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}\right] + \dfrac{T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

(15) $T_J = P_D \cdot \left(R_{th(J-C)} + \dfrac{1}{\dfrac{1}{R_{th(C-A)}} + \dfrac{1}{R_{th(C-S)}}}\right) + \dfrac{T_A \cdot R_{th(C-S)} + T_S \cdot R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

$R_{th(C-A)}$ is very large for negligible heat sinking to ambient.

(16) $T_J \approx P_D \cdot \left(R_{th(J-C)} + R_{th(C-S)}\right) + T_A \cdot \dfrac{R_{th(C-S)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)} + T_S \cdot \dfrac{R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

(17) $T_J \approx P_D \cdot \left(R_{th(J-C)} + R_{th(C-S)}\right) + T_A \cdot \dfrac{1}{\left(1 + \dfrac{R_{th(C-A)}}{R_{th(C-S)}}\right)} + T_S \cdot \dfrac{1}{\left(\dfrac{R_{th(C-S)}}{R_{th(C-A)}} + 1\right)}$

(18) $T_J \approx P_D \cdot \left(R_{th(J-C)} + R_{th(C-S)}\right) + T_A \cdot \dfrac{R_{th(C-S)}}{R_{th(C-A)}} + T_S \cdot \dfrac{R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

(19) $T_J \approx P_D \cdot \left(R_{th(J-C)} + R_{th(C-S)}\right) + T_S \cdot \dfrac{R_{th(C-A)}}{\left(R_{th(C-S)} + R_{th(C-A)}\right)}$

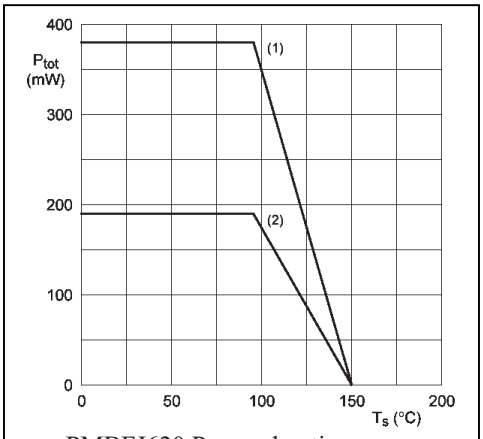
For a good thermal heat sink from the case to the heat sinking solder point: $R_{th(C-S)} << R_{th(C-A)}$

(20) $\boxed{T_J \approx P_D \cdot \left(R_{th(J-C)} + R_{th(C-S)}\right) + T_S}$

(21) $\boxed{R_{th(J-S)} = R_{th(J-C)} + R_{th(C-S)}}$

Example applied to ***PMBFJ620*** data sheet:

Single loaded:	$R_{th(J-S)}$=315K/W
Double loaded:	$R_{th(J-S)}$=160K/W
Max. Junction Temperature:	T_J=150˚C



PMBFJ620 Power derating curve
(1) Double loaded
(2) Single loaded

1.2 Example applied to the JFET family 310

Type	Package	Function	Rth / [K/W]	PTOT / [mW]	Condition
J310	TO92	single JFET	$R_{th(j-a)}$=250	400	assy on PCB
PMBFJ310	SOT23	single JFET	$R_{th(j-a)}$=500	250	assy on FR4
PMBFJ620	SOT363	double JFET	$R_{th(j-s)}$=315	190	single loaded
			$R_{th(j-s)}$=160		double loaded

Example:
JFET with biasing V_{DS}=9V, I_D=10mA. Determine the maximum environment temperature.

$P_D=V_{DS}*I_D$=9V*10mA=90mW

For single JFET package:

$$T_A = T_J - \left(R_{th(J-A)} \cdot P_D\right)$$

For ***J310*** in TO92: $T_A = 150°C - \left(400K/W \cdot 90mW\right) = 114°C$

For ***PMBFJ310*** in SOT23: $T_A = 150°C - \left(250K/W \cdot 90mW\right) = 127.5°C$

For PMBFJ620 in SOT363 package:

$$T_S = T_J - \left(R_{th(J-S)} \cdot P_D\right)$$

Single loaded:
One JFET used
$P_{DS}=P_T$=100mW
$R_{thS(J-S)}$=315K/W

$T_S = 150°C - \left(315K/W \cdot 90mW\right)$

T_S=121.65˚C

Double loaded:
Two JFETs used
$P_{DD}=2*P_T$=180mW
$R_{thD(J-S)}$=160K/W

$T_S = 150°C - \left(160K/W \cdot 180mW\right)$

T_S=121.2˚C

Only one JFET is used in single load, and this can be loaded up to 190mW.
Two JFETs are used in double load, and each JFET can be loaded up to 95mW.

The max. solder point temperature for max. load is:

Single loaded:
$T_S = 150°C - \left(315K/W \cdot 190mW\right)$

T_S=90.15˚C

Double loaded:
$T_S = 150°C - \left(160K/W \cdot 190mW\right)$

T_S=119.6˚C

1.2.1 Derating diagram PMBFJ620 in SOT363

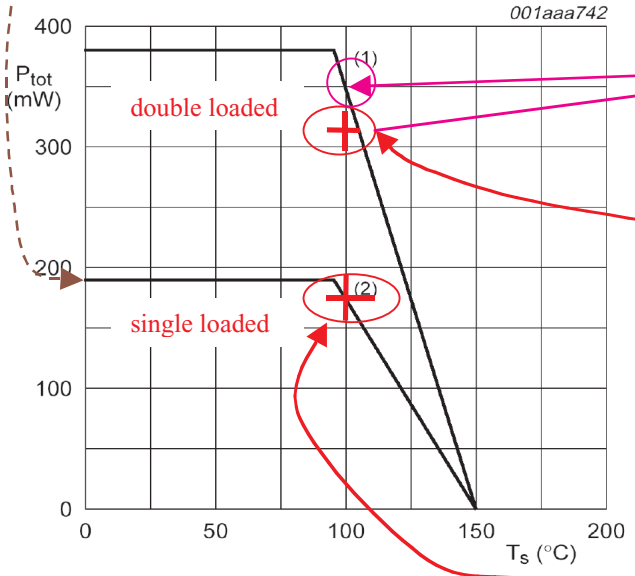
Tabel 5: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Max	Unit
Per FET					
V_{DS}	drain-source voltage		-	±25	V
V_{GSO}	gate-source voltage	open drain	-	-25	V
V_{GDO}	drain-gate voltage	open source	-	-25	V
I_G	forward gate current (DC)		-	50	mA
P_{tot}	total power dissipation	$T_s \leq 90°C$	-	190	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	150	°C

Table 6: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-s)}$	thermal resistance from junction to soldering points	single loaded	*315	K/W
		double loaded	*160	K/W

*T_s is the temperature at the soldering point of the gate pins, see Figure 1.



! Deviation !

(1) Double loaded.
(2) Single loaded.

Fig 1. Power derating curve.

Example P_D for the trace crossing the 100°C border:

$$P_D = \frac{T_J - T_S}{R_{th(J-S)}}$$

Single loaded:

$$P_D = \frac{150°C - 100°C}{315K/W} = 158.7mW$$

Double loaded:

$$P_D = \frac{150°C - 100°C}{160K/W} = 312.5mW$$

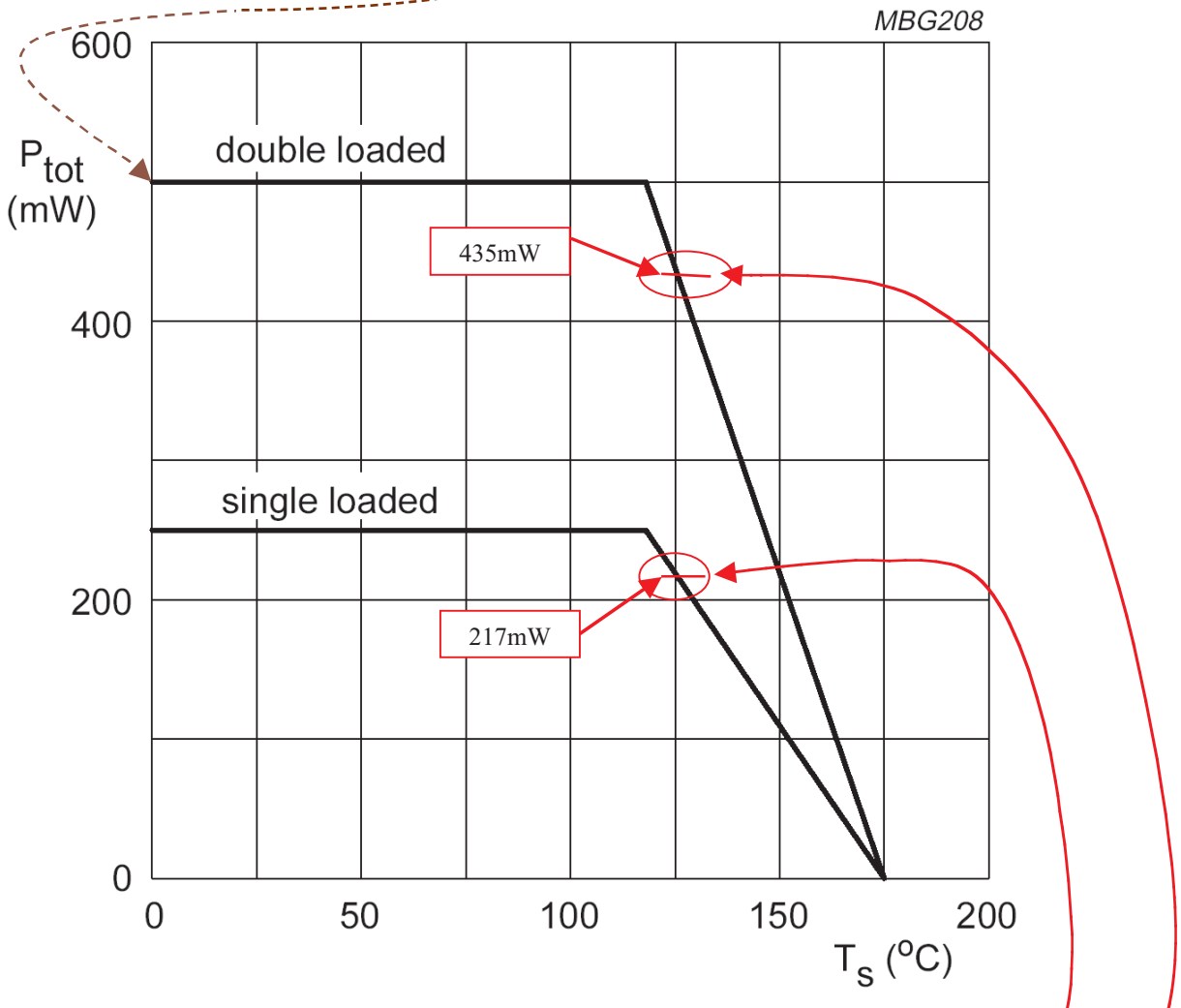
1.2.2 Cross checking: Derating diagram BFC505 in SOT353

I_c	DC collector current		-	18	mA
P_{tot}	total power dissipation	up to T_s = 118˚C; note 1	-	500	mW
T_{stg}	storage temperature		-65	+175	˚C
T_j	junction temperature		-	175	˚C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point; note 1	single loaded	230	K/W
		double loaded	115	K/W

Note to the limiting values and Thermal characteristics.
1. T_s is the temprature at the soldering point of the collector pin.



Single loaded trace crossing the 125˚C border: $P_d = \frac{175°C - 125°C}{230K/W} = 217mW$

Double loaded trace crossing the 125˚C border: $P_d = \frac{175°C - 125°C}{115K/W} = 435mW$

→ → → The diagram confirms the algebraic evaluation!!

1.2.3 Cross checking: Derating diagram BFG480W in SOT343R

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CBO}	collector-base voltage	open emitter	-	14.5	V
V_{CEO}	collector-emitter voltage	open base	-	4.5	V
V_{EBO}	emitter-base voltage	open collector	-	1	V
I_c	collector current (DC)		-	250	mA
P_{tot}	total power dissipation	$T_s \leq 60°C$; note 1; see Fig. 2	-	360	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	operating junction temperature		-	150	°C

Note 1. T_s is the temperature at the soldering point of the emitter pins.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	250	K/W

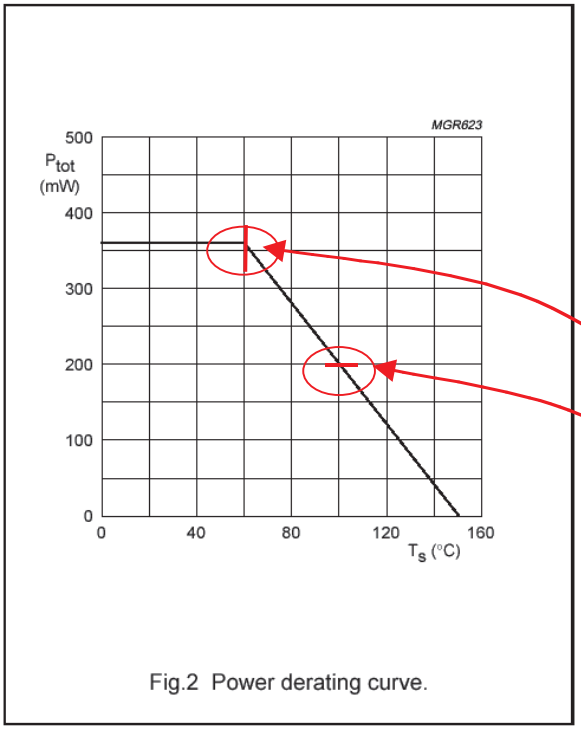


Fig.2 Power derating curve.

$$P_D = \frac{T_j - T_S}{R_{th(j-S)}} = \frac{150°C - 100°C}{250K/W} = 200mW$$

$$T_S = T_j - \left(R_{th(j-S)} \cdot P_D\right) = 150°C - \left(250K/W \cdot 360mW\right) = 60°C$$

→ → → The diagram confirms the algebraic evaluation!!

2. GH404 with TZA30x6

2.1 Introduction

The TZA3026, TZA3036 and TZA 046 are transimpedance amplifiers used for SDH/Sonet and FiberChannel/Gigabit Ethernet applications. In general, these devices are delivered as dies only. For this reason, the GH404 application board has been designed to enable and ease evaluation of the Philips TIA family members being assembled in a 4 or 5 pin ROSA (receiver optical sub-assembly).
The following describes the GH404 and its usage. For all three devices, the typical measurement results shown have been achieved with ROSAs assembled by OECA (http://www.oeca.de/). The measurement set-up is described, and the schematics of the GH404 and the component placement of the PCB top layer are given.

2.2 Connecting the GH404 board

The GH404 application board contains SMA and SMB connectors providing access to all relevant TIA signals, available on the ROSA pins. The application board is shown in Figure 1:

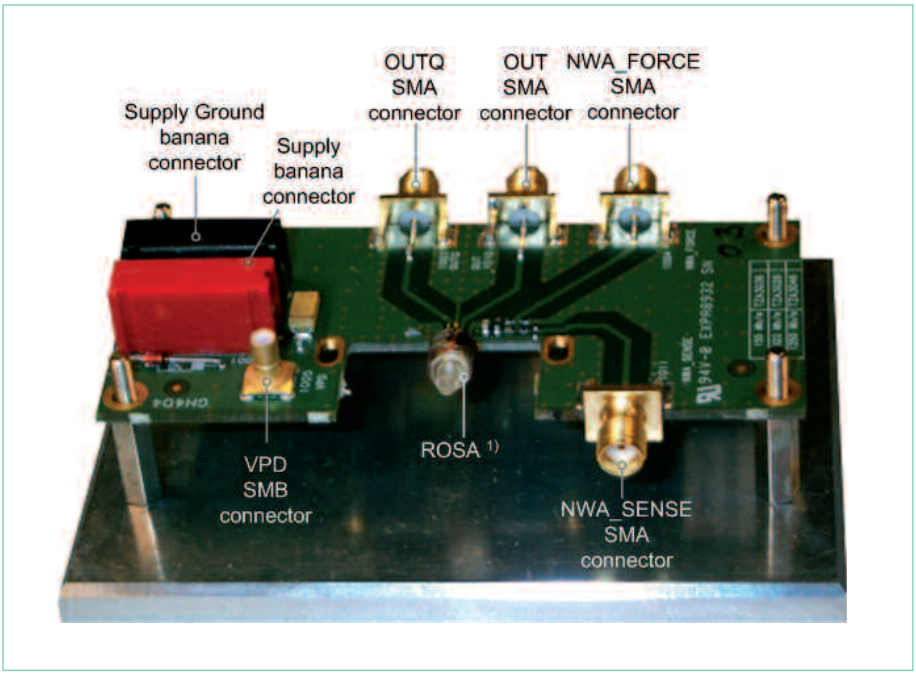


Figure 1 GH404 board connectors

Table 1 gives a brief description of the signals on the GH404 connectors.

Table 1 GH404 connectors

Connector name	Description
Supply, Supply ground	Power supply for the ROSA (3.3V)
Out, OutQ	Differential ROSA signal output
NWA_Force, NWA_Sense	Power Supply Rejection Ratio measurement connectors
VPD	Photo Detector Monitor voltage
ROSA	Receiver Optical Sub-Assembly[1]), containing the TZA3026/36/46 TIA.
	[1]) The picture shows a ROSA without receptacle

2. 3 ROSA

2.3.1 Connection

The ROSA can either be directly connected to the board as shown in Figure 1, or be part of a receptacle as shown in Figure 2. In both cases the pinning of the ROSA should be according to Figure 2.

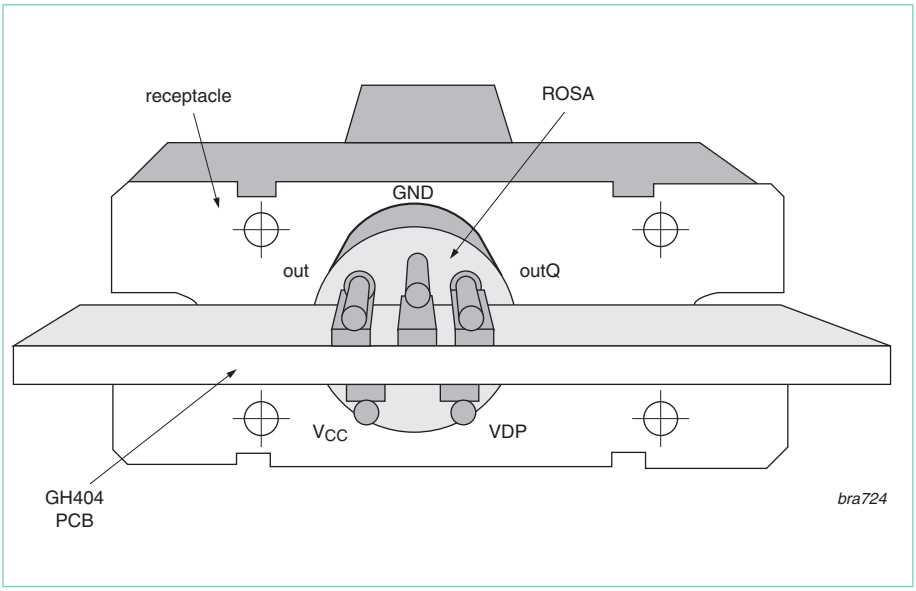


Figure 2 ROSA to PCB connection

2.3.2 Construction

The measured optical assemblies have been constructed by OECA (http://www.oeca.de/). The construction of the assembly incorporating the TZA3026 can be seen in Figure 3.

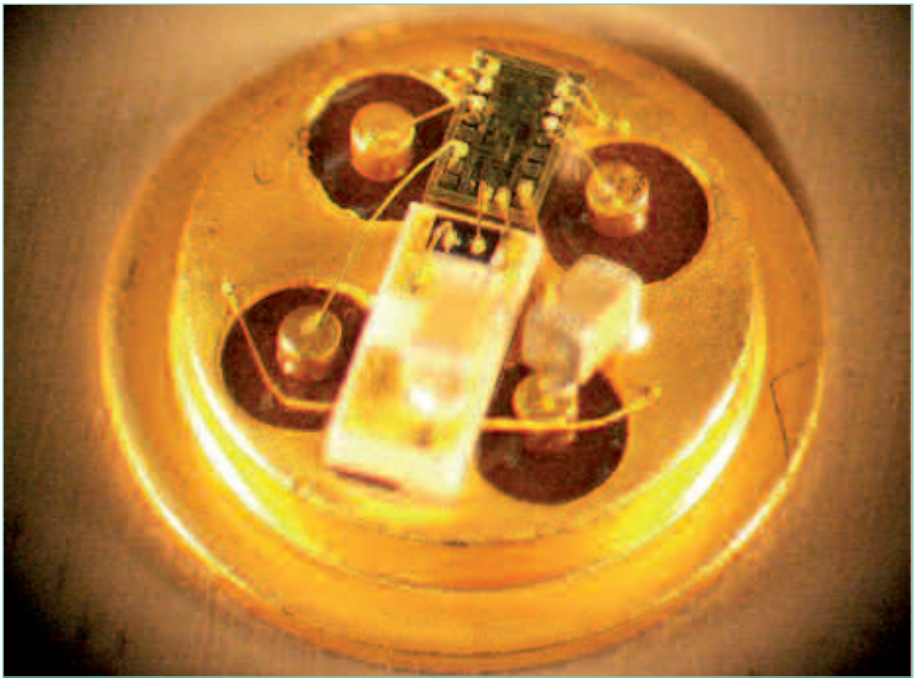


Figure 3 ROSA internal construction

2.3.3 Design hints

The sensitivity of an optical receiver is mostly determined by the total amount of noise present at the input of the TIA. This total noise comprises the noise of the TIA itself, and externally added noise. The noise of the TZA30x6 is fixed by design, and the datasheets specify its value as total integrated RMS noise over the bandwidth: $I_{n(tot)(rms)}$. In contrast, the external noise contribution is influenced by the construction of the optical assembly.

The ROSA must be properly designed to minimize noise and so achieve good sensitivity.

Basically, two noise adding mechanisms exist (see Figure 4):

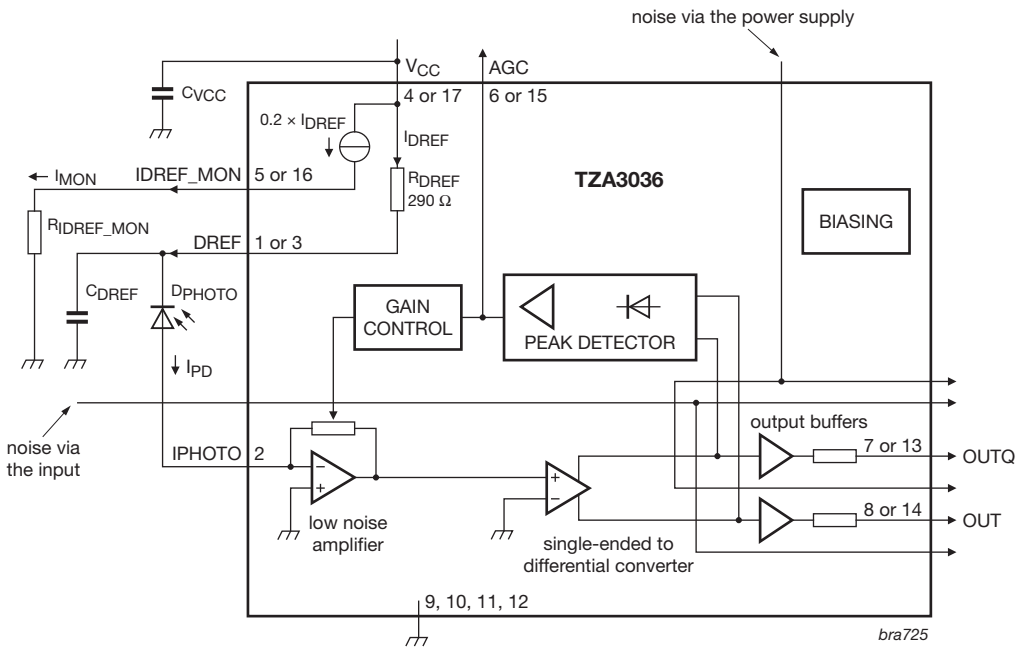


Figure 4 Noise adding mechanisms

First, noise can be coupled directly to the input of the TIA and hence amplified along with the desired signal. Second, noise can be added via the power supply and thus superimposed onto the amplifying chain.

To achieve good immunity against these external noise contributions, bear in mind the following hints when designing a ROSA (please also refer to Figure 5 and Figure 6). The examples also show some options for constructing a ROSA (e.g. using either SMD type or die-type capacitors, and using laminates to carry the capacitors and the photodiode).

Basically, the design of the ROSA is simplified by the symmetrical port layout of the TIAs. With the exception of IPHOTO/pin 2, the layout makes each port available at least twice.

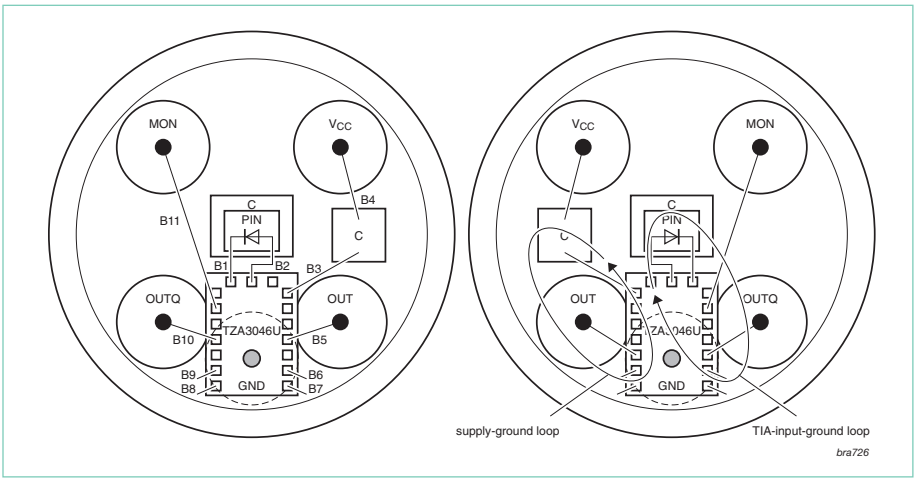


Figure 5 Data sheet application recommendations

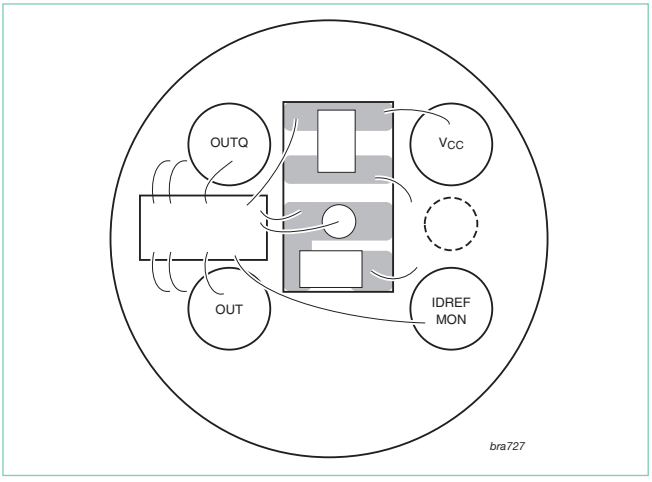


Figure 6 ROSA layout using TZA30x6 and laminate

Layout design hints:

- Minimize the coupling to the TIA input:
  - Place the photodiode as close as possible to the TIA and minimize the length of the bond-wires B1 (DREF) and B2 (IPHOTO) that connect the photodiode to pin 2 and pin 3 respectively
  - The coupling of the bond-wire B2 to bond-wire B4, which connects capacitor C_{VCC} to the supply VCC, should also be minimized
  - The bond-wires of the differential output, B5 and B10, should be kept as short as possible and placed orthogonally to the bond-wire of the TIA input, B1
- Optimize the power de-coupling network:
  - Place the de-coupling capacitor, C_{VCC}, between the TIA and the VCC connection of the ROSA to create an L-C-L network
  - Minimize the length of the respective interconnecting bond-wires, B3 and B4
- Provide proper grounding:
  - Provide a good common grounding, e.g. the plate of a TO can
  - Use all ground die pads (pins 9 to pin 12) to connect using short bond-wires, B6 to B9, to the common ground plane
  - Do not place the ground bond-wires, B6..B9, parallel to the bond-wires of the output, B5 and B10
  - Avoid common impedances to ground, e.g. connect C_{VCC} and C_{DREF} separately to ground
- Minimize the area and thus the radiation/coupling of the following loops:
  - TIA Input: C_{DREF} -> GND -> GND_{TIA} -> Pin 2 -> D_{PHOTO} -> C_{DREF}
  - Supply: C_{VCC} -> GND -> GND_{TIA} -> Pin 4/17 -> C_{VCC}

2.4. Measurements

The following chapters give measurement results from the TZA3026, TZA3036 and TZA3046 ROSA on the GH404 application board. These results have been obtained by using the set-ups as given in paragraph 4.4.

2.4.1 Measurement results TZA3026

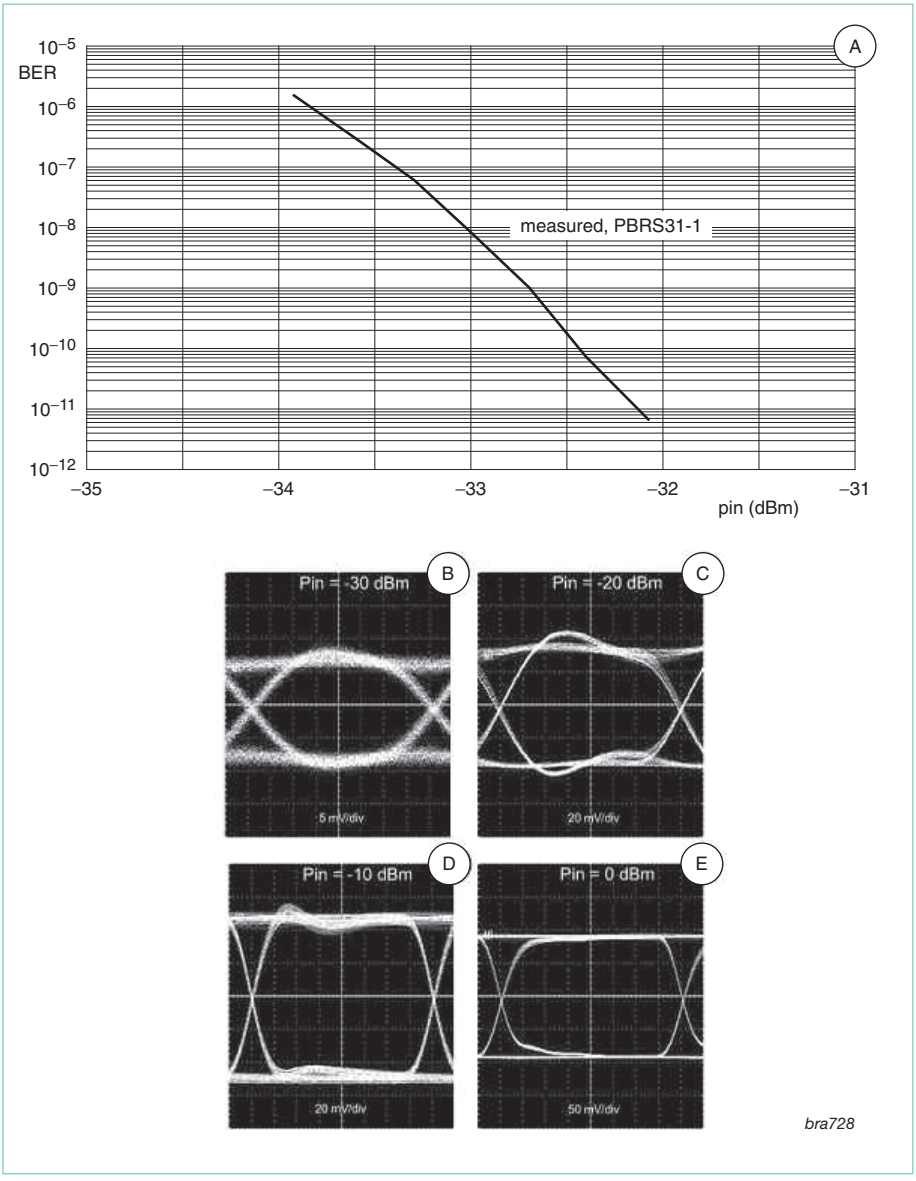


Figure 7 TZA3026 measurement results

2.4.2 Measurement results TZA3036

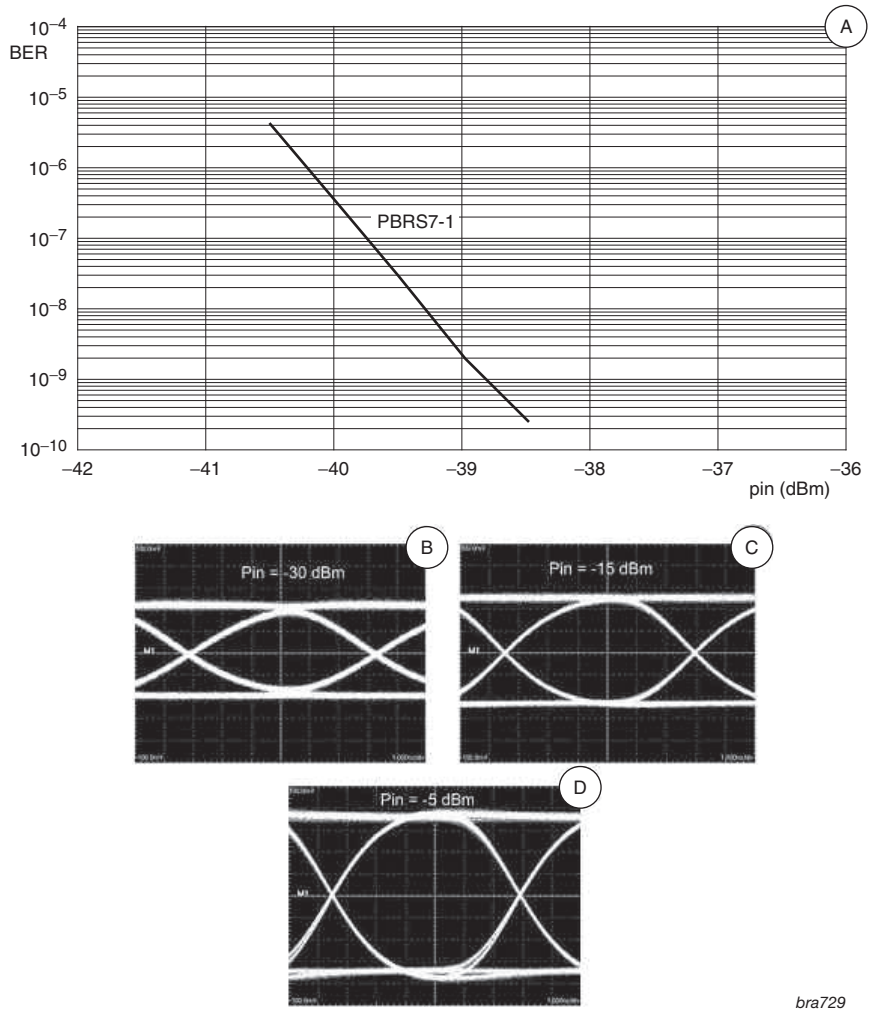


Figure 8 TZA3036 measurement results

2.4.3 Measurement results TZA3046

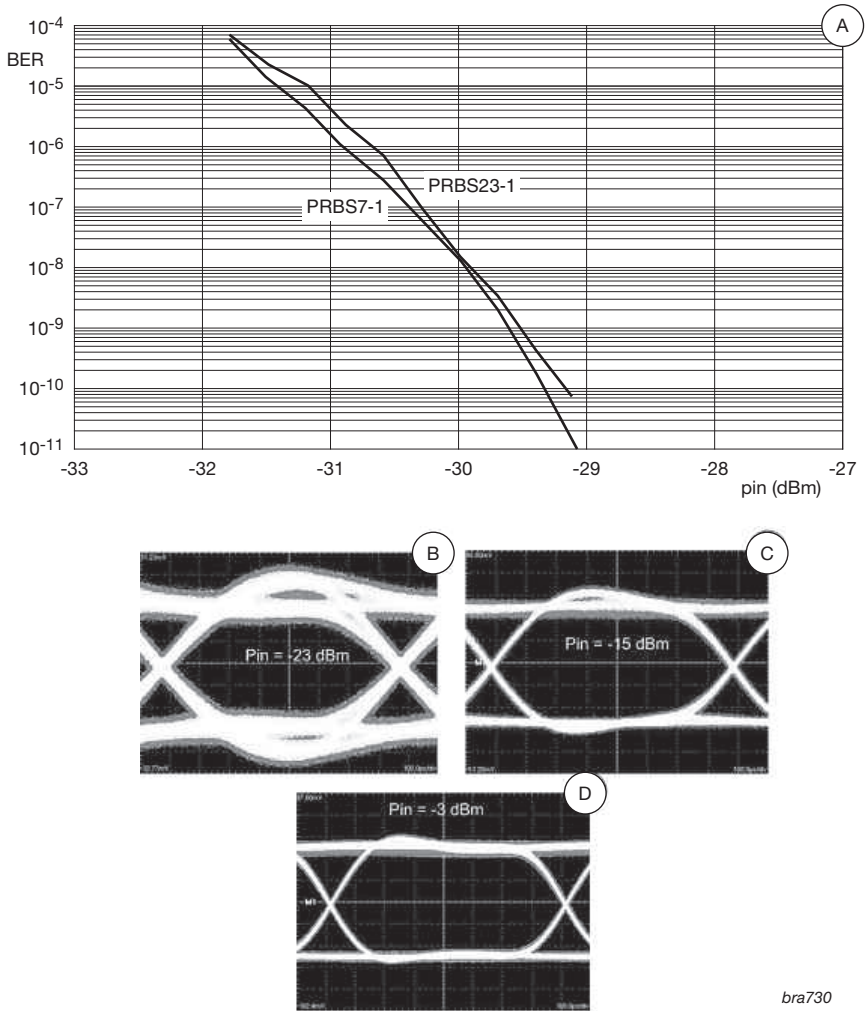
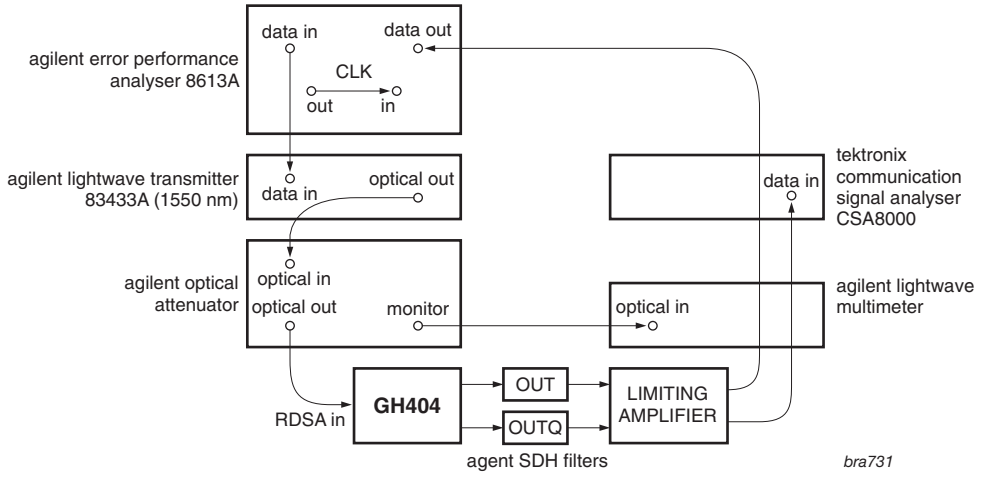


Figure 9 TZA3046 measurement results

2.4.4 Measurement set-ups

General Conditions	value
Supply voltage [VCC]	3.3V
Temperature	22 deg C
Data rate	622 Mbps (TZA3026), 155 Mbps (TZA3036), 1250 Mbps (TZA3046)

Table 2 Measurement conditions

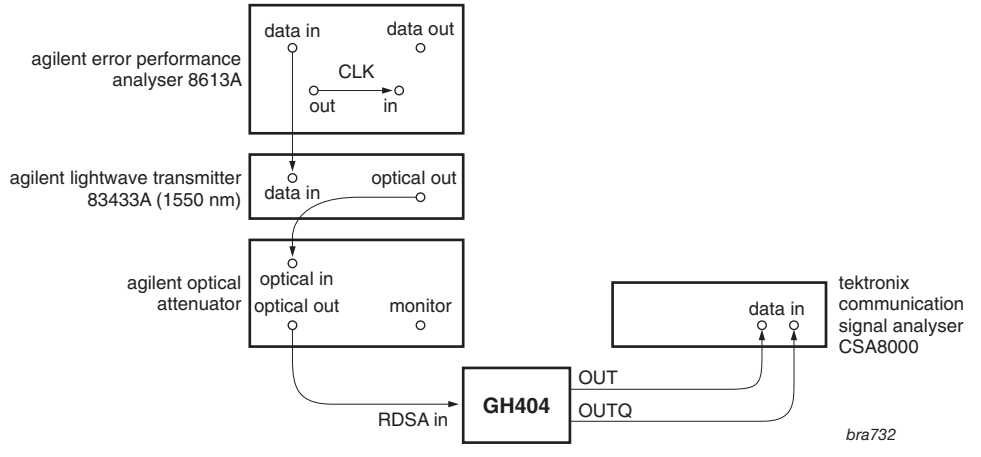


Bit Error Rate measurement

- Attenuator Monitor/Main ratio calibrated at –30 dBm
- For the TZA3036 measurements, the 2014 and 2015 capacitors were replaced by 100 nF versions
- Bandwidth is determined by SDH low pass filters from Agilent:
  TZA3026 Type 87441B / 622 Mbit/s
  TZA3036 Type 87441A / 155 Mbit/s

  TZA3046 No filter used, bandwidth set by 2.2 pF load capacitor

Eye patterns



2.5 Appendix

2.5.1 Schematics

The figures in this section show the schematic of the GH404 application board.
Figure 10 shows the connection of the ROSA to the GH404 application board.

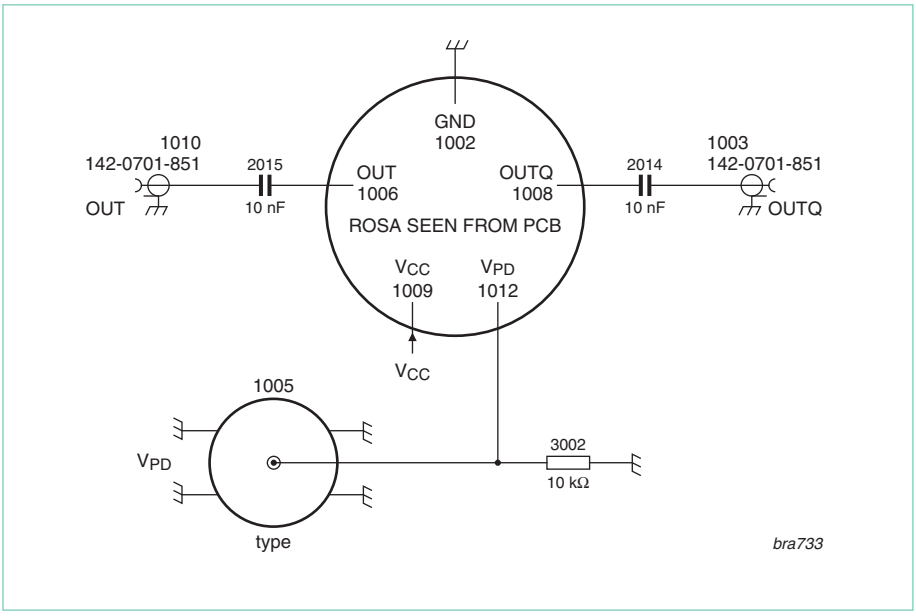


Figure 10 ROSA connection

For Power Supply Rejection Ratio (PSRR) measurements, a small circuit was added to introduce an RF interference component on the DC supply of the TIA. The circuit is shown in Figure 11.

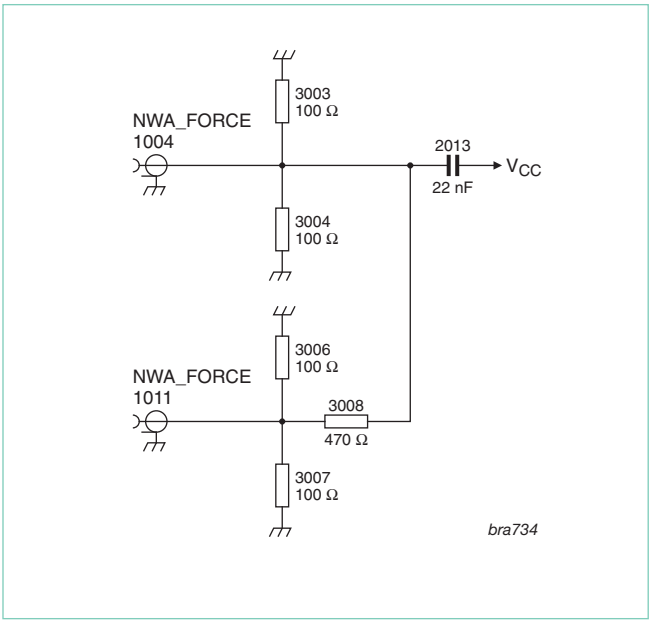


Figure 11 PSRR measurement circuit

The power supply circuit is shown in Figure 12. This circuit contains a reverse polarity protection diode and a zener diode for over-voltage protection when used with a current limited power supply.

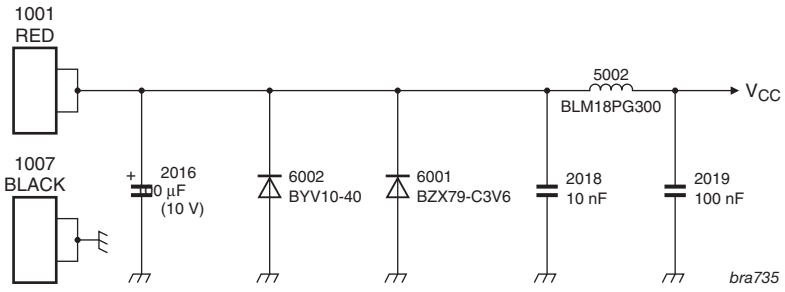


Figure 12 Power supply circuit

2.5.2 Component placement

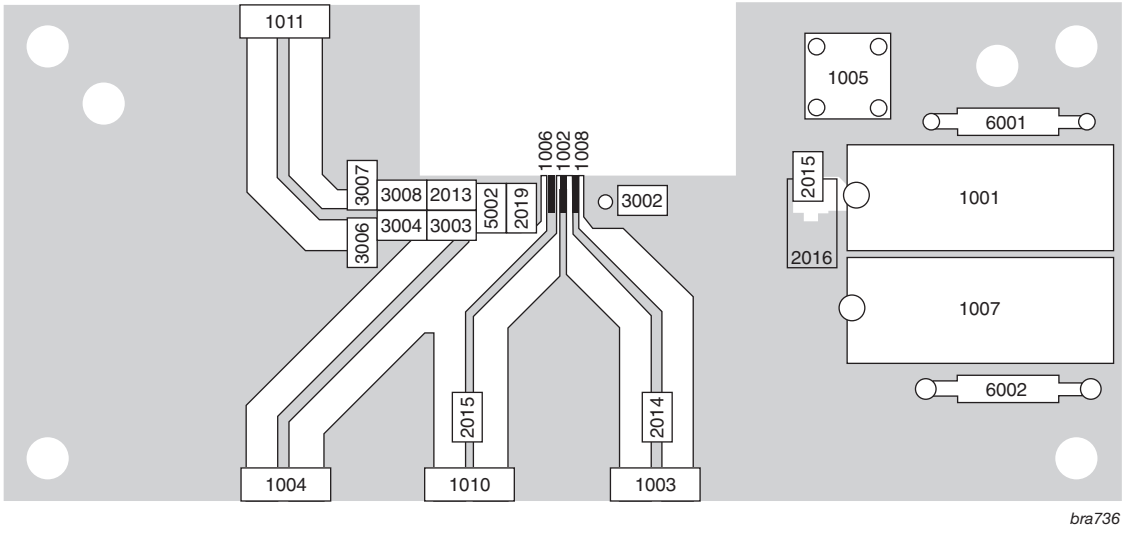


Figure 13 Layout and component placement top side

2.6 Disclaimers

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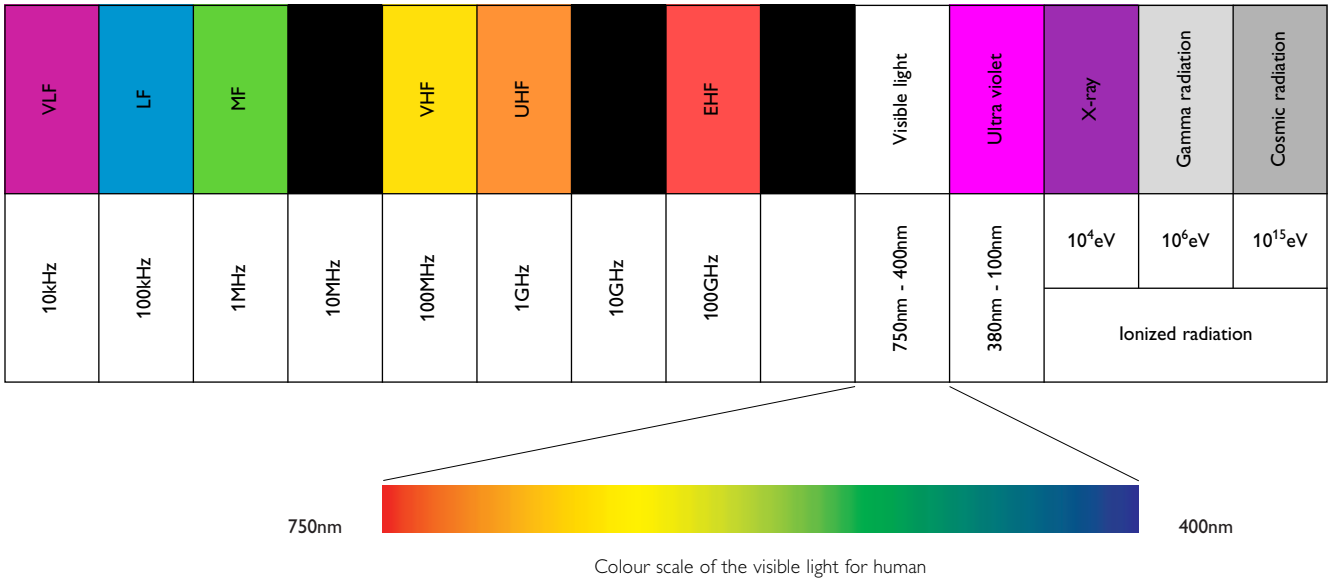
3. RF Application-Basics

3.1 Frequency spectrum

Radio spectrum and wavelengths

Each material's composition creates a unique pattern in the radiation emitted. This can be classified in the "frequency" and "wavelength" of the emitted radiation. As electro-magnetic (EM) signals travel with the speed of light, they do have the character of propagation waves.



Colour scale of the visible light for human

A survey of the frequency bands and related wavelengths:

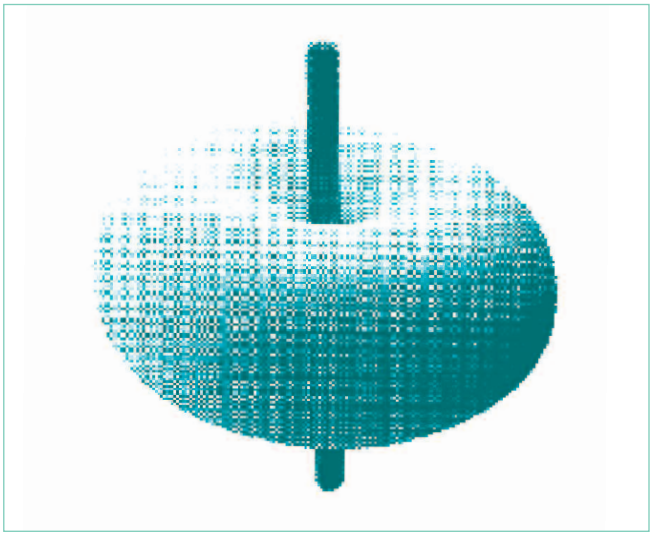
Band	Frequency	Definition	Wavelength - p acc. DIN40015	CCIR Band
VLF	3kHz to 30kHz	Very Low Frequency	100km to 10km	4
LF	30kHz to 300kHz	Low Frequency	10km to 1km	5
MF	300kHz to 1650kHz	Medium Frequency	1km to 100m	6
	1605KHz to 4000KHz	Boundary Wave		
HF	3MHz to 30MHz	High Frequency	100m to 10m	7
VHF	30MHz to 300MHz	Very High Frequency	10m to 1m	8
UHF	300MHz to 3GHz	Ultra High Frequency	1m to 10cm	9
SHF	3GHz to 30GHz	Super High Frequency	10cm to 1cm	10
EHF	30GHz to 300GHz	Extremely High Frequency	1cm to 1mm	11
…	300GHz to 3THz	…	1mm-100µm	12

Literature researches according to the Microwave's sub-bands showed a lot of different definitions with very few or none description of the area of validity. Due to it, the following table will try to give an overview but can't act as a reference.

Source	Nührmann	Nührmann	www.werweiss-was.de	www.atcnea.de	Siemens Online Lexicon	Siemens Online Lexicon	ARRL Book No. 3126	Wikipedia
Validity	IEEE Radar Standard 521	US Military Band	Satellite Uplink	Primary Radar	Frequency bands in the GHz Area	Microwave bands	...	Dividing of Sat and Radar techniques
Band	GHz	GHz	GHz	GHz	GHz	GHz		GHz
A						0,1 - 0,225		
C	4 - 8		3,95 - 5,8	5 - 6	4 - 8	4 - 8	4 - 8	3,95 - 5,8
D		1 - 3						
E		2 - 3					60 - 90	60 - 90
F		2 - 4					90 - 140	
G		4 - 6					140 - 220	
H		6 - 8						
I		8 - 10						
J		10 - 20	5,85 - 8,2					5,85 - 8,2
K	18 - 27	20 - 40	18,0 - 26,5		18 - 26,5	10,9 - 36	18 - 26.5	18 - 26,5
Ka	27 - 40				26,5 - 40	17 - 31	26.5 - 40	26,5 - 40
Ku	12 - 18			≈16	12,6 - 18	15,3 - 17,2	12.4 - 18	12,4 - 18
L	1 - 3	40 - 60	1,0 - 2,6	≈1,3	1 - 2	0,39 - 1,55	1 - 2	1 - 2,6
M		60 - 100						
mm	40 - 100							
P			12,4 - 18,0			0,225 - 0,39	110 - 170	0,22 - 0,3
R			26,5 - 40,0					
Q						36 - 46	33 - 50	33 - 50
S	3 - 4		2,6 - 3,95	≈3	2 - 4	1,55 - 3,9	2 - 4	2,6 - 3,95
U			40,0 - 60,0				40 - 60	40 - 60
V						46 - 56	50 - 75	50 - 75
W							75 - 110	75 - 110
X	8 - 12		8,2 - 12,4	≈10	8 - 12,5	6,2 - 10,9	8 - 12.4	8,2 - 12,4

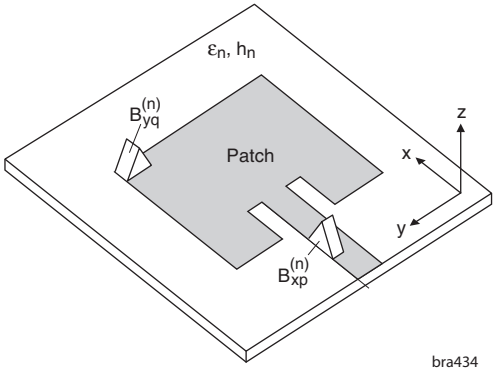
3.2 Function of an antenna

In standard application the RF output signal of a transmitter power amplifier is transported via a coaxial cable to a suitable location where the antenna is installed. Typically the coaxial cable has an impedance of 50Ω (75Ω for TV/Radio). The ether, that is the room between the antenna and infinite space, also has an impedance value. This ether is the transport medium for the traveling wireless RF waves from the transmitter antenna to the receiver antenna. For optimum power transfer from the end of the coaxial cable (e.g. 50Ω) into the ether (theoretical Z=120 πΩ=377Ω), we need a "power matching" unit. This matching unit is the antenna. It does match the cable's impedance to the space's impedance. Depending on the frequency and specific application needs there are a lot of antenna configurations and construction variations available. The simplest one is the isotropic ball radiator, which is a theoretical model used as a mathematical reference.

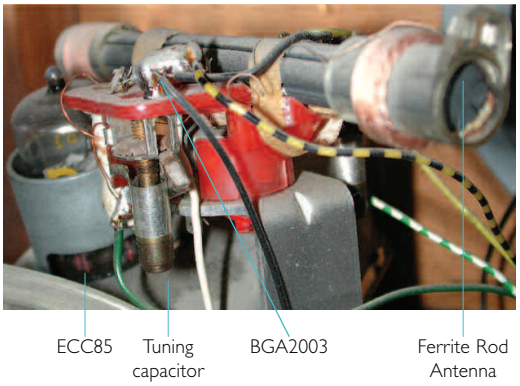


The next simplest configuration and a practical antenna in wide use is the dipole, also called the dipole radiator. It consists of two axial arranged sticks (Radiator). Removal of one Radiator results in to the "vertical monopole" antenna, as illustrated in the adjacent picture. The vertical monopole has a "donut-shaped" field centered on the radiating element.

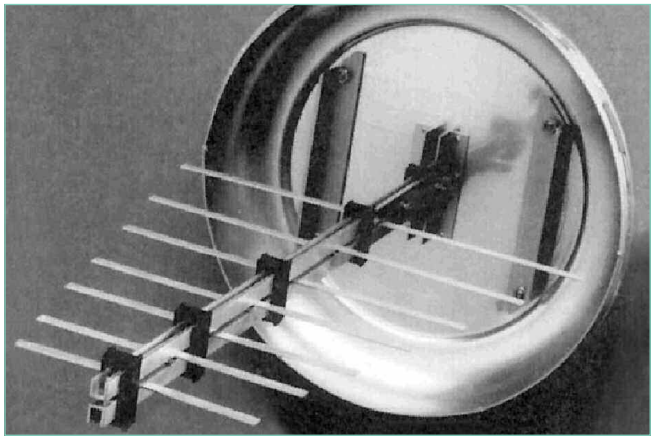
Higher levels of circuitry integration and cost reductions also influence antenna design. Based on the EM field radiation of strip-lines made by printed circuit boards (PCBs), PCB antenna structures were developed called 'patch-antennas' (see diagram). Use of ceramic instead of epoxy dielectric shrinks mechanical dimensions.



In the LF-MF-HF application range, ferrite-rod antennas were commonly used. They compress magnetic fields into a ferrite core, which acts like an amplifier for RF magnetic fields. Coils pick up signals like a transformer. They are a part of the pre-selection LC tank for image rejection and channel selection. The tuner shown is part of a Nordmende Elektra vacuum-tube radio (at least 40 years old and still working). To illustrate its dimensions, a Monolithic Microwave IC is placed in front of a solder point.



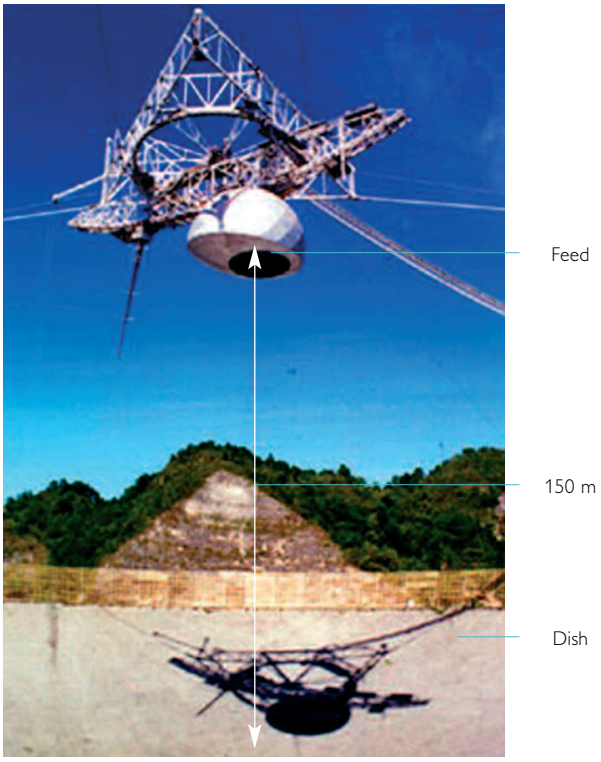
BGA2003



Logarithmic periodic antenna for 406-512 MHz

UHF broadband discone antenna

The Arecibo observatory, in Puerto Rico, is a radio telescope with a dish antenna 305 m in diameter and 51 m deep. The secondary reflector & receiver are located on a 900-ton platform, suspended 137 m in the air above the dish. This is the feed point of an L-band microwave antenna and 50 MHz - 10 GHz antennas used for the SETI@home project. The receiver is cooled down to 50 K using liquid Helium for low-noise operation, to receive weak, distant signals transmitted (potentially) by extraterrestrial intelligence.
The observatory can respond to incoming signals using a transmitter with a balanced klystron amplifier (2.5 kW output peak power; 120 kV / 4.4 A power supply).



The Arecibo observatory, in Puerto Rico

3.3 Transistor semiconductor process

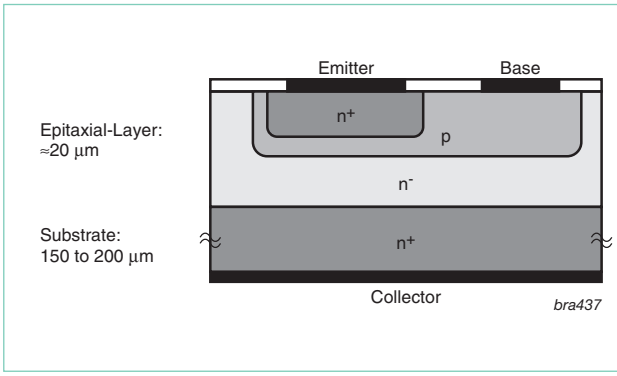
3.3.1 General-purpose small-signal bipolar

The transistor is built up from three different layers:

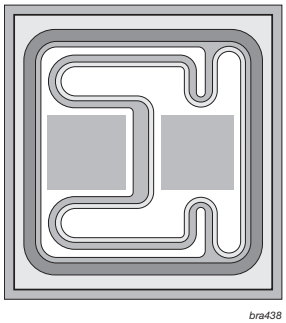
- Highly-doped emitter layer
- Medium-doped base area
- Low-doped collector area.

The highly doped substrate serves as a carrier and conductor only.

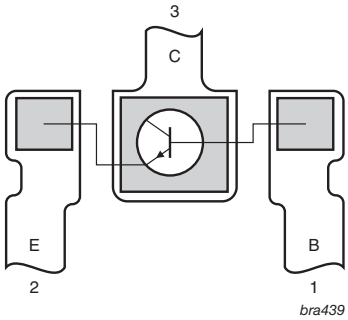
During the assembly process, the transistor die is attached to a lead-frame by gluing or eutectic soldering. The emitter and base contacts are connected to the lead-frame (leads) through bond wires (e.g. gold, aluminum, …) using, for example, an ultrasonic welding process.



NPN Transistor cross section



Die of BC337, BC817



SOT23 standard lead-frame

3.3.2 Double polysilicon

The mobile communications market and the use of ever-higher frequencies mean there is a demand for low-voltage/high-performance RF wideband transistors, amplifier modules and MMICs. To meet that demand, Philips has developed a double-polysilicon process to achieve excellent performance. The 'double-poly' diffusion process uses an advanced transistor technology that is vastly superior to existing bipolar technologies.

Advantages of double-poly-Si RF process:

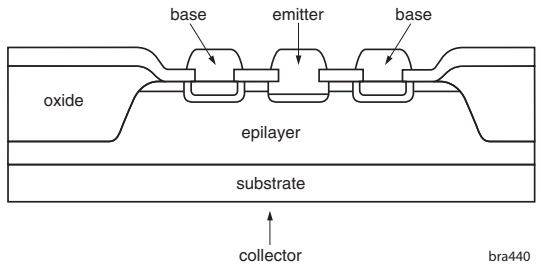
- Higher frequencies (>23GHz)
- Higher power gain G_{max}, e.g., 22dB/2GHz
- Lower noise operation
- Higher reverse isolation
- Simpler matching
- Lower current consumption
- Optimized for low supply voltages
- High efficiency
- High linearity
- Better heat dissipation
- Higher integration for MMICs (**SSI**= **S**mall-**S**cale-**I**ntegration)

Applications

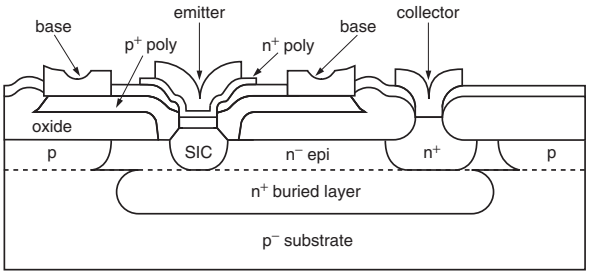
Cellular and cordless markets, low-noise amplifiers, mixers and power amplifier circuits operating at 1.8 GHz and higher), high-performance RF front-ends, pagers and satellite TV tuners.

Typical products manufactured in double-poly-Si:

- MMIC Family: BGA20xy, and BGA27xy
- 6th generation wideband transistors: BFG403W/410W/425W/480W



Existing advanced bipolar transistor



With double-poly, a polysilicon layer is used to diffuse and connect the emitter while another polysilicon layer is used to contact the base region. Via a buried layer, the collector is brought out on the top of the die. As with standard transistors, the collector is contacted via the back substrate and attached to the lead-frame.

4. RF design basics

4.1 RF fundamentals

4.1.1 RF waves

RF **electromagnetic (EM)** signals travel outward like **waves** in a pond that has had a stone dropped into it. The EM waves are governed by the laws that particularly apply to optical signals. In a homogeneous vacuum, without external influences, EM waves travel at a **speed of C_o=299792458 m/s.** Waves traveling in substrates, wires, or within a non-air dielectric material put into the traveling path slow down and their speed is proportional to the root of the dielectric constant:

$$v = \frac{C_O}{\sqrt{\varepsilon_{reff}}}$$

ε_{reff} is the **substrate's dielectric constant**.

With 'v' we can calculate the **wavelength**, as: $\lambda = \frac{v}{f}$

Example1: Calculate the speed of an electromagnetic wave in a **P**rinted **C**ircuit **B**oard (**PCB**) manufactured using a FR4 epoxy material and in a metal-dielectric-semiconductor capacitor of an integrated circuit.

Calculation: In a metal-dielectric-semiconductor capacitor, the dielectric material can be Silicon-Dioxide (SiO_2) or Silicon-Nitride (Si_3N_4).

$$v = \frac{C_O}{\sqrt{\varepsilon_{reff}}} = \frac{299792458 m/s}{\sqrt{4.6}} = 139.78 \cdot 10^6 m/s$$

FR4	➡	ε_{reff} = 4.6	➡	v = 139.8•10⁶m/s
SiO_2	➡	ε_{reff} = 2.7 to 4.2	➡	v = 182.4•10⁶m/s to 139.8•10⁶m/s
Si3N4	➡	ε_{reff} = 3.5 to 9	➡	v = 160.4•10⁶m/s to 99.9•10⁶m/s

Example2: What is the wavelength transmitted from a commercial SW radio broadcasting program (SWR3 in the 49 meter band) at 6030 kHz in air, and within a FR4 PCB?

Calculation: The ε_{reff} of air is close to vacuum. ➡ $\varepsilon_{reff} \approx 1$ ➡ $v = c_O$

Wavelength in air: $\lambda_{air} = \frac{C_O}{f} = \frac{299792458 m/s}{6030 KHz} = 49.72 m$

From Example 1 we take the FR4 dielectric constant to be ε_{reff} = 4.6, then v = 139.8•10⁶m/s and calculate the wavelength in the PCB as: λ_{FR4} = 23.18 meters

A forward-traveling wave is transmitted (or injected) by the source into the traveling medium (whether it be the ether, a **substrate**, a **dielectric**, wire, **microstrip**, **waveguide** or other medium) and travels to the load at the opposite end of the medium. At junctions between two different dielectric materials, a part of the forward-traveling wave is reflected back towards the source. The remaining part continues traveling towards the load.

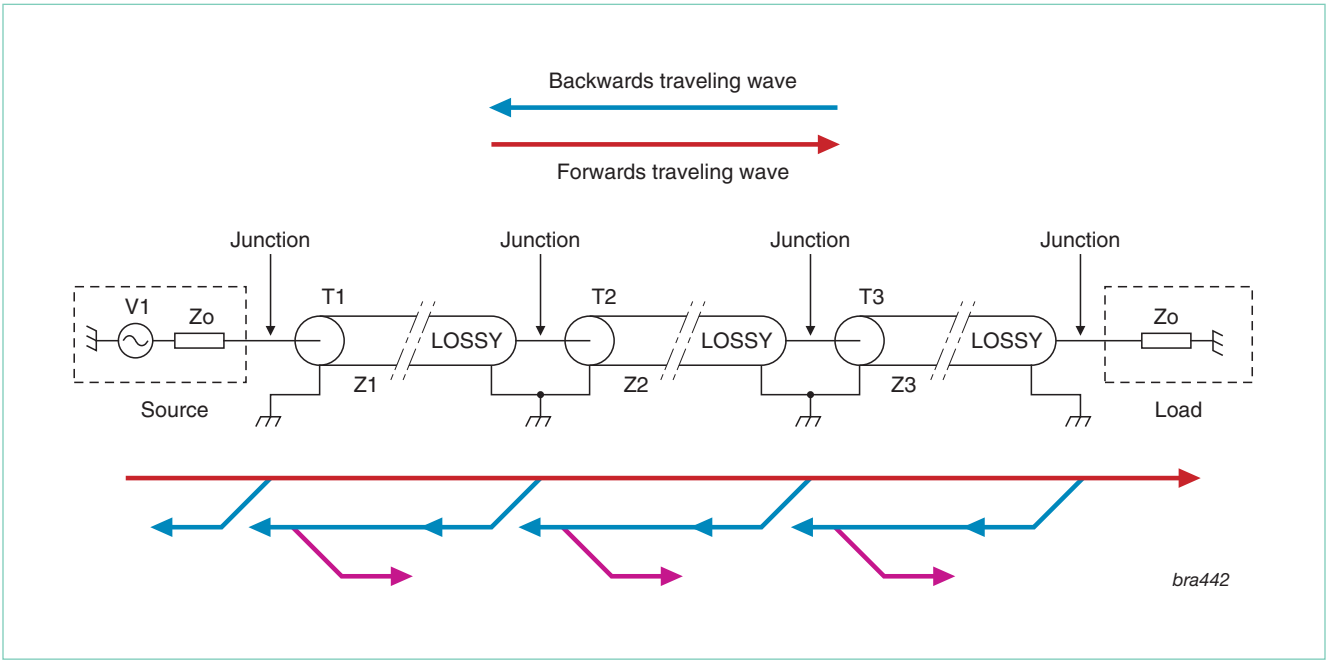
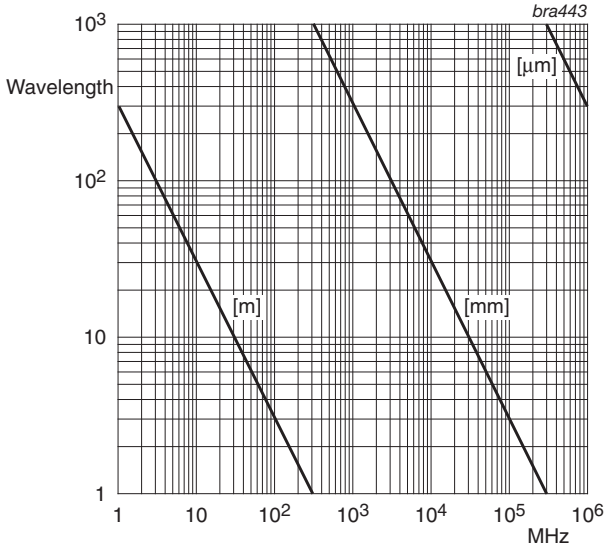


Fig.6: Multiple reflections between lines with different impedances Z1-Z3

In Fig.6, **reflections** of the forward-traveling main wave (red) are caused between materials with different impedance values (Z1, Z2, Z3). As shown, a backward-reflected wave (green) can again be reflected into a forward-traveling wave in the direction towards the load (shown as violet in Fig.6). In the case of optimum **matching** between different dielectric mediums, no signal reflection will occur and maximum power is forwarded. The amount of reflection caused by junctions of lines with different impedances, or line **discontinuities**, is determined by the **reflection coefficient**. This is explained in the next chapter.



Example: Select your frequency (ISM433) crossing a trace (blue) you can read the wavelength (70cm)

4.1.2 The reflection coefficient

As discussed previously, a forward-traveling wave is partially reflected back at junctions with line impedance discontinuities, or mismatches. Only the portion of the forward traveling wave (arriving at the load) will be absorbed and processed by the load. Because of the frequency-dependent speed of the propagating waves in a dielectric medium, there will be a delay in the arrival of the wave at the load point over what a wave traveling in free space would have (phase shift). Mathematically this behavior is modeled with a vector in the complex Gaussian space. At each location of the travel medium (or wire), wave-fronts with different amplitude and phase delay are heterodyned. The resulting energy envelope of the waves along the wire appears as a ripple with maximum and minimum values. The phase difference between maximums has the same value as the phase difference between minimums. This distance is termed the **half-wavelength, or λ/2 (also termed the normalized phase shift of 180°).**

Example: A line with mismatched ends driven from a source will have standing waves. These will result in minimum and maximum signal amplitudes at defined locations along the line. Determine the approximate distance between worst-case voltage points for a **Bluetooth** signal processed in a printed circuit on a FR4 based substrate.

Calculation: Assumed speed in FR4: $\nu = 139.8 \cdot 10^6 m/s$

Wavelength: $\lambda_{air} = \frac{v_{FR4}}{f_{BT}} = \frac{139.78 \cdot 10^6\, m/s}{2.4GHz} = 58.24mm$

➨ At the minimum we have minimum voltage, but maximum current.
➨ At the maximum we have maximum voltage, but minimum current.
➨ The distance between a minimum and a maximum voltage (or current) point is equal to Ï/4.

The reflection coefficient is defined by the ratio between the backward-traveling voltage wave and the forward-traveling voltage wave:

Reflection coefficient: $r_{(x)} = \frac{U_{b(x)}}{U_{f(x)}}$

Reflection loss or return loss: $r_{dB} = 20dB \cdot \log|r_{(x)}| = 20dB\{\log|U_{b(x)}| - \log|U_{f(x)}|\}$

The index '(x)' indicates different reflection coefficients along the line. This is caused by the distribution of the standing wave along the line. The return loss (in dB) indicates how much of the wave is reflected, compared to the forward-traveling wave.

Often the input reflection performance of a 50ø RF device is specified by the **V**oltage **S**tanding **W**ave **R**atio (**VSWR** or just **SWR**).

VSWR: $s = SWR = VSWR = \frac{U_{\max}}{U_{\min}}$ Matching factor: $m = \frac{1}{s}$

Some typical values of the VSWR:
100% mismatch caused by an open or shorted line: r = 1 and VSWR = ∞
Optimum (theoretical) matched line: r = 0 and VSWR = ∞
In all practical situations 'r' varies between 0 < r < 1 and 1 < VSWR < ∞

Calculating the reflection factor: $$r = \left| r_{(x)} \right| = \frac{SWR - 1}{SWR + 1}$$

Using some mathematical manipulation: $$r = \frac{\frac{U_{max}}{U_{min}} - 1}{\frac{U_{max}}{U_{min}} + 1}$$ results in: $$r = \frac{U_{max} - U_{min}}{U_{max} + U_{min}}$$

Reflection coefficients of certain impedances (e.g. a load) leads to: $$r = \frac{Z - Z_O}{Z + Z_O}$$

with Z_o = nominal system impedance (50Ω, 75Ω).

As explained, the standing waves cause different amplitudes of voltage and current along the wire.

The ratio of these two parameters is the impedance $$Z_{(x)} = \frac{V_{(x)}}{I_{(x)}}$$ at each location, (x). This means a line with length (L), and a mismatched load Z(x = L) at the wire-end location (x=L), will show a wire-length dependent impedance at the source location (x=0):

$$Z_{(x=0)\ f(\ell)} = \frac{V_{(x=0)}}{I_{(x=0)}}$$

Example: There are several special cases (tricks) that can be used in microwave designs.

Mathematically it can be shown that a wire with the length of $$\ell = \frac{\lambda}{4}$$ and an impedance ZL will be a **quarter wavelength transformer**:

$$\ell = \frac{\lambda}{4}$$ - impedance transformer: $$Z_{(x=\ell)} = \frac{Z_L{}^2}{Z_{(x=0)}}$$

This can be used in SPDT (single pole, double throw) based PIN diode switches or in DC bias circuits because an RF short (like a large capacitor) is transformed into infinite impedance with low resistive dc path (under ideal conditions).

As indicated in Fig.6, and shown by the RF traveling-wave basic rules, matching, reflection and individual wire performances affect bench measurement results caused by impedance transformation along the wire. Due to this constraint, each measurement set-up must be calibrated by precision references.

Examples of RF calibration references are:

- Open
- Through
- Short
- Sliding Load
- Match

The set-up calibration tools can undo unintended wire transformations, discontinuities from connectors, and similar measurement intrusion issues. This prevents **D**evice **U**nder **T**est (**DUT**) measurement parameters from being affected by mechanical bench set-up configurations.

Example: a) Determine the input VSWR of **BGA2711 MMIC** wideband amplifier for 2GHz, based on data sheet characteristics.
b) What kind of resistive impedance(s) can theoretically cause this VSWR?
c) What is the input return loss measured on a 50Ω coaxial cable in a distance of λ/4?

Calculation: **BGA2711** at 2 GHz: r_{IN} = 10dB

$$r = \frac{SWR-1}{SWR+1} \quad \Rightarrow \quad r \cdot SWR + r = SWR - 1 \quad \Rightarrow \quad SWR = \frac{1+r}{1-r}$$

$$r = 10^{\frac{-r_{dB}}{20dB}} = 10^{\frac{-10dB}{20dB}} = 0.3162 \quad \Rightarrow \quad SWR_{IN} = \frac{1+0.3162}{1-0.3162} = 1.92 \quad r = \frac{Z-Z_O}{Z+Z_O} \quad \Rightarrow$$

$$Z - r \cdot Z = r \cdot Z_O + Z_O \quad \Rightarrow \quad Z = Z_O \frac{1+r}{1-r}$$

Comparison: $Z = Z_O \frac{1+r}{1-r}$ & $SWR = \frac{1+r}{1-r}$ ➡ $Z = Z_O \cdot SWR$

We know only the magnitude of (r) but not it's angle. By definition, the VSWR must be larger than 1.
We then get two possible solutions:

$SWR_1 = \frac{Z_{\max}}{Z_O}$ and $SWR_2 = \frac{Z_O}{Z_{\min}}$ Z_{max}=1.92*50Ω=96.25Ω; Z_{min}=50Ω/1.92=25.97Ω

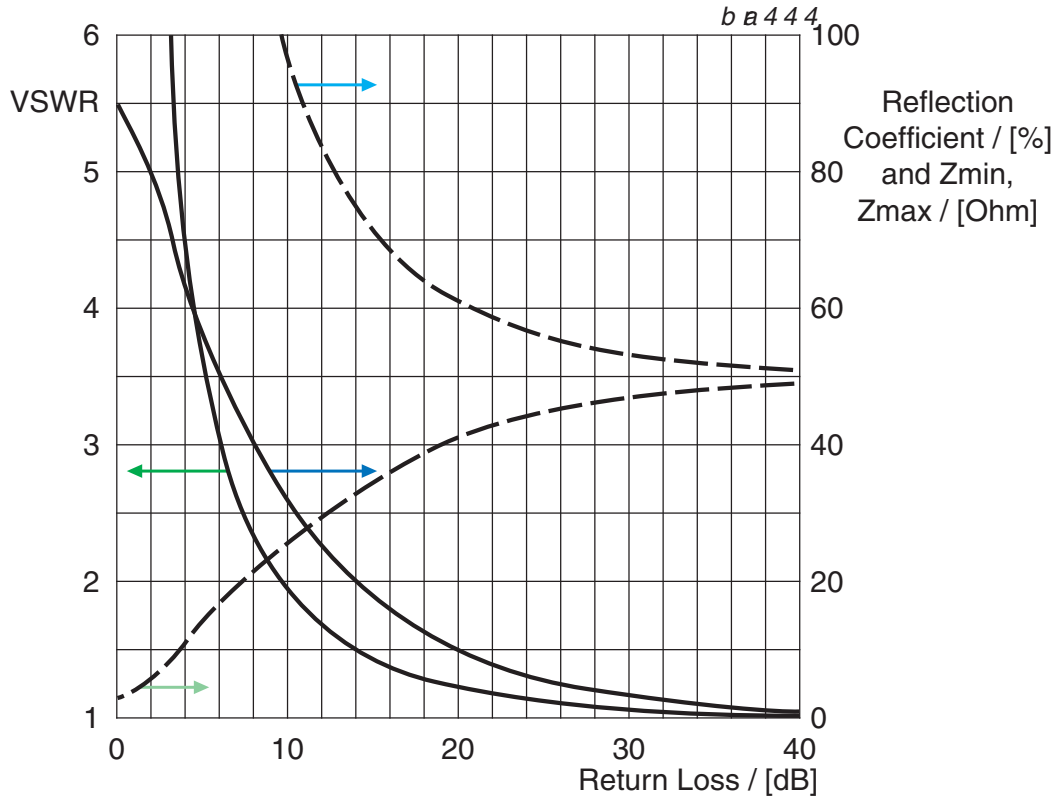
We can then examine r: $|r| = \left|\frac{96.25-50}{96.25+50}\right| = \left|\frac{25.96-50}{25.96+50}\right| = 0.316$

The λ/4 transformer transforms the device impedance to:

Z_{IN1}=96.25Ω ➡ $Z_{Ende} = \frac{Z_O^{\,2}}{Z_{IN}} = \frac{50\Omega^2}{96.25\Omega} = 25.97\Omega$ and for Z_{IN2}=25.97Ω ➡ 96.25Ω

Results: At 2GHz, the **BGA2711** offers an input return loss of 10dB or VSWR=1.92. This reflection can be caused by a 96.25Ω or a 25.97Ω impedance. Of course there are infinite results possible if one takes into account all combinations of L and C values.
Measuring this impedance at 2GHz with the use of a non-50Ω cable will cause extremely large errors in λ/4 distance, because the Zin1 = 96.25Ω appears as 25.97Ω and the second solution Zin_2=25.97Ω appears as 96.25Ω!

As illustrated in the above example, the VSWR (or return loss) quickly indicates the quality of a device's input matching without any calculations, but does not tell about its real (vector) performance (missing or phase information). Detailed mathematical network analysis of RF amplifiers depends on the device's input impedance versus output load (S12 issue). The output device impedance is dependent on the impedance of the source driving the amplifier (S21 issue). Due to this interdependence, the use of s-parameters in linear small signal networks offers reliable and accurate results. This s-parameter theory will be presented in the next chapters.



Example: Select your interesting return-loss (10dB). Crossing the dark green trace you can find the VSWR (≈1,9) and crossing the dark blue trace you can find the reflection coefficient (r≈0,32). There are two (100% resistive) mismatches found either crossing the dashed light green traces (Z_{max}≈96Ω) or crossing the dashed light blue trace (Z_{min}≈26Ω). For further details, please refer to the former algebraic application example.

4.1.3 Differences between ideal and practical passive devices

Practical devices have so-called parasitic elements at very high frequencies.

Resistor	Has an inductive parasitic action and acts like a low-pass filtering function.
Inductor	Has a capacitive and resistive parasitic, causing it to act like a damped parallel resonant tank circuit with a certain self resonance.
Capacitor	Has an inductive and resistive parasitic, causing it to act like a damped tank circuit with **S**eries **R**esonance **F**requency (**SRF**).

The inductor's and the capacitor's parasitic reactance causes self-resonances.

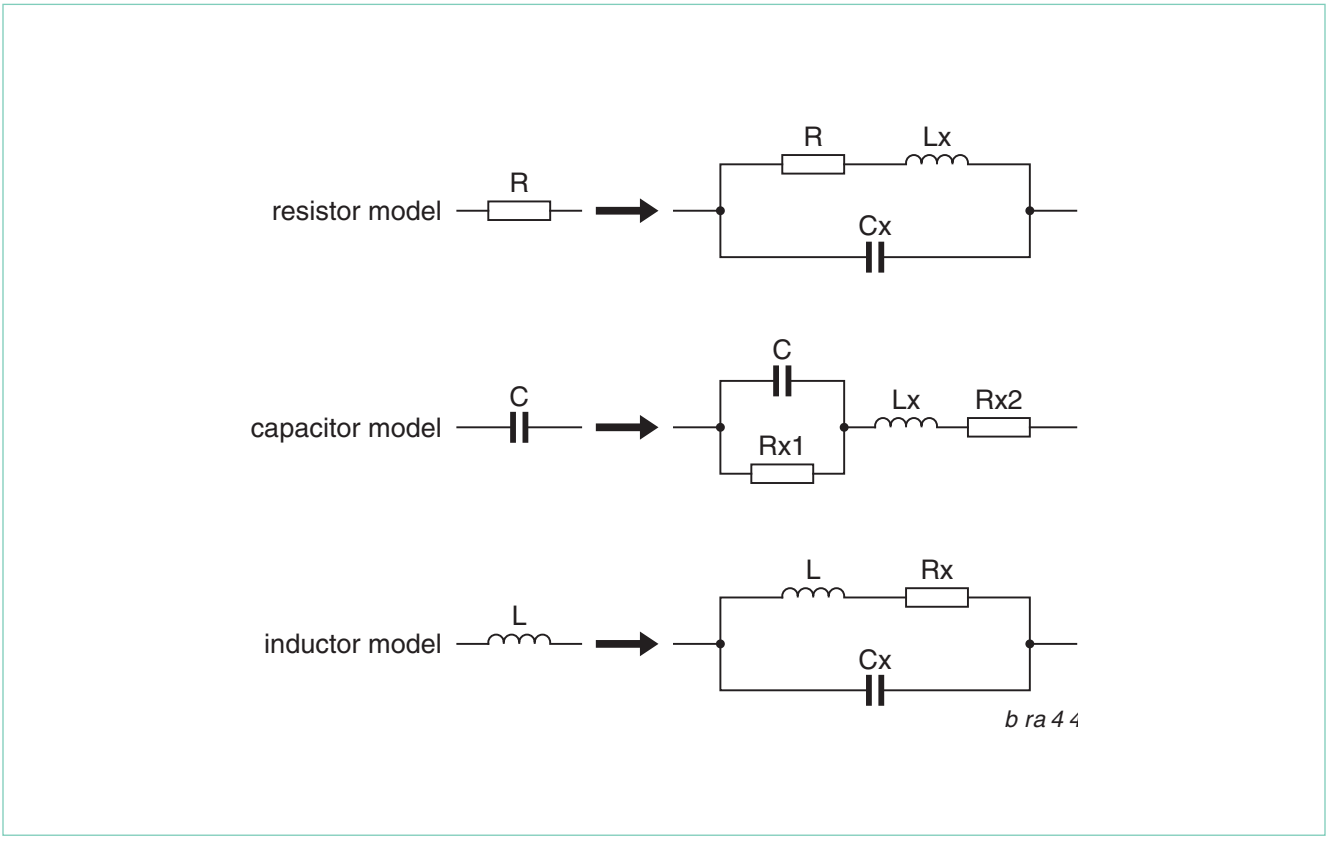


Fig.7 Equivalent models of passive lumped elements

The use of a passive component above its SRF is possible, but must be critically evaluated. A capacitor above its SRF appears as an inductor with DC blocking capabilities.

4.1.4 The Smith chart

As indicated in an example in the previous chapter, the impedances of semiconductors are a combination of resistive and reactive parts caused by phase delays and parasitics. RF impedances are best analyzed in the frequency domain under the use of vector algebraic expressions:

Object	➡	into	➡	Frequency domain
Resistor	➡	R	➡	$R = \lvert R \rvert \cdot e^{+j0^\circ}$
Inductor	➡	L	➡	$X_L = +j\omega \cdot L = \omega \cdot L \cdot e^{+j90^\circ}$
Capacitor	➡	C	➡	$X_C = -j\frac{1}{\omega \cdot C} = \frac{1}{\omega \cdot C} \cdot e^{-j90^\circ}$
Frequency	➡	f	➡	$\omega = 2\pi \cdot f$
Complex designator	➡	j	➡	$+j = \sqrt{-1} = \frac{1}{-j} = e^{+j90^\circ}$

Some useful basic vector algebra in RF analysis:

Complex impedance:

$$Z = \mathrm{Re}\{Z\} + j\,\mathrm{Im}\{Z\} = \lvert Z \rvert \cdot e^{j\varphi} = \lvert Z \rvert \cdot (\cos\varphi - j\sin\varphi)$$

$$\mathrm{Im}\{Z\} = \lvert Z \rvert \sin\varphi \; ; \; \mathrm{Re}\{Z\} = \lvert Z \rvert \cos\varphi \; ;$$

$$\tan = \frac{\sin\varphi}{\cos\varphi} \quad \Rightarrow \quad \tan\varphi = \frac{\mathrm{Im}\{Z\}}{\mathrm{Re}\{Z\}} \quad \text{with;} \quad \varphi = \omega \cdot t$$

Use of angle ➡ **Polar** notation
Use of sum ➡ **Cartesian (Rectangular)** notation

The same rules are used for other issues,

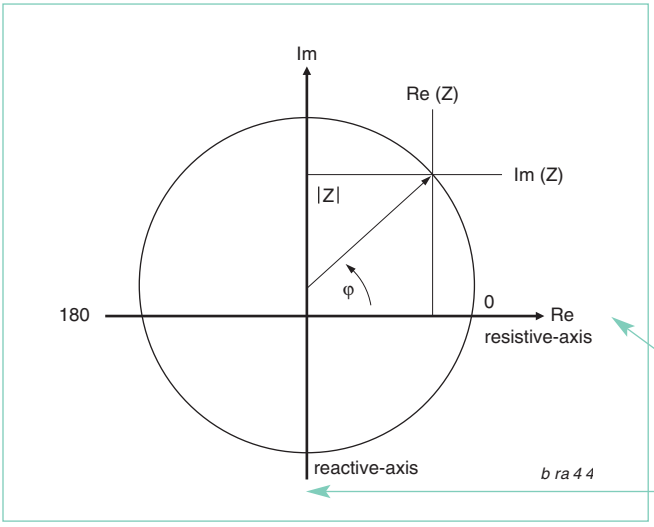
e.g., the **complex reflection coefficient:**

$$r = \lvert r \rvert \cdot e^{j\varphi} = \frac{\lvert U_b \rvert \cdot e^{j\varphi_b}}{\lvert U_f \rvert \cdot e^{j\varphi_f}} = \left\lvert \frac{U_b}{U_f} \right\rvert \cdot e^{j(\varphi_b - \varphi_f)}$$

Special cases:

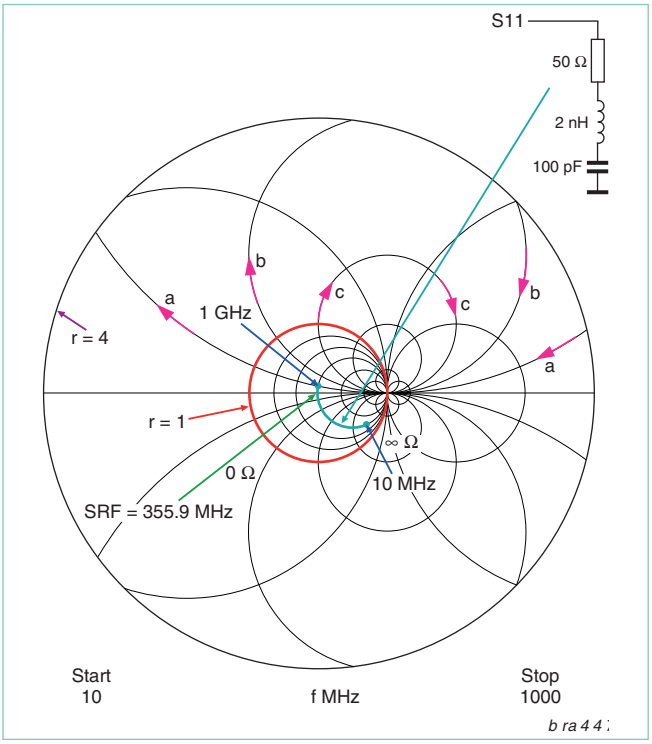
- Resistive mismatch: $\varphi_{(R)} = 0°$ reflection coefficient: $\varphi_{(r)} = 0°$
- Inductive mismatch: $\varphi_{(L)} = +90°$ reflection coefficient: $\varphi_{(r)} = +90°$
- Capacitive mismatch: $\varphi_{(C)} = -90°$ reflection coefficient: $\varphi_{(r)} = -90°$

The **Gaussian number area (Polar Diagram)** allows charting rectangular two-dimensional vectors:



Dots on the Re-Line are 100% resistive
Dots on the Im-Line are 100% reactive
Dots some their above the Re-Line are inductive + resistive
Dots some their below the Re-Line are capacity + resistive

In applications, RF designers try to remain close to a 50 Ω resistive impedance. The polar diagram's origin is 0 Ω. In RF circuits, relatively large impedances can occur but we try to remain close to 50 Ω by special network design for maximum power transfer. Practically, very low and very high impedances don't need to be known accurately. The Polar diagram can't show simultaneous large impedances and the 50 Ω region with acceptable accuracy, because of limited paper size.



Using this fact Mr. Phillip Smith, an engineer at Bell Laboratories, developed the so-called **Smith Chart** in the 1930s. The chart's origin is at 50Ω. Left and right resistive values along the real axis end in 0Ω and at ?Ω. The imaginary reactive axis (imaginary axis, or Im-Axis) ends in 100% reactive (L or C). High resolution is provided close to the 50Ω origin. Far away of the chart's centre the resolution drops. Further from the centre of the chart, the resolution / error increases. The standard Smith Chart only displays **positive resistances** and has a unit radius (r=1). **Negative resistances** generated by **instability** (e.g. **oscillation**) lie outside the unit circle. In this non-linear scaled diagram, the infinite dot of the Re-Axis is 'theoretically' bent to the zero point of the Smith Chart. Mathematically it can be shown that this will form the Smith Chart's unit circle (r=1). All dots lying on this circle represent a reflection coefficient magnitude of 1 (100% mismatch). Any positive L/C combination with a resistor will be mathematically represented by its polar notation reflection coefficient inside the Smith Chart's unity circle. Because the Smith Chart is a transformed linear-scale polar diagram, we can use 100% of the polar diagram rules. Cartesian-diagram rules are changed due to non-linear scaling.

Special cases:

- Dots below the horizontal axis represent impedance with a capacitive part (180° < φ < 360°)
- Dots laying on the horizontal axis (ordinate) are 100% resistive (φ = 0°)
- Dots laying on the vertical axis (abscissa) are 100% reactive (φ = 90°)

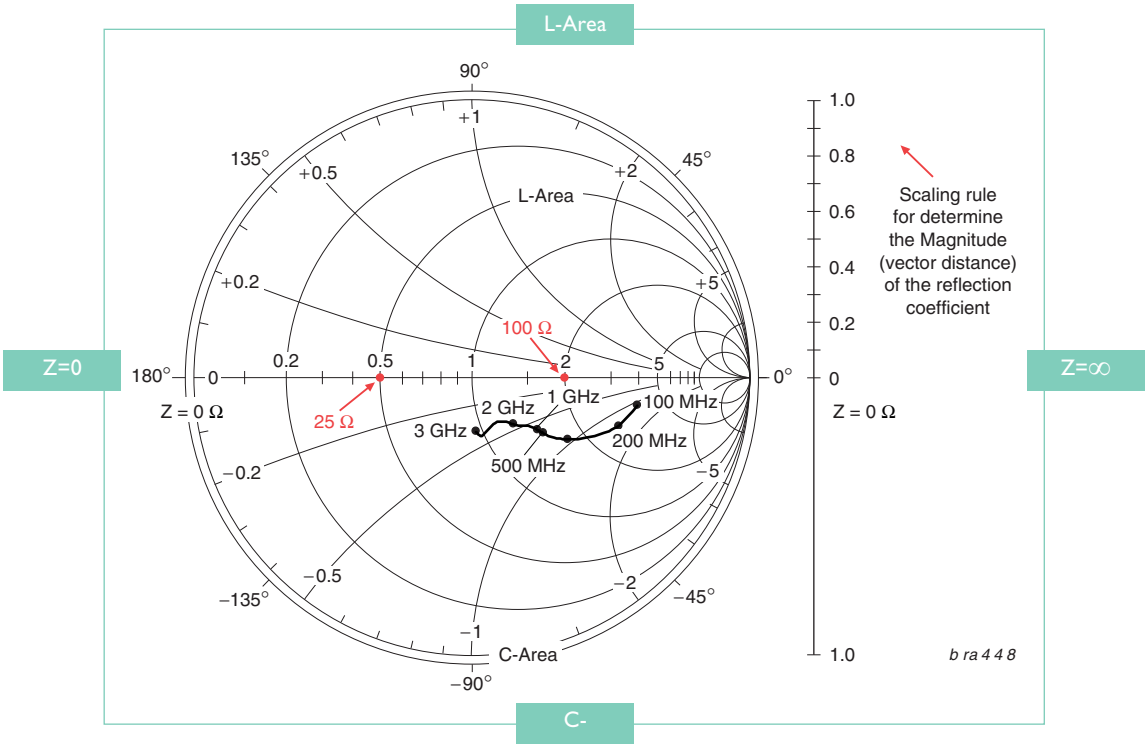


Fig.8: BGA2003 output Smith chart (S_{22})

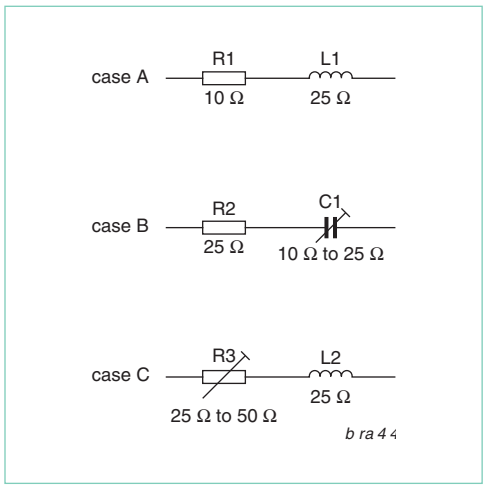
The special cases for zero and infinitely large impedance are illustrated (above). The upper half circle is the inductive region. The lower half of the circle is the capacitive region. The origin is the 50Ω system reference (Z_O). To be more flexible, numbers printed in the chart are normalized to Z_O.

Normalizing impedance procedure: $Z_{norm} = \frac{Z_x}{Z_o}$ Z_O = System reference impedance (e.g., 50Ω, 75Ω)

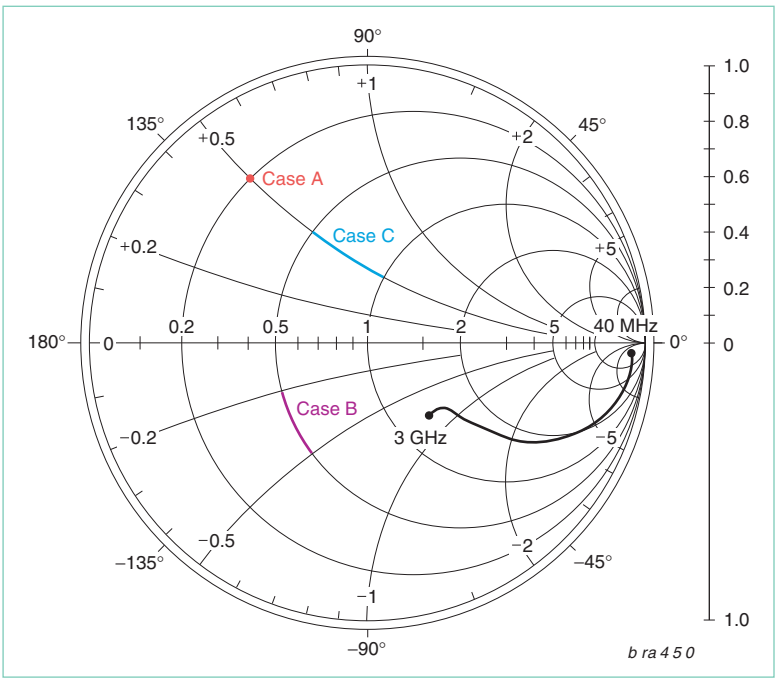
Example: Plot a 100Ω & 50Ω resistor into the upper **BGA2003's** output Smith chart.
Calculation: Z_{norm1}=100Ω/50Ω=2; Z_{norm2}=25Ω/50Ω=0.5
Result: The 100Ω resistor appears as a dot on the horizontal axis at the location 2.
The 25Ω resistor appears as a dot on the horizontal axis at the location 0.5

Example1: In the following three circuits, capacitors and inductors are specified by the amount of reactance @ their 100MHz design frequency. Determine the value of the parts. Plot their impedance in to the **BFG425W's** output (S22) Smith chart.

Circuit:



Result:



Calculation: **Case A** (constant resistance)

From the circuit ➡ $Z_A = 10\Omega + j25\Omega$;

$$L_1 = \frac{25\Omega}{2\pi \cdot 100MHz} = 39.8nH$$

$Z_{(A)norm}$ = ZA/50Ω = 0.2 + j0.5 ➡ Drawing into Smith chart

Basics:

$$C = \frac{1}{\omega \cdot X_C}$$

$$L = \frac{X_L}{\omega}$$

$$\omega = 2\pi \cdot f$$

Case B (constant resistance and variable reactance - variable capacitor)

From the circuit ➡ $Z_B = 10\Omega + j(10 \text{ to } 25)\Omega$

$$C_B = \frac{1}{2\pi \cdot 100MHz \cdot (10 \text{ to } 25)\Omega} = 63.7\text{pF to } 159.2\text{pF}$$

$Z_{(B)norm}$=ZB/50Ω=0.5-j(0.2 to 0.5) ➡ Drawing into Smith chart

Case C (constant resistance and variable reactance - variable inductor)

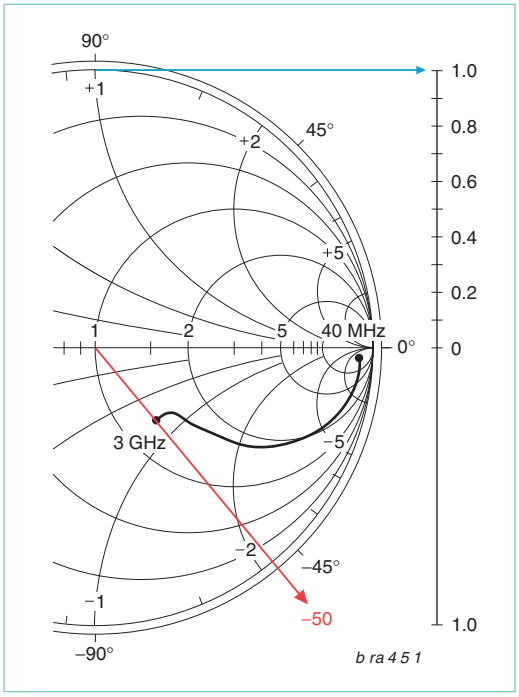
From the circuit ➡ $Z_C = (25\Omega \text{ to } 50\Omega) + j25\Omega$

$$L_C = \frac{(25 \text{ to } 50)\Omega}{2\pi \cdot 100MHz} = 39.8\text{nH to } 79.6\text{nH}$$

$Z_{(C)norm}$=ZC/50Ω=(0.5 to 1)+j0.5 ➡ Drawing into Smith chart

Example2: Determine **BFG425W's** outputs reflection coefficient (S22) at 3GHz from the data sheet. Determine the output return loss and output impedance. Compensate the reactive part of the impedance.

Calculation: The data in the Smith chart can be read with improved resolution by using the vector reflection coefficient in Polar notation.



Procedure: 1) Mechanically measure the scalar length from the chart origin to the 3GHz (vector distance).
2) On the chart's right side is printed a ruler with the numbers of 0 to 1. Read from it the equivalent scaled scalar length |r| = 0.34

3) Measure the angle ∠(r) = φ = -50°. Write the reflection coefficient in vector polar notation

$$r = 0.34e^{-j50^\circ}$$

Normalized impedance: $\frac{Z}{Z_O} = \frac{1+r}{1-r} = 1.513e^{-j30.5^\circ}$

Because the transistor was characterized in a 50Ω bench test set-up ➨ $Z_o = 50\Omega$

Impedance: $Z_{22} = 75.64\Omega e^{-j30.5^\circ} = (65.2 - j38.4)\Omega$

$$C = \frac{1}{2\pi \cdot 3GHz \cdot 38.4\Omega} = 1.38\,pF$$

The output of **BFG425W** has an equivalent circuit of 65.2Ω with 1.38pF series capacitance. Output return loss, not compensated: RL_{OUT}= -20log(|r|)=9.36dB resulting in $VSWR_{OUT}$=2

For compensation of the reactive part of the impedance, we take the **conjugate complex** of the reactance:
Xcon=-Im{Z} = -{-j38.4Ω} = +j38.4Ω resulting in

$$L = \frac{38.4\Omega}{2\pi \cdot 3GHz} = 2nH$$

A 2nH series inductor will compensate the capacitive reactance. The new input reflection coefficient is calculated to:

$$r = \frac{65.2\Omega - 50\Omega}{65.2\Omega + 50\Omega} = 0.132$$

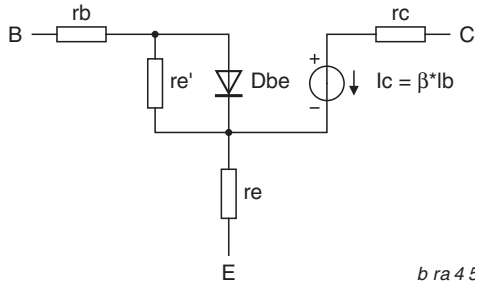
Output return loss, compensated: RL_{OUT}= -20log(0.132)=17.6dB resulting in $VSWR_{OUT}$=1.3

Please note: In practical situations the output impedance is a function of the input circuit. The input and output matching circuits are defined by the **stability** requirements, the need gain and noise-matching. Investigation is done by using network analysis based on **s-parameters**.

4.2 Small signal RF amplifier parameters

4.2.1 Transistor parameters, DC to microwave

At low DC currents and voltages, one can assume a transistor acts like a voltage-controlled current source with diode clamping action in the base-emitter input circuit. In this model, the transistor is specified by its large-signal DC-parameters, i.e., DC-current gain (B, ß, h_{fe}), maximum power dissipation, breakdown voltages and so forth.



$$I_C = I_{CO} \cdot e^{\frac{U_{BE}}{V_T}} \qquad r_e' = \frac{V_T}{I_E}$$

Thermal Voltage: VT=kT/q≈26mV@25°C

I_{CO} = Collector reverse saturation current

Low frequency voltage gain $V_u \approx \frac{R_C}{r_e'}$

Current gain $\beta = \frac{I_C}{I_B}$

Increasing the frequency to the audio frequency range, the transistor's parameters change due to frequency-dependent phase shift and parasitic capacitance effects. For characterization of these effects, small signal **h-parameters** are used. These hybrid parameters are determined by measuring voltage and current at one terminal and using open or short (standards) at the other port. The **h-parameter** matrix is shown below.

h-parameter Matrix:

$$\begin{pmatrix} u_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} * \begin{pmatrix} i_1 \\ u_2 \end{pmatrix}$$

Increasing the frequency to the HF and VHF ranges, open ports become inaccurate due to electrically stray field radiation. This results in unacceptable errors. Due to this phenomenon, **y-parameters** were developed. They again measure voltage and current, but use only a 'short' standard. This 'short' approach yields more accurate results in this frequency region. The **y-parameter** matrix is shown below.

y-parameter Matrix:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} * \begin{pmatrix} u_1 \\ u_2 \end{pmatrix}$$

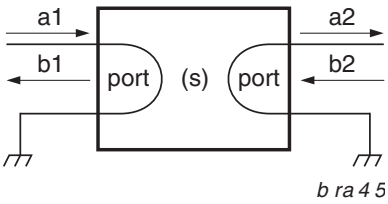
Further increasing the frequency, the parasitic inductance of a 'short' causes problems due to mechanical-dependent parasitics. Additionally, measuring voltage, current and phase is quite tricky. The scattering parameters, or **s-parameters**, were developed based on the measurement of the forward and backward traveling waves to determine the reflection coefficients on a transistor's terminals (or ports). The **s-parameter** matrix is shown below.

s-parameter Matrix:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} * \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

4.2.2 Definition of the s-parameters

Every amplifier has an input port and an output port (a 2-port network). Typically the input port is labeled Port-1 and the output is labeled Port-2.



Matrix:
$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} * \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

Equation:
$$b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2$$
$$b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2$$

Fig.10: Two-port network's (a) and (b) waves

The forward-traveling waves (a) are traveling into the DUT's (input or output) ports.
The backward-traveling waves (b) are reflected back from the DUT's ports
The expression 'port ZO terminate' means the use of a 50ø-standard.
This is not a conjugate complex power match! In the previous chapter the reflection coefficient was defined as:

Reflection coefficient: $r = \dfrac{back\ running\ wave}{forward\ running\ wave}$

Calculating **the input reflection factor** on port 1: $S_{11} = \left.\dfrac{b_1}{a_1}\right|_{a_2=0}$ with the output terminated in Z_O.

That means the source injects a forward-traveling wave (a1) into Port-1. No forward-traveling power (a2) injected into Port-2. The same procedure can be done at Port-2 with the

Output reflection factor: $S_{22} = \left.\dfrac{b_2}{a_2}\right|_{a_1=0}$ with the input terminated in Z_O.

Gain is defined by: $gain = \dfrac{output\ wave}{input\ wave}$

The **forward-traveling wave** gain is calculated by the wave (b2) traveling out of Port-2 divided by the wave (a1) injected into Port-1.

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$$

The **backward traveling wave** gain is calculated by the wave (b1) traveling out of Port-1 divided by the wave (a2) injected into Port-2.

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

The normalized waves (a) and (b) are defined as:

$a_1 = \dfrac{1}{2\sqrt{Z_O}}(V_1 + Z_O \cdot i_1)$ = signal into Port-1

$a_2 = \dfrac{1}{2\sqrt{Z_O}}(V_2 + Z_O \cdot i_2)$ = signal into Port-2

$b_1 = \dfrac{1}{2\sqrt{Z_O}}(V_1 + Z_O \cdot i_1)$ = signal out of Port-1

$b_2 = \dfrac{1}{2\sqrt{Z_O}}(V_1 + Z_O \cdot i_2)$ = signal out of Port-2

Forward transmission:
$FT = 20\log(S_{21})dB$

Isolation:
$S12(dB) = -20\log(S_{12})dB$

Input return loss:
$RL_{in} = -20\log(S_{11})dB$

Output return loss:
$RL_{OUT} = -20\log(S_{22})dB$

Insertion loss:
$IL = -20\log(S_{21})dB$

The normalized waves have units of $\sqrt{Watt}$ and are referenced to the system impedance Z_O, shown by the following mathematical analyses: The relationship between U, P an Z_O can be written as:

$$\frac{u}{\sqrt{Z_O}} = \sqrt{P} = i \cdot \sqrt{Z_O} \qquad \text{Substituting:} \quad \frac{Z_0}{\sqrt{Z_O}} = \sqrt{Z_O}$$

$$a_1 = \frac{V_1}{2\sqrt{Z_O}} + \frac{Z_O \cdot i_1}{2\sqrt{Z_O}} = \frac{\sqrt{P_1}}{2} + \frac{Z_O \cdot i_1}{2\sqrt{Z_O}}$$

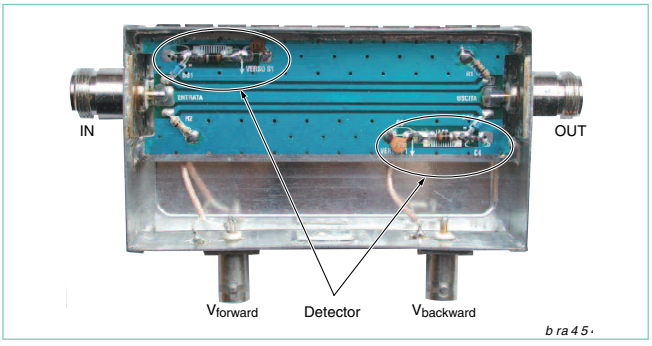
$$a_1 = \frac{\sqrt{P_1}}{2} + \frac{\sqrt{Z_O \cdot i_1}}{2} = \frac{\sqrt{P_1}}{2} + \frac{\sqrt{P_1}}{2} \text{ Ë } \quad a_1 = \sqrt{P_1} \text{ (Ë Unit } = \sqrt{Watt} = \frac{Volt}{\sqrt{Ohm}})$$

Rem:

$$\frac{Z_O}{\sqrt{Z_O}} = \frac{Z_O \cdot \sqrt{Z_O}}{\sqrt{Z_O} \cdot \sqrt{Z_O}} = \frac{Z_O \cdot \sqrt{Z_O}}{Z_O} = \sqrt{Z_O}$$

$$P = U \cdot I = \frac{U^2}{R} \rightarrow \sqrt{P} = \frac{U}{\sqrt{R}} = I \cdot \sqrt{R}$$

Because $a_1 = \frac{V_{forward}}{\sqrt{Z_O}}$, the normalized waves can be determined by the measuring the voltage of a forward-traveling wave referenced to the system impedance constant $\sqrt{Z_O}$. Directional couplers or VSWR bridges can divide the standing waves into the forward- and backward-traveling voltage wave. (Diode) Detectors convert these waves to the $V_{forward}$ and $V_{backward}$ DC voltage. After easy processing of both DC voltages, the VSWR can be read.



A 50Ω VHF-SWR-meter built from a kit (Nuova Elettronica). It consists of three strip-lines. The middle line passes the main signal from the input to the output. The upper and lower strip-lines select a part of the forward and backward traveling waves by special electrical and magnetic cross-coupling. Diode detectors at each coupled strip-line-end rectify the power to a DC voltage, which is passed to an external analog circuit for processing and monitoring of the VSWR. Applications include: power antenna match control, PA output power detector, vector voltmeter, vector network analysis, AGC, etc. These kinds of circuit kits are discussed in amateur radio literature and in several RF magazines.

4.2.2.1 2-Port Network definition

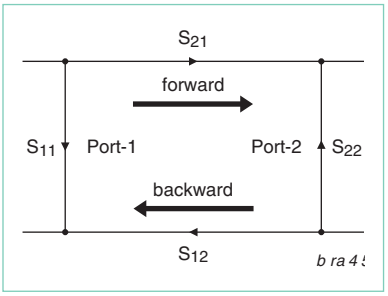


Fig.11: S-parameters in the two-port network

Philips' data sheet parameter **Insertion power gain**

$|S_{21}|^2$: $10dB \cdot \log|S_{21}|^2 = 20dB \cdot \log|S_{21}|$

Input return loss

$$S_{11} = \sqrt{\frac{\text{Power reflected from input port}}{\text{Power available from generator at input port}}}$$

Output return loss

$$S_{22} = \sqrt{\frac{\text{Power reflected from output port}}{\text{Power available from generator at output port}}}$$

Forward transmission loss (insertion loss)

$$S_{21} = \sqrt{\text{Transducer power gain}}$$

Reverse transmission loss (isolation)

$$S_{12} = \sqrt{\text{Reverse transducer power gain}}$$

Example: Calculate the insertion power gain for the **BGA2003** at 100MHz, 450MHz, 1800MHz, and 2400MHz for the bias set-up $V_{VS\text{-}OUT}$=2.5V, $I_{VS\text{-}OUT}$=10mA.

Calculation: Download the s-parameter data file [2_510A3.S2P] from the Philips website page for the Silicon MMIC amplifier **BGA2003**.

This is a section of the file:

MHz S MA R 50

! Freq	S11		S21		S12		S22 :	
100	0.58765	-9.43	21.85015	163.96	0.00555	83.961	0.9525	-7.204
400	0.43912	-28.73	16.09626	130.48	0.019843	79.704	0.80026	-22.43
500	0.39966	-32.38	14.27094	123.44	0.023928	79.598	0.75616	-25.24
1800	0.21647	-47.97	4.96451	85.877	0.07832	82.488	0.52249	-46.31
2400	0.18255	-69.08	3.89514	76.801	0.11188	80.224	0.48091	-64

Results:

100MHz ➨ 20?log(21.85015) = 26.8 dB

450MHz ➨ $20dB\log\left|\frac{16.09626e^{130.48^\circ}+14.27094e^{123.44^\circ}}{2}\right| = 23.6dB$

1800MHz ➨ 20?log(4.96451) = 13.9 dB

2400MHz ➨ 20?log(3.89514) = 11.8 dB

4.2.2.2 3-Port Network definition

Typical products for 3-port s-parameters are: directional couplers, power splitters, combiners, and phase splitters.

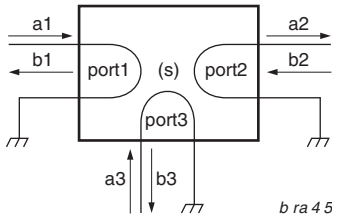


Fig.12: Three-port networks (a) and (b) waves

3-Port s-parameter definition:

• Port reflection coefficient / return loss:

Port 1 ➨ $S_{11}=\frac{b_1}{a_1}|_{(a_2=0;a_3=0)}$

Port 2 ➨ $S_{22}=\frac{b_2}{a_2}|_{(a_1=0;a_3=0)}$

Port 3 ➨ $S_{33}=\frac{b_3}{a_3}|_{(a_1=0;a_2=0)}$

• Transmission gain:

Port 1=>2 ➨ $S_{21}=\frac{b_2}{a_1}|_{(a_3=0)}$

Port 1=>3 ➨ $S_{31}=\frac{b_3}{a_1}|_{(a_2=0)}$

Port 2=>3 ➨ $S_{32}=\frac{b_3}{a_2}|_{(a_1=0)}$

Port 2=>1 ➨ $S_{12}=\frac{b_1}{a_2}|_{(a_3=0)}$

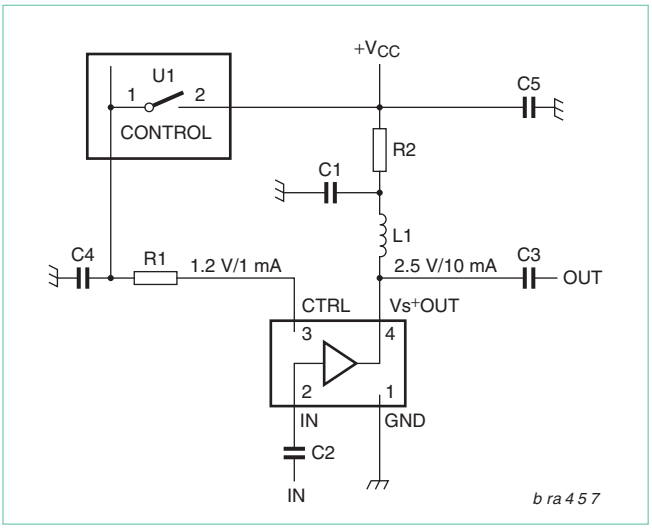
Port 3=>1 ➨ $S_{31}=\frac{b_1}{a_3}|_{(a_2=0)}$

Port 3=>2 ➨ $S_{23}=\frac{b_3}{a_2}|_{(a_1=0)}$

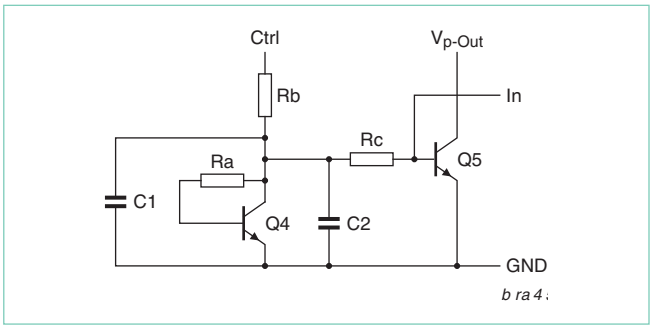
4.3 RF amplifier design fundamentals

4.3.1 DC bias point adjustment for MMICs

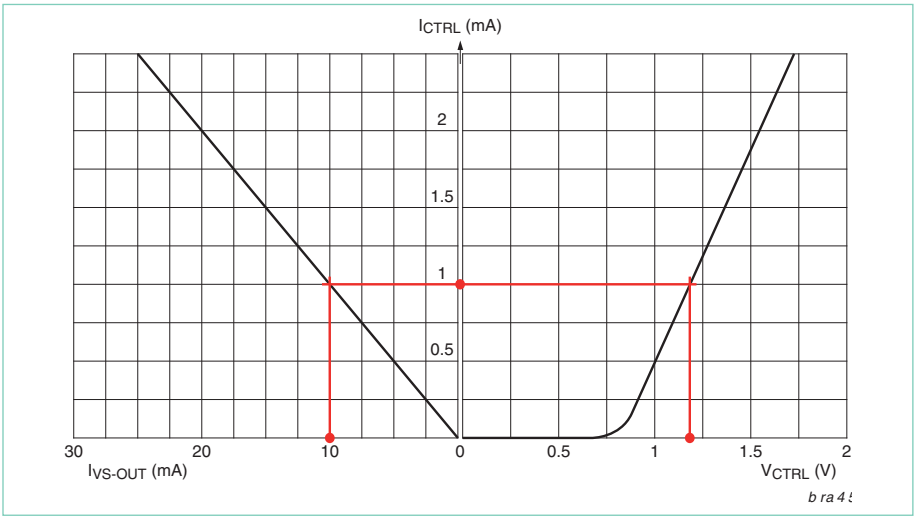
S-parameters are dependent on the bias point and the frequency, as shown in the previous chapter. Consequently, s-parameter files do include the DC bias-setting data. It's recommended to use this setup because the s-parameter will not be valid for a different bias point. An example of DC bias-circuit design is illustrated with the **BGU2003** for Vs=2.5V; Is=10mA. The supply voltage is chosen to be VCC=3V.



LNA DC bias setup



BGA2003 equivalent circuit: Q5 is the main RF transistor. Q4 forms a current mirror with Q5. The input current of this current mirror is determined by the current into Ctrl.pin. Rb limits the current when a control voltage is applied directly to the Ctrl input. RC, C1, and C2 decouple the bias circuit from the RF input signal. Because Q4 and Q5 are located on the same die, Q5's bias point is very temperature-stable.



DC bias point adjustment for transistors

From the **BGA2003** datasheet, Figs 4 and 5 were combined (see adjacent graph) to better illustrate the MMIC's I/O DC relationship.

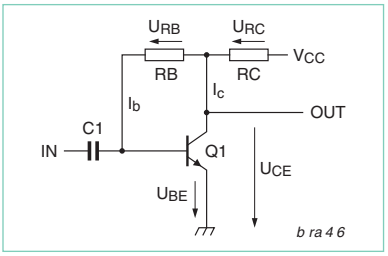
The red line shows the graphical construction starting with the requirement of I_{VS-OUT}=10mA, automatically crossing the ordinate ICTRL=1mA, and finishing into the abscissa at V_{CTRL}=1.2V

$$R_2 = \frac{V_{cc} - V_S}{I_{VS-OUT}} = \frac{3V - 2.5V}{10mA} = 50\Omega$$

$$R_1 = \frac{V_{cc} - V_{CTRL}}{I_{VS-OUT}} = \frac{3V - 1.2V}{1mA} = 1.8\text{k}\Omega$$

4.3.2 DC bias point adjustment for transistors

In contrast to the easy bias setup for MMICs, here is the design of a setup used, for example, in audio or IF amplifiers.



$$h_{FE} = \beta = B = \frac{I_C}{I_b} \qquad R_C = \frac{V_{CC} - U_{CE}}{I_b + I_C} = \frac{V_{CC} - U_{CE}}{I_C\left(\frac{h_{FE}+1}{h_{FE}}\right)}$$

$$R_C = \frac{V_{CC} - U_{CE}}{I_C(h_{FE}+1)} \cdot h_{FE} \quad ; V_{CC} - I_C \cdot R_C = V_{CE} = I_b \cdot R_B + U_{BE}$$

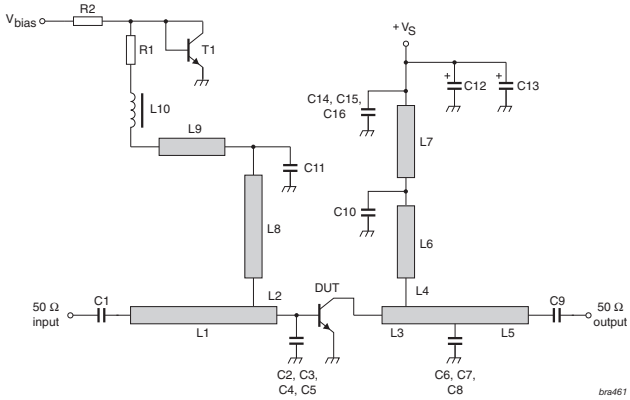
$$R_B = h_{FE} \cdot \left(\frac{V_{CC} - U_{BE}}{I_C} - R_C\right) = h_{FE} \cdot \frac{V_{CE} - V_{BE}}{I_C}$$

DC bias setup with stabilization via voltage feedback

The advantage of this setup is a very highly resistive, resistor RB. Its lowering of the input impedance at terminal [IN] can be negated, and the IF-band filter is less loaded. Because there is no emitter feedback resistor, high gain is achieved from Q1. This is needed for narrow bandwidth, high-gain IF amplifiers. The disadvantage is a very low stability of the operating point caused by the Si BE-diodes' relatively linear negative

temperature coefficient of ca.VBE≈ -2.5mV/K into amplified $I_C = \frac{V_C - V_{BE}}{R_B} \cdot h_{FE}$

This can be lowered by adding an extra resistor between ground and the emitter.



An emitter resistor has the disadvantage of gain loss or the need for a bypassing capacitor. Additionally, the transistor will loose quality in its gnd performance (instability) and will have an emitter heat sinking into the gnd plane. At medium output power, the bias setup must be stabilized due to the increased junction temperature causing DC drifting. Without stabilization the transistor will burn out or distortion can rise. A possible solution is illustrated in the adjacent picture **(BFG10)**. Comparable to the **BGA2003**, a current mirror is designed together with the DC transistor T1. T1 works like a diode with a V_{CE} (V_{BE}) drift close to the RF transistor (DUT) in the case of close thermal coupling. With ,$\beta_1=\beta_{DUT}$ and $V_{BE\text{-}1}\approx V_{BE\text{-}DUT}$ we can do a very simplified algebraic analysis:

$$V_T \cdot \ell n\left(\frac{I_{C-1}}{I_{CO}}\right) \approx V_T \cdot \ell n\left(\frac{I_{C-DUT}}{I_{CO}}\right)$$

finalizing into a very temperature-independent relation ship of $I_{C\text{-}DUT} \approx I_{C1} \approx (V_{bias}\text{-}V_{BE})/R_2$ For best current imaging, the BE die structure areas should have similar dimensions.

4.3.3 Gain definitions

The gain of an amplifier is specified in several ways depending on how the (theoretical) measurement is implemented, on stability conditions, and on way of matching (e.g. best power processing, max. gain, lowest noise figure or a certain stability performance). Often certain power gains are calculated for the upper and lower possible parameter extremes. Additionally calculating circles in the smith chart (power gain circles, stability circles) can be used to select a useful working range in the input or output. The algebraic expressions used can vary from one literature source to the other. In reality S12 cannot be neglected, causing the output being a function of the required source and the input being a function of the required load. This makes matching complicated and is a part of the GA and GP design procedure.

Transducer power gain: $$G_T = \frac{P_L}{P_{AVS}} = \frac{\text{power delivered to the load}}{\text{power available from the source}}$$

This includes the effect of I/O matching and device gain but doesn't take into account the losses in components.

Power gain or operating power gain: $$G_P = \frac{P_L}{P_{IN}} = \frac{\text{power deliverd to the load}}{\text{power input to the network}}$$

Used in the case of non-negligible S_{12}, G_P is independent of the source impedance.

Available power gain: $$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{\text{power avaialble from the network}}{\text{power avaialble from the source}}$$

G_A is independent of the load impedance.

Maximum available gain (MAG): $$MAG = G_{T,\max} = 10\log\left(\frac{|S_{21}|}{|S_{12}|}\cdot\left|K \pm \sqrt{K^2-1}\right|\right)$$

The MAG you could ever hope to get from a transistor is under simultaneous conjugated I/O match with a **Rollett stability** factor of K>1. K is calculated from the s-parameters in several sub steps. At a frequency of unconditional stability, MAG ($GT_{,max}$=$GP_{,max}$=$GA_{,max}$) is plotted in transistor data sheets.

Maximum stable gain: $$MSG = \frac{|S_{21}|}{|S_{12}|}$$

MSG is a figure of merit for a potentially unstable transistor and valid for K=1 (subset of MAG). At a frequency of potential instability, MSG is plotted in transistor data sheets.

Further examples of used definitions in the design of amplifiers:

- $GT_{,max}$ = Maximum transducer power gain under simultaneous conjugated match conditions
- $GT_{,min}$ = Minimum transducer power gain under simultaneous conjugated match conditions
- GT_U = Unilateral transducer power gain
- $GP_{,min}$ = Minimum operating power gain for potential unstable devices

- Unilateral figure of merit $\frac{G_T}{G_{TU}}$ determine the error caused by assuming S_{12}=0.

The adjacent example shows the **BGU2003's** gain as a function of frequency

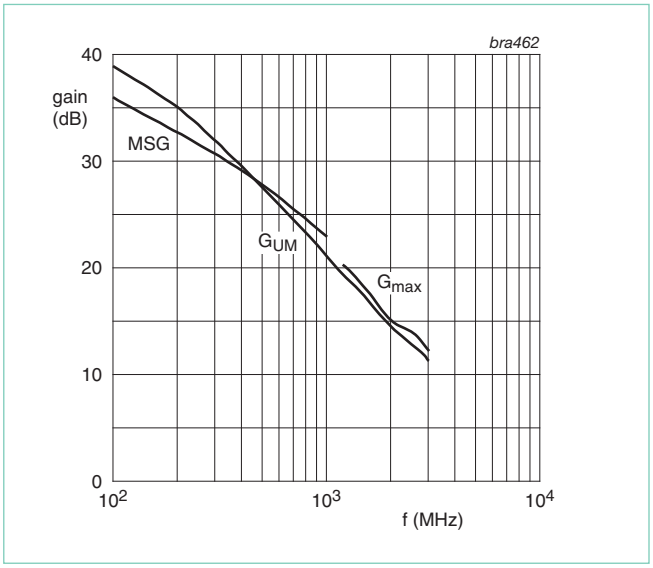
In the frequency range of 100 MHz to 1 GHz the MMIC is potentially unstable. Above 1.2 GHz the MMIC is unconditionally stable (within the 3 GHz range of measurement)

G_{UM} is the maximum unilateral transducer power gain assuming S_{12}=0 and a conjugated I/O match: A S12=0 (=unilateral figure of merit) specify an unilateral 2-port network resulting in K=infinite and D_s=S_{11}*S_{22}

$$G_{TU,\max} = 10\log\frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)}dB$$

$$G_{UM} = 10\log\left(G_{TU,\max}\right)$$

For further details please refer to books e.g. Pozar, Gonzalez, Bowick, etc.



4.3.4 Amplifier stability

All variables must be processed with complex data. The evaluated K-factor is only valid for the frequency and bias setup for the selected s-parameter quartet [S_{11}, S_{12}, S_{21}, S_{22}]

Determinant: $$D_S = S_{11}\cdot S_{22} - S_{12}\cdot S_{21}$$

Rollett stability factor: $$K = \frac{1+|D_S|^2-|S_{11}|^2-|S_{22}|^2}{2\cdot|S_{21}\cdot S_{12}|}$$

In some literature sources, the size of D_s isn't take into account for dividing into the following stability qualities.

K>1 & |Ds|<1
Unconditionally stable for any combination of source and load impedance

K<1
Potentially unstable and will most likely oscillate with certain combinations of source and load impedance. It does not mean that the transistor will not be useable for the application. It means the transistor is more tricky to use. A simultaneous conjugated match for the I/O isn't possible.

-1<K<0
Used in oscillator designs

K>1 & |Ds|>1
This potentially unstable transistors with the need $SWR_{(IN)}=SWR_{(OUT)}=1$ are not manufactured and do have a gain of $G_{T,min}$.

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射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训推荐课程列表： http://www.edatop.com/peixun/tuijian/

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

课程网址：http://www.edatop.com/peixun/rfe/110.html

手机天线设计培训视频课程

该套课程全面讲授了当前手机天线相关设计技术，内容涵盖了早期的外置螺旋手机天线设计，最常用的几种手机内置天线类型——如 monopole 天线、PIFA 天线、Loop 天线和 FICA 天线的设计，以及当前高端智能手机中较常用的金属边框和全金属外壳手机天线的设计；通过该套课程的学习，可以帮助您快速、全面、系统地学习、了解和掌握各种类型的手机天线设计，以及天线及其匹配电路的设计和调试...

课程网址： http://www.edatop.com/peixun/antenna/133.html

WiFi 和蓝牙天线设计培训课程

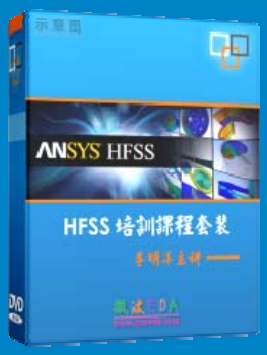
该套课程是李明洋老师应邀给惠普 (HP)公司工程师讲授的 3 天员工内训课程录像，课程内容是李明洋老师十多年工作经验积累和总结，主要讲解了 WiFi 天线设计、HFSS 天线设计软件的使用，匹配电路设计调试、矢量网络分析仪的使用操作、WiFi 射频电路和 PCB Layout 知识，以及 EMC 问题的分析解决思路等内容。对于正在从事射频设计和天线设计领域工作的您，绝对值得拥有和学习！…

课程网址：http://www.edatop.com/peixun/antenna/134.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

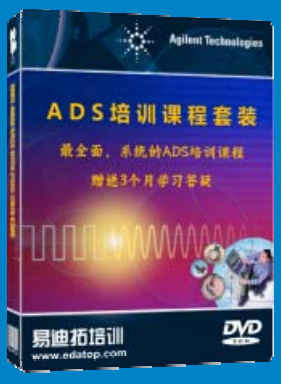


HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

ADS 学习培训课程套装



该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com