PRELIMINARY
May 2005

AR2316 Single Chip MAC/Baseband/Radio and Processor for 2.4 GHz Wireless LANs

General Description

The Atheros AR2316 integrated the MAC/baseband/radio and processor into a single chip for wireless access point and router applications. It includes a 2.4 GHz radio, MIPS 4000 processor, 802.11 MAC/baseband processor, 802.3 Ethernet MAC and MII interface, SDRAM controller, external memory interface for Flash, ROM, or RAM, PCI bus interface or a flexible local bus, UART, GPIOs, LED controls.

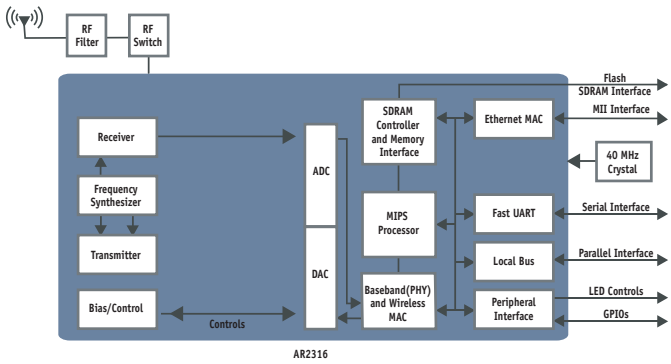
The AR2316 implements an 802.11 MAC/baseband processor supporting all IEEE 802.11g data rates (1 to 54 Mbps) and all IEEE 802.11b complementary key coding (CCK) data rates (1 to 11 Mbps). In Atheros Super G™ mode, AR2316 supports data rates up to 108 Mbps. Additional features include forward error correction coding at rates for 1/2, 2/3, and 3/4, signal detection, automatic gain control, frequency offset estimation, symbol timing, channel estimation, error recovery, enhanced security, and quality of service (QoS). The AR2316 performs receive and transmit filtering for IEEE 802.3 and 802.11 networks.

The AR2316 is an all CMOS, highly integrated single-chip solution that supports 802.11b/g WLANs.

Features

- Integrated MIPS 4000 processor
- 180 MHz processor frequency
- IEEE 802.11b/g Access Point, Ad Hoc, and station functions supported
- OFDM and CCK modulation schemes supported
- Data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, 54 Mbps and Atheros Super G™ mode offering up to 108 Mbps
- IEEE 802.3 Ethernet MAC supporting 10/100 Mbps, full and half duplex, and MII interface to external Ethernet PHY
- UART for console support
- Flexible, programmable local bus
- PCI bus host and client modes
- IEEE 1149.1 standard test access port and boundary scan architecture supported
- EJTAG based debugging of the processor core supported
- Standard 0.18 µm CMOS technology
- 15 mm x 15 mm 233 PBGA package

System Block Diagram



1. Pin Descriptions

This section contains both a package pinout (see Table 1-1 through Table 1-5) and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

- NC indicates no connection should be made to this pin.
- _L at the end of the signal name indicates active low signal.
- P at the end of the signal name indicates the positive side of a differential signal.
- N at the end of the signal name indicates the negative side of a differential signal.

The following nomenclature is used for signal types:

- IA indicates an analog input signal.
- I indicates a digital input signal.
- IH indicates input signals with weak internal pull-up, to prevent signals from floating when left open.
- IL indicates input signals with weak internal pull-down, to prevent signals from floating when left open.
- I/O indicates a digital bidirectional signal.
- OA indicates an analog output signal.
- O indicates a digital output signal.
- P indicates a power or ground signal.

Table 1-1. **AR2316 Pin Assignments (1–9)**

	1	2	3	4	5	6	7	8	9
A	GPIO_7	PCI_CBE1_L / LB_DATA_0[1]	GPIO_5	GPIO_3	GPIO_2	GPIO_1	MODE_SEL_1	WF_ANTC	WF_ANTB
B	GPIO_6	PCI_AD_14 / LB_DATA_4	PCI_DEVSEL_L / LB_DATA_8	GPIO_4	PCI_SERR_L / LB_DATA_6	PCI_CLKRUN_L / LB_DATA_10	WF_ANTD	PCI_AD_16 / LB_DATA_11	WF_ANTA
C	PCI_AD_15 / LB_ADDR_12	PROC_REF_CLK	GND	PCI_PERR_L / LB_DATA_7	GPIO_0	MODE_SEL_0	PCI_FRAME_L / LB_DATA_13	PCI_IRDY_L / LB_DATA_12	PCI_CBE2_L / LB_DATA_9
D	PCI_AD_11 / GPIO_11	PCI_AD_12 / LB_RDY_L	PCI_AD_13 / LB_ADDR_14	GND	PCI_STOP_L / LB_DATA_9	PCI_TRDY_L / LB_ADDR_5	VDD33	VDD33	VDD19
E	SD_DATA_1	SD_DATA_0	SD_DATA_15	PCI_AD_10	NA	NA	NA	NA	NA
F	SD_DATA_14	PCI_AD_9 / GPIO_8	SD_DATA_13	SD_DATA_2	NA	NA	NA	NA	NA
G	PCI_AD_8 / LB_ADDR_15	SD_DATA_12	SD_DATA_8	SD_DATA_3	NA	NA	GND	GND	GND
H	SD_DATA_11	PCI_CBE0_L / GPIO_9	VDD19	VDD19	NA	NA	GND	GND	GND
J	SD_DATA_10	PCI_AD_7 / LB_ADDR_0	SD_WE_L	VDD19	NA	NA	GND	GND	GND
K	SD_DATA_9	PCI_AD_6 / LB_OE_L	SD_DATA_4	VDD33	NA	NA	GND	GND	GND
L	PCI_AD_5 / LB_INTR	SD_DATA_5	PCI_AD_4 / LB_WAIT_L	VDD33	NA	NA	GND	GND	GND
M	SD_DATA_6	SD_CAS_L	SD_DATA_7	SD_DQM_0	NA	NA	NA	NA	NA
N	PCI_AD_2 / LB_DATA_1	SD_DQM_1	PCI_AD_3 / LB_DATA_5	SD_RAS_L	NA	NA	NA	NA	NA
P	SD_CLK	PCI_AD_0 / LB_ADDR_2	SD_CLK_FB	GND	SD_BANK_0	PCI_REQ1_L / LB_DATA_3	SD_ADDR_1	VDD19	VDD19
R	SD_BANK_1	SD_CKE	GND	SD_ADDR_9	SD_ADDR_8	SD_ADDR_6	SD_ADDR_12	PCI_GNT1_L / LB_ADDR_8	ETH_CRS
T	PCI_AD_1 / LB_ADDR_1	SD_CS_L	PCI_INT_L / LB_WE_L	SD_ADDR_0	PCI_GNT0_L / LB_DATA_2	SD_ADDR_2	SD_ADDR_5	PCI_AD_29 / GPIO_22	PCI_AD_30 / GPIO_20
U	SD_ADDR_10	SD_ADDR_11	PCI_RST_L / LB_ADDR_4	PCI_REQ0_L / LB_CS	SD_ADDR_7	PCI_AD_31 / LB_ADDR_7	SD_ADDR_4	SD_ADDR_3	ETH_TXD_3

[1]Note that two listed pin assignments show multiplexing pins, and list the PCI pin name / Local Bus pin name.

Table 1-2. **AR2316 Pin Assignments (10–17)**

	10	11	12	13	14	15	16	17
A	RFOUTN_BIAS	RFOUTN	RFOUTP	RFOUTP_BIAS	AGND	RFINN	RFINP	AGND
B	AGND	AVDD	AVDD	AGND	AGND	AGND	AGND	AGND
C	AVDD	PDETN	PDETP	AVDD33	NC	AGND	NC	NC
D	VDD19	PCI_EPRM_EN_ / LB_MASTER[1]	AVDD	AVDD33	AGND	AVDD	NC	NC
E	NA	NA	NA	NA	AVDD33	BIASREF	AGND	AVDD
F	NA	NA	NA	NA	AVDD33	VREG_OUT	NC	NC
G	GND	GND	NA	NA	VDD33	AGND	AVDD	AVDD33
H	GND	GND	NA	NA	VDD33	VREG_COMP	XTALO	XTALI
J	GND	GND	NA	NA	VDD19	UART_SIN	PCI_AD_18 / LB_DATA_14	UART_SOUT
K	GND	GND	NA	NA	VDD19	TRST_L	PCI_AD_17 / LB_ADDR_10	EJTAG_SEL
L	GND	GND	NA	NA	PCI_PAR / LB_DATA_15	TCLK	TDI	TDO
M	NA	NA	NA	NA	SPI_MOSI	PCI_AD_20 / LB_ADDR_13	COLD_RST_L	TMS
N	NA	NA	NA	NA	ETH_RXC	SPI_CS_L	SPI_CK	PCI_AD_19 / LB_ADDR_11
P	VDD33	VDD33	ETH_TXD_0	PCI_CBE3_L / GPIO_16	GND	ETH_MDIO	SPI_MISO	PCI_AD_22 /
R	VDD33	ETH_TXD_1	ETH_COL	ETH_RXD_0	ETH_RXD_1	GND	PCI_CLK / GPIO_13	ETH_RESET_L
T	ETH_TXD_2	PCI_AD_28 / GPIO_19	ETH_RXERR	PCI_AD_26 / GPIO_17	PCI_AD_24 / GPIO_15	ETH_TXC	PCI_IDSEL / LB_ADDR_6	PCI_AD_21 / GPIO_14
U	PCI_AD_27 / GPIO_21	PCI_AD_25 / GPIO_18	ETH_RXDV	ETH_TXEN	ETH_RXD_2	ETH_RXD_3	PCI_AD_23 / LB_ADDR_3	ETH_MDC

[1]Note that two listed pin assignments show multiplexing pins, and list the PCI pin name / Local Bus pin name.

Table 1-3, Table 1-4, and Table 1-5 provide the signal-to-pin relationship information for the AR2316.

Table 1-3. **PCI Signal to Pin Relationships and Descriptions**

Signal Name	Pin	Direction	Description
PCI_CLK	R16	I/O	PCI clock, input for target, output for master
PCI_AD_31	U6	I/O	Multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contains a physical byte address. During subsequent clocks, it contains data.
PCI_AD_30	T9	I/O	
PCI_AD_29	T8	I/O	
PCI_AD_28	T11	I/O	
PCI_AD_27	U10	I/O	
PCI_AD_26	T13	I/O	
PCI_AD_25	U11	I/O	
PCI_AD_24	T14	I/O	
PCI_AD_23	U16	I/O	
PCI_AD_22	P17	I/O	
PCI_AD_21	T17	I/O	
PCI_AD_20	M15	I/O	
PCI_AD_19	N17	I/O	
PCI_AD_18	J16	I/O	
PCI_AD_17	K16	I/O	
PCI_AD_16	B8	I/O	
PCI_AD_15	C1	I/O	
PCI_AD_14	B2	I/O	
PCI_AD_13	D3	I/O	
PCI_AD_12	D2	I/O	
PCI_AD_11	D1	I/O	
PCI_AD_10	E4	I/O	
PCI_AD_9	F2	I/O	
PCI_AD_8	G1	I/O	
PCI_AD_7	J2	I/O	
PCI_AD_6	K2	I/O	
PCI_AD_5	L1	I/O	
PCI_AD_4	L3	I/O	
PCI_AD_3	N3	I/O	
PCI_AD_2	N1	I/O	
PCI_AD_1	T1	I/O	
PCI_AD_0	P2	I/O	

Table 1-3. **PCI Signal to Pin Relationships and Descriptions**

Signal Name	Pin	Direction	Description
PCI_CBE3_L	P13	I/O	PCI multiplexed bus command and byte enables. During the address phase of a transaction, these signals define the bus command. During the data phase, they are used as byte enables.
PCI_CBE2_L	C9	I/O	
PCI_CBE1_L	A2	I/O	
PCI_CBE0_L	H2	I/O	
PCI_CLKRUN_L	B6	I	Provides for starting and stopping the PCI clock.
PCI_DEVSEL_L	B3	I/O	PCI device select.
PCI_EPRM_EN_L	D11		
PCI_FRAME_L	C7	I/O	PCI frame.
PCI_GNT1_L	R8	I	PCI grant.
PCI_GNT0_L	T5	I	
PCI_IDSEL	T16	I	PCI ID select.
PCI_INT_L	T3	O	PCI interrupt.
PCI_IRDY_L	C8	I/O	PCI initiator ready.
PCI_PAR	L14	I/O	PCI parity.
PCI_PERR_L	C4	I/O	PCI parity error.
PCI_REQ1_L	P6	O	PCI request.
PCI_REQ0_L	U4	O	
PCI_RST_L	U3	I	PCI Reset
PCI_SERR_L	B5	I/O	PCI system error.
PCI_STOP_L	D5	I/O	PCI stop.
PCI_TRDY_L	D6	I/O	PCI target ready.

Table 1-4. **Local Bus Signal-to-Pin Relationships**

Signal Name	Pin	Direction	Description
Local Bus			
LB_ADDR_0	J2	I	Address [0]
LB_ADDR_1	T1	I	Address [1]
LB_ADDR_2	P2	I	Address [2]
LB_ADDR_3	U16	I	Address [3]
LB_CS	U4	I	Chip select
LB_DATA_15	L14	I/O	Data [15]
LB_DATA_14	J16	I/O	Data [14]
LB_DATA_13	C7	I/O	Data [13]
LB_DATA_12	C8	I/O	Data [12]
LB_DATA_11	B8	I/O	Data [11]
LB_DATA_10	C5	I/O	Data [10]
LB_DATA_9	D5	I/O	Data [9]
LB_DATA_8	C3	I/O	Data [8]
LB_DATA_7	C4	I/O	Data [7]
LB_DATA_6	B5	I/O	Data [6]

Table 1-4. **Local Bus Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
LB_DATA_5	N3	I/O	Data [5]
LB_DATA_4	B2	I/O	Data [4]
LB_DATA_3	P6	I/O	Data [3]
LB_DATA_2	T5	I/O	Data [2]
LB_DATA_1	N1	I/O	Data [1]
LB_DATA_0	A2	I/O	Data [0]
LB_INTR	L1	O	Interrupt output
LB_OE_L	K2	I	Output enable
LB_RDY_L	D2	I	Ready input
LB_WAIT_L	L3	O	Wait output
LB_WE_L	T3	I	Write enable
GPIO			
GPIO8	F2		General purpose GPIO pins
GPIO9	H2		
GPIO10	E4		
GPIO11	D1		
GPIO12	P17		
GPIO14	T17		
GPIO15	T14		
GPIO16	P13		
GPIO17	T13		
GPIO18	U11		
GPIO19	T11		
GPIO20	T9		
GPIO21	U10		
GPIO22	T8		

Table 1-5. **Signal-to-Pin Relationships**

Signal Name	Pin	Direction	Description
General			
GPIO0	C5	I/O	General purpose GPIO pins
GPIO1	A6	I/O	
GPIO2	A5	I/O	
GPIO3	A4	I/O	
GPIO4	B4	I/O	
GPIO5	A3	I/O	
GPIO6	B1	I/O	
GPIO7	A1	I/O	
BIASREF	E15	IA	Connects a 6.19 ohm +/- 1% resistor to ground.
COLD_RST_L	M16	I	Reset entire chip
SPI_CK	N16		SPI Serial Flash Clock
SPI_CS_L	N15		SPI Serial Flash Chip Select
SPI_MISO	P16		SPI Serial Flash Data - Master In, Slave out
SPI_MOSI	M14		SPI Serial Flash Data - Master Out, Slave In
VREG_COMP	H15	OA	Compensation node for voltage regulator

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
VREG_OUT	F15	IA	1.9V voltage regulator output
XTALI	H17	I	40 MHz crystal
XTALO	H16	O	40 MHz crystal
PROC_REF_CLK	C3		
Ethernet			
ETH_COL	R12	I	Collision Detect
ETH_MDIO	P15	I/O	PHY chip control bus data
ETH_MDC	U17	O	PHY chip control bus clock
ETH_RESET_L	R17	O	PHY Reset
ETH_RXC	N14	I	Receive Clock (2.5MHz @ 10Mbit; 25MHz @ 100Mbit)
ETH_RXD_0	R13	I	Receive Data
ETH_RXD_1	R14	I	
ETH_RXD_2	U14	I	
ETH_RXD_3	U15	I	
ETH_RXDV	U12	I	Receive Data Valid
ETH_RXERR	T12	I	Receive Error
ETH_TXC	T15	I	Transmit Clock (2.5MHz @ 10Mbit; 25MHz @ 100Mbit)
ETH_TXD_0	P12	O	Transmit Data
ETH_TXD_1	R11	O	
ETH_TXD_2	T10	O	
ETH_TXEN	U13	O	Transmit Enable
JTAG Interface			
EJTAG_SEL	K17	I	When asserted, JTAG pins are routed to EJATAG TAP controller. When deasserted, JTAG pins are routed to TAP controller.
TCLK	L15	I	JTAG test clock
TDI	L16	I	JTAG data input
TDO	L17	O	JTAG data output
TMS	M17	I	JTAG test mode
TRST_L	K15	I	JTAG test reset
Mode Selection			
MODE_SEL_1	A7	I	Selects the desired bus configuration
MODE_SEL_0	C6	I	
RF Interface			
PDETN	C11	IA	Differential Power detector
PDETP	C12	IA	
RFINN	A15	IA	Differential RF input
RFINP	A16	IA	
RFOUTN	A11	OA	Differential RF output
RFOUTP	A12	OA	
RFOUTP_BIAS	A13	IA	1.9 V
RFOUTN_BIAS	A10	IA	1.9 V

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
Antenna Control			
WF1_ANTA	B9	O	Antenna selection
WF1_ANTB	A9	O	
WF1_ANTC	A8	O	
WF1_ANTD	B7	O	
DRAM Control			
SD_DATA_15	E3	I/O	Read/write data [15]
SD_DATA_14	F1	I/O	Read/write data [14]
SD_DATA_13	F3	I/O	Read/write data [13]
SD_DATA_12	G2	I/O	Read/write data [12]
SD_DATA_11	H1	I/O	Read/write data [11]
SD_DATA_10	J1	I/O	Read/write data [10]
SD_DATA_9	K1	I/O	Read/write data [9]
SD_DATA_8	G3	I/O	Read/write data [8]
SD_DATA_7	M3	I/O	Read/write data [7]
SD_DATA_6	M1	I/O	Read/write data [6]
SD_DATA_5	L2	I/O	Read/write data [5]
SD_DATA_4	K3	I/O	Read/write data [4]
SD_DATA_3	G4	I/O	Read/write data [3]
SD_DATA_2	F4	I/O	Read/write data [2]
SD_DATA_1	E1	I/O	Read/write data [1]
SD_DATA_0	E2	I/O	Read/write data [0]
SD_CLK	P1	O	SDRAM clock
SD_CKE	R2	O	SDRAM clock enable
SD_CLK_FB	P3	I	SDRAM clock feedback
SD_CAS_L	M2	O	Column address select
SD_RAS_L	N4	O	Row address select
SD_CS_L	T2	O	Chip select for DRAM
SD_BANK_1	R1	O	Bank address [1]
SD_BANK_0	P5	O	Bank address [0]
SD_DQM_1	N2	O	Data mask for byte 1
SD_DQM_0	M4	O	Data mask for byte 0
SD_WE_L	J3	O	Write enable
SD_ADDR_12	R7	O	Row/column address within bank
SD_ADDR_11	U2	O	
SD_ADDR_10	U1	O	
SD_ADDR_9	R4	O	
SD_ADDR_8	R5	O	
SD_ADDR_7	U5	O	
SD_ADDR_6	R6	O	
SD_ADDR_5	T7	O	
SD_ADDR_4	U7	O	
SD_ADDR_3	U8	O	
SD_ADDR_2	T6	O	
SD_ADDR_1	P7	O	
SD_ADDR_0	T4	O	

Table 1-5. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
UART Control			
UART_SOUT	J17	O	Serial output data
UART_SIN	J15	I	Serial input data
Power			
AGND	A14, A17, B10, B13, B14, B15, B16, B17, C15, D14, E16, G15		Analog ground
AVDD	B11, B12, C10, D12, D15, E17, G16		Analog 1.9V supply
AVDD33	C13, D13, E14, F14, G17		Analog 3.3V supply
NA	E5, E6, E7, E8, E9, E10, E11, E12, E13, F5, F6, F7, F8, F9, F10, F11, F12, F13, G5, G6, G12, G13, H5, H6, H12, H13, J5, J6, J12, J13, K5, K6, K12, K13, L5, L6, L12, L13, M5, M6, M7, M8, M9, M10, M11, M12, M13, N5, N6, N7, N8, N9, N10, N11, N12, N13		Not Applicable
GND	C3, D4, G7, G8, G9. G10. G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11, P4, P14, R3, R15		Digital ground
VDD19	D9, D10, H3, H4, J4, J14, K14, P8, P9		Digital 1.9V
VDD33	D7, D8, G14, H14, K4, L4, P10, P11, R10		Digital 3.3V
No Connection			
NC	C14, C16, C17, D16, D17, F16, F17		No connection, must be open

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1 summarizes the absolute maximum ratings and Table 2-2 lists the recommended operating conditions for the AR2316. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 2-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max. Rating	Unit
V_{DD19}	Supply Voltage (1.9 V)	–0.3 to 3.6	V
V_{DD33}	I/O Supply Voltage (3.3 V)	–0.3 to 4.6	V
T_{store}	Storage Temperature	–65 to 150	°C
ESD	Electrostatic Discharge Tolerance	TBD	V

2.1.1 Recommended Operating Conditions

Table 2-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD19}[1]	Supply Voltage	±5%	1.8	1.9	2.0	V
V_{DD33}	I/O Supply Voltage	± 10%	3.0	3.3	3.6	V
T_{case}	Case Temperature		0	25	95	°C
T_J	Junction Temperature		0	50	110	°C
θ_{JA}	Junction to Ambient Temperature				25	°C/W

[1]The recommended power-on sequence is V_{DD33} before VDD19.

2.2 General DC Electrical Characteristics

Table 2-3 lists the general DC electrical characteristics. The following conditions apply to all DC characteristics unless otherwise specified:

V_{dd} = 3.3 V, T_{amb} = 25 °C

Table 2-3. **General DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage	$V_{out} = V_{OH\ (min)}$	2.0	—	V_{dd} + 0.3	V
V_{IL}	Low Level Input Voltage	$V_{out} = V_{OL\ (min)}$	–0.3	—	0.8	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	—	± 5	—	µA
		With Pull-up or Pull-down	—	± 65	—	µA
V_{OH}	High Level Output Voltage	No Load (I_o = 0)	V_{dd} –0.3	—	—	V
		I_o = 12 mA	V_{dd} –0.8	—	—	V
V_{OL}	Low Level Output Voltage	No Load (I_o = 0)	—	—	0.20	V
		I_o = 12 mA	—	—	0.27	V
I_O	Output Current (SYS_RESET_L, LCL_0, LCL_1, LCL_2, LCL_3, GPIO_0, GPIO_1, GPIO_2, GPIO_3, M1_MDIO, MEM_WE_L, SD_CS_L, SD_CLK)	V_o = 0 to V_{dd}	—	—	12	mA
I_O	Output Current All other digital output pins	V_o = 0 to V_{dd}	—	—	8	mA
C_{IN}	Input Capacitance	—	—	6	—	pF

2.2.1 Radio Receiver Characteristics

Table 2-4 summarizes the receiver characteristics for the AR2316.

Table 2-4. **Receiver Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	2.312	—	2.484	GHz
NF	Receive chain noise figure	See Note [1]	—	5.5	—	dB
S_{rf}	Sensitivity	See Note [2]				dBm
	CCK, 1 Mbps		—	–95	—	
	CCK, 11 Mbps		—	–90	—	
	OFDM, 6 Mbps		—	–92	—	
	OFDM, 54 Mbps		—	–73	—	
IP1dB	Input 1 dB compression (min. gain)	—	—	–10	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	–1	—	dBm
Z_{RFin_input}	Recommended LNA differential drive impedance	See Note [3]	—	9+j40	—	—
ER_{phase}	I,Q phase error		—	1	—	degree
ERamp	I,Q amplitude error		—	0.5	—	dB
R_{adj}	Adjacent channel rejection	10 to 20 MHz [4]				dB
	CCK		35		—	
	OFDM, 6 Mbps		16	20	—	
	OFDM, 54 Mbps		–1	3	—	
TRpowup	Time for power up (from synth on)	—	—	1	—	µs

[1]An increase of 2 dB in noise figure is expected at 95°C. For improved sensitivity performance, an external LNA may be used.
[2]Sensitivity performance is based on the Atheros reference design which includes RF filter, Tx/Rx antenna switch and an external LNA.
[3]Refer to the *Hardware Design Guide* for information.
[4]Measured with AR2316.

2.2.2 Radio Transmitter Characteristics

Table 2-5 summarizes the transmitter characteristics for the AR2316.

Table 2-5. **Transmitter Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.312	—	2.484	GHz
P_{out}	Mask Compliant CCK output power	See Note [1]	—	0	—	dBm
	EVM Compliant OFDM output power for 64 QAM	See Note [1]		–4	—	dBm
SP_{gain}	PA gain step	See Note [2]	—	0.5	—	dB
A_{pl}	Accuracy of power leveling loop	See Notes [3] [4]	—	± 0.5	—	dB
Z_{RFout_load}	Recommended PA differential load impedance	See Note [5]	—	10 – j30	—	—
OP1dB	Output P1dB (max. gain)	2.442 GHz	—	6	—	dBm
OIP3	Output third order intercept point (max. gain)	2.442 GHz	—	13	—	dBm
SS	Sideband suppression		—	–40	—	dBc
RS	Synthesizer reference spur:	—	—	–65		dBc
Tx_{mask}	Transmit spectral mask	See Note [6]				dBr
	CCK					
	At 11 MHz offset		–30	–35	—	
	At 22 MHz offset		–50	–53	—	
	OFDM					
	At 11 MHz offset		–20	–27	—	
	At 20 MHz offset		–28	–38	—	
	At 30MHz offset		–40	–52	—	
TTpowup	Time for power up (from synth on)	—	—	1.5	—	µs

[1]Measured using the balun recommended by Atheros under closed-loop power control.
[2]Guaranteed by design.
[3]Manufacturing calibration required.
[4]Not including tolerance of external power detector and its temperature variation.
[5]Refer to the design guide for information.
[6]Measured at the antenna connector port. Average conducted transmit power levels = 20 dBm (CCK), 19 dBm at 64 QAM (OFDM). System includes external PA.

2.2.3 Synthesizer Characteristics

Table 2-6 summarizes the synthesizer characteristics for the AR2316.

Table 2-6. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pn	Phase noise (at Tx_Out)					dBc/Hz
	At 30 kHz offset		—	–105	—	
	At 100 kHz offset		—	–105	—	
	At 500 kHz offset		—	–105	—	
	At 1 MHz offset		—	–120	—	
F_c	Center channel frequency	Center frequency at 5 MHz spacing See Note [1]	2.312	—	2.484	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm	—	40	—	MHz
F_{step}	Frequency step size (at RF)	See Note	—	1	—	MHz
TS_{powup}	Time for power up (from sleep)	—	—	0.2	—	ms

[1]Frequency is measured at the TX output.

2.3 Power Consumption

These conditions apply to the following typical characteristics unless otherwise specified:

V_{DD19}= 1.9 V, V_{DD33} = 3.3 V,
AVDD = 1.9 V, T_{amb} = 25 °C

The following table depicts the typical power drain on each of the three on-chip power supply domains as a function of the AR2316's operating mode.

Operating Mode	Unit
1.9V Supply	500mA
3.3V Supply	50mA

3. Register Descriptions

This section describes internal registers for the various blocks of the AR2316.

3.1 Reset/Configuration Control Registers

Table 3-1 summarizes the AR2316 Reset/Configuration registers. These registers use:

- Internal base address: 0x1100_0000
- External PCI MBAR_0 base offset: 0x1_4000

Table 3-1. **Reset/Configuration Control Register Summary**

Offset	Name	Description	Page
0x0000	RST_COLD_CTL	Cold reset control	page 22
0x0004	RST_WARM_CTL	Warm reset control	page 22
0x0008	RST_AHB_ARB_CTL	AHB master arbitration control	page 23
0x000C	RST_BYTESWAP_CTL	Byteswap control	page 23
0x0010	RST_NMI_CTL	CPU non-maskable interrupt control	page 25
0x0014	RST_SREV	Silicon revision	page 25
0x0018	RST_IF_CTL	Interface control	page 25
0x0020	RST_MISR	Miscellaneous interrupt status	page 27
0x0024	RST_MIMR	Miscellaneous interrupt mask	page 28
0x0028	RST_GISR	Global interrupt status	page 28
0x0030	RST_GTIME	General timer	page 29
0x0034	RST_GTIME_RELOAD	General timer reload value	page 29
0x0038	RST_WDOG	Watchdog timer	page 29
0x003C	RST_WDOG_CTL	Watchdog timer control	page 29
0x0040	RST_MEMCTL	SDR-DRAM memory controller parameters	page 30
0x0044	RST_CPUPERF_CTL	CPU performance counter control	page 31
0x0048	RST_CPUPERF_0	CPU performance counter 0	page 31
0x004C	RST_CPUPERF_1	CPU performance counter 1	page 32
0x0050	RST_AHBERR0	AHB error status register 0	page 32
0x0054	RST_AHBERR1	AHB error status register 1	page 32
0x0058	RST_AHBERR2	AHB error status register 2	page 33
0x005C	RST_AHBERR3	AHB error status register 3	page 33
0x0060	RST_AHBERR4	AHB error status register 4	page 33
0x0064	RST_PLLC_CTL	CPU/AHB/APB PLL (PLLc) control	page 34
0x006C	RST_CPUCLK_CTL	CPU final clock MUX/divider control	page 35
0x0070	RST_AMBACLK_CTL	AHB/APB final clock MUX/divider control	page 35
0x0074	RST_SYNCCLK_CTL	Video sync. final clock MUX/divider control	page 36
0x0080	RST_DSL_SLEEP_CTL	DSL sleep control	page 36
0x0084	RST_DSL_SLEEP_DUR	DSL sleep duration	page 37
0x0088	RST_GPIOIN0	GPIO input, set 0	page 37
0x0090	RST_GPIOOUT0	GPIO output, set 0	page 37
0x0098	RST_GPIODIR0	GPIO direction, set 0	page 37
0x00A0	RST_GPIOINTR	GPIO interrupt control	page 38
0x00A4	RST_PCICLK_CTL	PCI final clock MUX/divider control	page 38
0x00A8	RST_SCRATCH0	Scratch register 0	page 39
0x00AC	RST_SCRATCH1	Scratch register 1	page 39
0x00B0	RST_OBS_CTL	Observation control	page 39
0x00B4	RST_MISCCLK_CTL	General clock control	page 40
0x00B8	RST_CIMR	Client interrupt mask	page 41

3.1.1 Cold Reset Control (RST_COLD_CTL)

Offset: 0x0000
Internal Address: 0x1100_0000
PCI Address: 0x1_4000
Access: Write-only (reads always return 0)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		AHB cold reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a cold reset to the AHB arbitration and MUXing logic and all connected blocks. Auto-clears after 128 clocks.
1		APB cold reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a cold reset to the APB arbitration and MUXing logic and all connected blocks. Auto-clears after 128 clocks.
2	RES	CPU cold reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a cold reset to the MIPS CPU (asserts the CPU's SI_ColdReset and SI_Reset inputs). Auto-clears after 128 clocks.
3		CPU warm reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a warm reset to the MIPS CPU (asserts the CPU's SI_Reset input). Auto-clears after 128 clocks.
31:4		Reserved

3.1.2 Warm Reset Control (RST_WARM_CTL)

Offset: 0x0004
Internal address: 0x1100_0004
PCI address: 0x1_4004
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		WMAC warm reset. Resets to 0x1.
1		WBB warm reset. Resets to 0x1.
2	RES	Reserved
3		PCI interface warm reset. Resets the AHB/PCI interface logic and PCI DMA logic, but not the PCI core; PCI_RC register bit [4] resets this. Resets to 0x0.
4		Memory controller warm reset. Resets to 0x0.
5		Local bus interface warm reset. Resets to 0x0.
6	RES	Reserved. Resets to 0x0.
7		SPI interface warm reset. Resets to 0x0.
8		UART interface warm reset. Resets to 0x0.
9	RES	Reserved. Resets to 0x0
10		Ethernet interface warm reset. Resets to 0x1.
11		Ethernet MAC warm reset. Resets to 0x1.
31:11	RES	Reserved

3.1.3 AHB Master Arbitration Control (RST_AHB_ARB_CTL)

Offset: 0x0008
Internal address: 0x1100_0008
PCI address: 0x1_4008
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Bits [4:0] in this register control whether the associated interface can arbitrate for access to the AHB bus as master. This register does not affect operation of these interfaces as AHB targets. For each bit:

- 0 = Requests for AHB master access from the interface are ignored
- 1 = Requests for AHB master access from the interface process normally. Some bits are affected by value of the interf_mode_sel signal, a two-bit signal connected directly to AR2316 pins. The value is a static selection of the interfaces enabled on cold reset exit. Encodings for interf_mode_sel are:

Value	Meaning
0	PCI mode (client mode)
1	Local bus mode (client if PCI_EPRM_EN_L = 0, host if = 1)
2	Radio test mode
3	PCI mode (host mode)

Bit	Bit Name	Description
0		CPU AHB master arbitration control. Resets to 0x1.
1		WMAC AHB master arbitration control. Resets to 0x0.
2	RES	Reserved
3		Local bus AHB master arbitration control. Resets to 0x0.
4		PCI AHB master arbitration control. Resets to 0x1.
5		Ethernet AHB master arbitration control. Resets to 0x0.
7:6	RES	Reserved
8		AHB master retry handling policy. For debug use only. Resets to 0x0. ■ 0 = Normal handling: re-arbitration occurs one cycle after the hresp=RETRY/hready cycle. ■ 1 = Conservative handling: re-arbitration occurs three cycles after the hresp=RETRY/hready cycle.
31:9	RES	Reserved

3.1.4 Byteswap Control (RST_BYTESWAP_CTL)

Offset: 0x000C
Internal address: 0x1100_000C
PCI address: 0x1_400C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		EC-to-AHB bridge Endianness control. This signal affects how the EC-to-AHB bridge logic handles sub-word-sized reads and writes when acting as AHB master. Resets to 0x0. ■ 0 = EC-to-AHB interface operates in little Endian mode ■ 1 = EC-to-AHB interface operates in big Endian mode
1		WMAC AHB master byteswap control. Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = WMAC AHB master interface does not byteswap data words ■ 1 = WMAC AHB master interface byteswaps data words for both writes and reads
2	RES	Reserved

Bit	Bit Name	Description
3		PCI endpoint AHB master byteswap control. Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = PCI endpoint AHB master interface does not byteswap data words ■ 1 = PCI endpoint AHB master interface byteswaps data words for both writes and reads
4		Memory controller Endianness control. This signal directly drives the Endian input to the Synopsys DesignWare DW_memctl module. Resets to 0x0. ■ 0 = DW_memctl operates in little Endian mode ■ 1 = DW_memctl operates in big Endian mode
5		Local bus AHB master byteswap control. Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = Local bus AHB master interface does not byteswap data words ■ 1 =Local bus AHB master interface byteswaps data words for reads and writes
6		Ethernet controller byteswap control. Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = Ethernet controller master interface does not byteswap data words ■ 1 = Ethernet controller byteswaps data words for both writes and reads
8:7	RES	Reserved
9		CPU write buffer merge mode. Resets to 0x0. ■ 0 = No merge ■ 1 = Full merge
10		CPU Endian control. Resets to 0x1. The reset value of this bit (currently 1), defines the value of the CPU_BIG_ENDIAN_RST parameter referenced as the reset value for various other register fields in the chip. ■ 0 = CPU operates in little Endian mode (CPU's SI_ENDIAN input negated) ■ 1 = CPU operates in big Endian mode (CPU's SI_ENDIAN input asserted)
11		PCI target AHB master byteswap control. Resets to 0x0. ■ 0 = PCI target AHB master interface does not byteswap data words ■ 1 = PCI target AHB master interface byteswaps data words for both writes and reads
12		PCI-to-AHB PCI target bridge Endianness control. This signal affects how the PCI-to-AHB bridge logic for externally-issued PCI transactions handles sub-word-sized reads and writes when acting as AHB master. Resets to 0x0. ■ 0 = PCI-to-AHB external transaction interface operates in little Endian mode ■ 1 = PCI-to-AHB external transaction interface operates in big Endian mode
14:13	RES	Reserved
15		CPU SPI access byteswap control. This bit controls whether the CPU swaps reads and writes to the two AHB SPI regions (AHB addresses 0x0800_0000-0x0FFF_FFFF and 0x1FC0_0000-0x1FFF_FFFF). Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = CPU does not swap SPI read/write data ■ 1 = CPU does swap SPI read/write data
16		CPU DRAM access byteswap control. This bit controls whether the CPU swaps reads and writes to the AHB DRAM region (AHB addresses 0x0000_0000-0x07ff_ffff). Resets to 0x0. ■ 0 = CPU does not swap DRAM read/write data ■ 1 = CPU does swap DRAM read/write data
17		CPU PCI external access byteswap control. This bit controls whether the CPU swaps reads and writes to the AHB PCI external region (AHB addresses 0x8000_0000-0xBFFF_FFFF). Resets to 0x0. ■ 0 = CPU does not swap PCI external read/write data ■ 1 = CPU does swap PCI external read/write data
18		CPU MMR access byteswap control. This bit controls whether the CPU swaps reads and writes to the AHB MMR regions (AHB addresses 0x1000_0000-0x17FF_FFFF). Resets to 0x0. ■ 0 = CPU does not swap MMR read/write data ■ 1 = CPU does swap MMR read/write data
31:19	RES	Reserved

3.1.5 CPU Non-Maskable Interrupt (NMI) Control (RST_NMI_CTL)

Offset: 0x0010
Internal address: 0x1100_0010
PCI address: 0x1_4010
Access: Write-only; reads always return 0x0
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		NMI control to CPU. Resets to 0x0. Write of: ■ 0 = No effect ■ 1 = Issues an NMI to the CPU (generates a pulse on the CPU's SI_NMI input)
31:1	RES	Reserved

3.1.6 Silicon Revision (RST_SREV)

Offset: 0x0014
Internal address: 0x1100_0014
PCI address: 0x1_4014
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
3:0		AR2316 revision level
7:4		AR2316 version level ■ 0x8 = AR2316 1.0 ■ (others) = Reserved
31:8	RES	Reserved

3.1.7 Interface Control (RST_IF_CTL)

Offset: 0x0018
Internal address: 0x1100_0018
PCI address: 0x1_4018
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
2:0		Interface enable control. Reset value is a function of the interf_mode_sel setting; see the Notes section of the RST_AHB_ARB_CTL register for details. The reset value of this field is determined by the interf_mode_sel setting: **Value** / **Reset Value for Field** 0 / 1 1 / 2 2 / 0 3 / 1 ■ 0 = Disable both PCI and local bus interfaces. For radio test. ■ 1 = Enable PCI interface. Disable the local bus interface. ■ 2 =Enable the local bus interface. Disable the PCI interface. ■ 3 = Enable both PCI and local bus interfaces. For emulation only. ■ 4 = Reserved ■ 5 = Reserved ■ 6 = Reserved ■ 7 = Reserved

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>3</td><td></td><td>Local bus host mode enable. Resets to <PCI_EPRM_EN_L>.
■ 0 = Local bus device is in slave mode
■ 1 = Local bus device is in host mode</td></tr>
<tr><td>4</td><td></td><td>PCI host mode enable. Resets to <INTERF_MODE_SEL[1] and INTERF_MODE_SEL[0]>.
■ 0 = PCI interface operates as a PCI client
■ 1 = PCI interface operates as a PCI host (can only write a 1 if PCI_AVAIL=1)</td></tr>
<tr><td>5</td><td></td><td>PCI interrupt enable. The value of this bit and the value of bit [15] of this register together control when asserts the PCI interrupt signal (PCI_INTA#). Both bits reset to 0.
<table>
<tr><th>Bit [5]</th><th>Bit [15]</th><th>Function</th></tr>
<tr><td>0</td><td>x</td><td>Never assert the PCI_INTA# signal</td></tr>
<tr><td>1</td><td>0</td><td>Assert PCI_INTA# whenever the logical AND of the global interrupt status register (RST_GISR) and the client interrupt mask register (RST_CIMR) are non-zero.</td></tr>
<tr><td>1</td><td>1</td><td>Assert PCI_INTA# whenever both:
■ The logical AND of the PCI interrupt status register (PCI_ISR) and the PCI host interrupt mask register (PCI_HIMR) is non-zero; and
■ The PCI host interrupt enable register (PCI_HIER) is non-zero. For use when the AR2316 CPU is enabled and an external host is transferring data between the AR2316 and host memory using AR2316 PCI DMA logic.</td></tr>
</table></td></tr>
<tr><td>7:6</td><td></td><td>DSL observation port MUX select. Controls what gets driven on the obs_dsl observation bus. Resets to 0x0.
■ 0 = AHB observation bus
■ 1 = APB observation bus
■ 2 = Reserved
■ 3 = Reserved</td></tr>
<tr><td>10:8</td><td></td><td>AHB observation port MUX select. Controls what gets driven on the obs_ahb observation bus. Resets to 0x0.
■ 0 = Ethernet WMAC-to-AHB bridge observation bus
■ 1 = Local bus interface observation bus
■ 2 = PCI interface observation bus
■ 3 = EC-to-AHB bridge observation bus
■ 4 = WMAC-to-AHB bridge observation bus
■ 5 = AHB bus observation group 0
■ 6 = AHB bus observation group 1
■ 7 = AHB bus observation group 2</td></tr>
<tr><td>13:11</td><td></td><td>APB observation port MUX select. Controls what gets driven on the obs_apb observation bus. Resets to 0x0.
■ 0 = APB bus observation group 0
■ 1 = APB bus observation group 1
■ 2 = APB bus observation group 2
■ 3 = APB bus observation group 3
■ 4 = APB bus observation group 4
■ 5 = Reserved
■ 6 = Reserved
■ 7 = Reserved</td></tr>
<tr><td>14</td><td></td><td>APB timeout disable. Resets to 0x0.
■ 0 = Enable APB timeout of 8192 cycles
■ 1 = Disable APB timeout</td></tr>
<tr><td>15</td><td></td><td>Additional select bit used to control when the AR2316 asserts the PCI interrupt (PCI_INTA#) signal. See the description that accompanies bit [5] of this register for details. Resets to 0.</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>17:16</td><td></td><td>PCI_CLK_EN control. Resets to 0x0. These bits control the PCI_CLK pin state.
<table>
<tr><th>Bit [17]</th><th>Bit [16]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>PCI_CLK pin behaves as an input.</td></tr>
<tr><td>0</td><td>1</td><td>PCI_CLK pin is set to output LOW.</td></tr>
<tr><td>1</td><td>0</td><td>PCI_CLK pin is set to output a clock.</td></tr>
<tr><td>1</td><td>1</td><td>PCI_CLK pin is set to output HI.</td></tr>
</table>
Note: It is recommended to do a reset sequence after this register is programmed. The when these bits are programmed to 01, the clock frequency is determined by the clock divider.</td></tr>
<tr><td>18</td><td></td><td>WMAC/WBB warm reset alias gating control. Resets to 0.
■ 0 = WMAC and WBB warm resets (bits 1:0 of RST_WARM_CTL) are not aliased by the corresponding bits of PCI_RC when PCI HOST mode is enabled.
■ 1 = WMAC and WBB warm resets (bits 1:0 of RST_WARM_CTL) are aliased by the corresponding bits of PCI_RC when PCI HOST mode is enabled.</td></tr>
<tr><td>23:19</td><td>RES</td><td>Reserved</td></tr>
<tr><td>25:24</td><td></td><td>Current value of the interf_mode_sel pins. Read-only field.</td></tr>
<tr><td>26</td><td></td><td>Current value of the pci_eprm_en_l pin. Read-only field.</td></tr>
<tr><td>31:27</td><td>RES</td><td>Reserved</td></tr>
</table>

3.1.8 Miscellaneous Interrupt Status (RST_MISR)

Offset: 0x0020
Internal Address: 0x1100_0020
PCI Address: 0x1_4020
Access: Read/Write-one-to-clear
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Only bits [7:5] are cleared by a write to this register. To clear the other bits, software must clear the interrupt at the associated interface.

Bit	Bit Name	Description
0		UART interrupt pending. Resets to 0x0.
1		Never asserted in the AR2316. Resets to 0x0.
2		SPI interrupt pending. Resets to 0x0.
3		AHB error interrupt pending. Resets to 0x0.
4		APB error interrupt pending. Resets to 0x0
5		General timer interrupt pending. Resets to 0x0.
6		GPIO interrupt pending. Resets to 0x0.
7		Watchdog timer interrupt pending. Resets to 0x0.
8		Never asserted. Resets to 0x0.
31:9	RES	Reserved

3.1.9 Miscellaneous Interrupt Mask (RST_MIMR)

Offset: 0x0024
Internal Address: 0x1100_0024
PCI Address: 0x1_4024
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		UART interrupt mask. Resets to 0x0.
1	RES	Reserved. Resets to 0x0.
2		SPI interrupt mask. Resets to 0x0.
3		AHB error interrupt mask. Resets to 0x0.
4		APB error interrupt mask. Resets to 0x0.
5		General timer interrupt mask. Resets to 0x0.
6		GPIO interrupt mask. Resets to 0x0.
7		Watchdog timer interrupt mask. Resets to 0x0.
8	RES	Reserved. Resets to 0x0.
31:9	RES	Reserved.

3.1.10 Global Interrupt Status (RST_GISR)

Offset: 0x0028
Internal address: 0x1100_0028
PCI address: 0x1_4028
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: This register cannot be written and does not support read-and-clear access. The only way to clear a bit is to clear the underlying interrupt causing the GISR bit to assert.

Bit	Bit Name	Description
0		Miscellaneous interrupt pending. Indicates that the bitwise logical AND of RST_MISR and RST_MIMR is non-zero. Software must read the RST_MISR to determine which miscellaneous interrupts are pending. Connected to bit [0] of the CPU's SI_Int input.
1		WMAC interrupt pending. Indicates that the WMAC is signaling an interrupt. Software must read the WMAC's interrupt-related registers to determine what WMAC interrupts are pending. Connected to bit [1] of the CPU's SI_Int input.
2	RES	Reserved
3		Local bus/PCI interrupt pending. Indicates that the local bus interface and/or the PCI interface are signaling an interrupt. Because only one interface can be enabled at a time, software must read only the enabled interface's interrupt-related registers to determine what local bus/PCI interrupts are pending. Connected to bit [3] of the CPU's SI_Int input.
4		WMAC poll interrupt pending. Indicates that the WMAC has just received a Poll frame and CPU intervention is required to generate a response frame. Software must read the Poll-related WMAC registers to determine how to proceed. Connected to bit [4] of the CPU's SI_Int input.
5		CPU timer interrupt pending. Indicates that the CPU is asserting its SI_TimerInt output because the CPU's cop0 Count register has reached the value stored in the CPU's cop0 Compare register. Software must rewrite the cop0 Compare register to clear this interrupt (see the MIPS32 documentation for more details). Connected to bit [5] of the CPU's SI_Int input.
6		Ethernet interrupt pending. Indicates that the Ethernet interface is signaling an interrupt. Software must read the Ethernet interface's interrupt-related registers to determine which Ethernet interrupts are pending. Connected to bit [2] of the CPU's SI-Int input.
31:6	RES	Reserved

3.1.11 General Timer (RST_GTIME)

Offset: 0x0030
Internal address: 0x1100_0030
PCI address: 0x1_4030
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Notes: This register decrements every cycle. When its value reaches zero:

- A general timer interrupt is signaled (see bit [5] of the RST_MISR)
- The register is reloaded with the value of the general timer reload register (RST_GTIME_RELOAD)

Bit	Bit Name	Description
31:0		Current value of general timer. Resets to 0x0.

3.1.12 General Timer Reload Value (RST_GTIME_RELOAD)

Offset: 0x0034
Internal address: 0x1100_0034
PCI address: 0x1_4034
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0		Value to be loaded into the general timer register when it reaches zero. Resets to 0x0.

3.1.13 Watchdog Timer (RST_WDOG)

Offset: 0x0038
PCI address: 0x1_4038
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: This register decrements every cycle. When its value reaches zero, a watchdog interrupt is signaled (see bit [7] of RST_MISR)

Bit	Bit Name	Description
31:0		Current value of watchdog timer. Resets to 0x0.

3.1.14 Watchdog Timer Control (RST_WDOG_CTL)

Offset: 0x003C
Internal address: 0x1100_003C
PCI address: 0x1_403C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
1:0	RES	Reserved
2		Enable AHB error signalling upon watchdog expiration. Resets to 0x0. ■ 0 = Do not signal an AHB error (see bit [2] of the RST_AHBERR0 register) when the watchdog timer expires ■ 1 = Signal an AHB error (see bit [2] of the RST_AHBERR0 register) when the watchdog timer expires.
31:3	RES	Reserved

3.1.15 SDR-DRAM Memory Controller Parameters (RST_MEMCTL)

Offset: 0x0040
Internal address: 0x1100_0040
PCI address: 0x1_4040
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		Memory controller remap control. This bit is connected directly to the Synopsys DW_memctl 'remap' input port. See Table 8 on pages 77-78 in the DW_memctl databook for additional details. Resets to 0x0.
1		Memory controller 'power down' control. This bit is connected directly to the Synopsys DW_memctl 'power_down' input port. See Table 8 on pages 77-78 in the DW_memctl databook for additional details. Resets to 0x0.
2		Memory controller clear self-refresh/power-down control. This bit is connected directly to the Synopsys DW_memctl clear_sr_dp input port. See Table 8 on pages 77-78 in the DW_memctl databook for additional details. Resets to 0x0.
3		SDRAM capture clock select. Resets to 0. ■ 0 = Use delayed hclk (i.e., hclk after being delayed by the coarse and fine delay lines) ■ 1 = Use the dram_clk_fb input from off-chip
7:4		Coarse delay line control. This field selects how many coarse delay elements to enable in the DRAM clock delay line that generates the clock used to sample read data returning from the DRAM and drive address/control and write data to the DRAM. Each coarse delay element adds about a 0.4ns delay at nominal PVT. Resets to 0x0.
11:8		Fine delay line control. This field selects how many fine delay elements to enable in the DRAM clock delay line that generates the clock used to sample read data returning from the DRAM and drive address/control and write data to the DRAM. Each fine delay element adds about a 0.1ns delay at nominal PVT. Resets to 0x0.
15:12	RES	Reserved
17:16		Coarse delay phase detector status. This field reports the relative phase between the DRAM clock feedback input from off-chip (the dram_clk_fb pin) and the internally-generated delayed DRAM clock (dram_clk_dly) used to sample/drive the DRAM data and control signals. The relative phase is determined at the granularity of a single coarse delay element. The value of this field is interpreted as follows:

17:16	Meaning
00	dram_clk_dly is delayed by too much relative to sd_clk_fb; need less delay on dram_clk_dly
01	dram_clk_dly is in phase relative to sd_clk_fb; delay on dram_clk_dly is correct
10	dram_clk_dly is 180 degrees out of phase relative to sd_clk_fb; need either more or less delay on dram_clk_dly
11	dram_clk_dly is delayed by too little relative to sd_clk_fb; need more delay on dram_clk_dly

19:18		Fine delay phase detector status. This field reports the relative phase between the DRAM clock feedback input from off-chip (the sd_clk_fb pin) and the internally-generated delayed DRAM clock (dram_clk_dly) used to sample/drive the DRAM data and control signals. The relative phase is determined at the granularity of a single fine delay element. The value of this field is interpreted in the same manner as for the coarse delay phase detector status field.
31:20	RES	Reserved

3.1.16 CPU Performance Counter Control (RST_CPUPERF_CTL)

Offset: 0x0044
Internal address: 0x1100_0044
PCI address: 0x1_4044
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
3:0		Performance counter 0 event select. This field determines the event counted by performance counter 0. Resets to 0x0.
7:4		Performance counter 1 event select. This field determines the event counted by performance counter 1. Uses the same encodings as specified in bits [3:0] of this register for performance counter 0. Resets to 0x3.
8		Performance counter pause. Resets to 0x0. ■ 0 = Both performance counters run normally ■ 1 = Both performance counters hold their values
31:9	RES	Reserved

Value	Event
0	Clock cycles
1	Write buffer pushes without merge
2	Write buffer pushes with merge
3	Instruction completions
4	Instruction cache misses
5	Instruction cache hits
6	Data cache misses
7	Data cache hits
8–15	Reserved

3.1.17 CPU Performance Counter 0 (RST_CPUPERF_0)

Offset: 0x0048
Internal address: 0x1100_0048
PCI address: 0x1_4048
Access: Read-and-clear/no write access
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: When either CPU performance counter reaches its maximum value, both counters are shifted right by one bit (i.e., divided by 2).

Bit	Bit Name	Description
31:0		Current value of performance counter 0. Read-and-clear access. Resets to 0x0.

3.1.18 CPU Performance Counter 1 (RST_CPUPERF_1)

Offset: 0x004C
Internal address: 0x1100_004C
PCI address: 0x1_404C
Access: Read-and-clear/no write access
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: When either CPU performance counter reaches its maximum value, both counters shift right by one bit (i.e., divide by two).

Bit	Bit Name	Description
31:0		Current value of performance counter 1. Read-and-clear access. Resets to 0x0.

3.1.19 AHB Error Status Register 0 (RST_AHBERR0)

Offset: 0x0050
Internal address: 0x1100_0050
PCI address: 0x1_4050
Access: Special (See field descriptions)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		AHB error indication. Resets to 0x0. Read: ■ 0 = No AHB error has been detected ■ 1 = An AHB error has been detected; other AHB error registers provide more details. Write: ■ 0 = No effect ■ 1 = Clears all bits in this register
1		AHB error overflow indication. Resets to 0x0. Read: ■ 0 = If bit [0] is set, then an AHB error has been detected. However, no additional AHB errors have occurred since detecting and capturing the original error. ■ 1 = An AHB error has been detected, and one or more additional AHB errors were detected before software processed the first error. Writes have no effect.
2		AHB error due to watchdog timer expiration indication. Resets to 0x0. Read: ■ 0 = If bit [0] is set, then an AHB error has been detected and this error was caused by an explicit ERROR response code being observed on the AHB hresp signal. ■ 1 = An AHB error is detected, but the error was implied by watchdog timer expiration rather than by an explicit AHB hresp ERROR response. Probably the AHB bus is hung, as no response is observed on the AHB bus and the watchdog timer eventually expires. Writes have no effect.
31:3	RES	Reserved

3.1.20 AHB Error Status Register 1 (RST_AHBERR1)

Internal address: 0x1100_0054
PCI address: 0x1_4054
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0		AHB address (haddr) for which the error occurred

3.1.21 AHB Error Status Register 2 (RST_AHBERR2)

Offset: 0x0058
Internal address: 0x1100_0058
PCI address: 0x1_4058
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0		AHB write data (hwdata) present when the error occurred

3.1.22 AHB Error Status Register 3 (RST_AHBERR3)

Offset: 0x005C
Internal address: 0x1100_005C
PCI address: 0x1_405C
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0		AHB read data (hrdata) present when the error occurred

3.1.23 AHB Error Status Register 4 (RST_AHBERR4)

Offset: 0x0060
Internal address: 0x1100_0060
PCI address: 0x1_4060
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
3:0		AHB bus master (hmaster) when the error occurred ■ 0 = Default bus master ■ 1 = WMAC ■ 2 = Ethernet ■ 3 = PCI Tx/Rx endpoints ■ 4 = Local bus ■ 5 = CPU ■ 6 = PCI target interface ■ 7–15 = Undefined
4		AHB write indication (hwrite) when the error occurred ■ 0 = Transaction was a read ■ 1 = Transaction was a write
6:5		AHB transaction size (hsize) when the error occurred ■ 0 = Byte ■ 1 = Halfword ■ 2 = Word ■ 3 = Reserved
8:7		AHB transaction type (htrans) when the error occurred ■ 0 = Idle ■ 1 = Busy [not used in the AR2316] ■ 2 = Non-sequential address ■ 3 = Sequential address
11:9		AHB burst type (hburst) when the error occurred ■ 0 = Single beat ■ 1 = Incrementing, unspecified length ■ 2 = WRAP4 ■ 3 = INCR4
31:12	RES	Reserved

3.1.24 CPU/AHB/APB PLL (PLLc) Control (RST_PLLC_CTL)

Offset: 0x0064
Internal address: 0x1100_0064
PCI address: 0x1_4064
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
1:0		Reference divider value. Connects to the Malta refdivc[1:0] input. Resets to 0. ■ 0 = Sets the value of the PLL 'refdiv' parameter to 1 ■ 1 = Sets the value of the PLL 'refdiv' parameter to 2 ■ 2 = Sets the value of the PLL 'refdiv' parameter to 4 ■ 3 = Sets the value of the PLL 'refdiv' parameter to 5
3:2		Feedback divider value. Connects to the Malta divc[4:0] input. Because this field specifies the divider value on the feedback path of the PLL, it effectively controls the frequency multiplication performed on the output of the divided-down reference clock. Resets to 25. ■ 0–3 = Reserved ■ 4–31 = Sets the value of the PLL div parameter to the specified value
7		Additional feedback divide-by-2 enable. Connects to the Malta divc[5] input. Resets to 0. ■ 0 = Sets the value of the PLL divby2 parameter to 0 (i.e., enables an additional divide-by-2 in the feedback path) ■ 1 = Sets the value of the PLL divby2 parameter to 1 (i.e., enables an additional divide-by-4 in the feedback path)
13:8	RES	Reserved
16:14		clkc final divider select. Bit [2] connects to the Malta dutycycle50 input. Bits [1:0] connect to the Malta cpu_div[1:0] input. Resets to 3. ■ 0 = clkc output frequency equal to the PLL output frequency divided by 2 ■ 1 = clkc output frequency equal to the PLL output frequency divided by 3 (with an unequal duty cycle) ■ 2 = clkc output frequency equal to the PLL output frequency divided by 4 ■ 3 = clkc output frequency equal to the PLL output frequency divided by 6 ■ 4 = clkc output frequency equal to the PLL output frequency divided by 3, with a 50% duty cycle ■ 5–7 = Reserved
18:17	RES	Reserved
19		Power-down enable. Connects to the Malta pllcpwd input. Resets to 0. ■ 0 = PLLc operates normally ■ 1 = PLLc is powered down and must not be used as a clock source
22:20		clkm final divider select. Bit [2] connects to the Malta dutycycle50_mem input. Bits [1:0] connect to the Malta mem_div[1:0] input. Resets to 3. ■ 0 = clkm output frequency equal to the PLL output frequency divided by 2 ■ 1= clkm output frequency equal to the PLL output frequency divided by 3 (with an unequal duty cycle) ■ 2 = clkm output frequency equal to the PLL output frequency divided by 4 ■ 3 = clkm output frequency equal to the PLL output frequency divided by 6 ■ 4 = clkm output frequency equal to the PLL output frequency divided by 3, with a 50% duty cycle ■ 5–7 = Reserved
31:23	RES	Reserved

3.1.25 CPU Final Clock MUX/Divider Control (RST_CPUCLK_CTL)

Offset: 0x006C
Internal address: 0x1100_006C
PCI address: 0x1_406C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: The output of this register drives the proc_clk signal. This signal clocks the MIPS CPU (via SI_ClkIn) as well as the related ec2ahb logic.

Bit	Bit Name	Description
1:0		Input clock select. Resets to 3. ■ 0 = Use PLLc's clkm as input ■ 1 = Use PLLc's clkm as input ■ 2 = Use PLLc's clkc as input ■ 3 = Use the raw ref_clk as input
3:2		CPU clock divider select. Resets to 0. ■ 0 = CPU clock frequency is equal to the input clock frequency ■ 1 = CPU clock frequency is equal to the input clock frequency divided by 2 ■ 2 = CPU clock frequency is equal to the input clock frequency divided by 4 ■ 3 = CPU clock frequency is equal to the input clock frequency divided by 6
31:4	RES	Reserved

3.1.26 AHB/APB Final Clock MUX/Divider Control (RST_AMBACLK_CTL)

Offset: 0x0070
Internal address: 0x1100_0070
PCI address: 0x1_4070
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: The output of this register drives the hclk, pclk, and dram_clk signals, which clock the AHB and APB busses, the SDRAM, and all related logic.

Bit	Bit Name	Description
1:0		Input clock select. Resets to 3. ■ 0 = Use PLLc's clkm as input ■ 1 = Use PLLc's clkm as input ■ 2 = Use PLLc's clkc as input ■ 3 = Use the raw ref_clk as input
3:2		AHB/APB clock divider select. Resets to 0. ■ 0 = AHB/APB clock frequency equal to the input clock frequency ■ 1 = AHB/APB clock frequency equal to the input clock frequency/2 ■ 2 = AHB/APB clock frequency equal to the input clock frequency/4 ■ 3 = AHB/APB clock frequency equal to the input clock frequency/6
31:4	RES	Reserved

3.1.27 Video Sync. Final Clock MUX/Divider Control (RST_SYNCCLK_CTL)

Offset: 0x0074
Internal address: 0x1100_0074
PCI address: 0x1_4074
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Notes: This register output controls the sync_clk signal, which clocks the video synchronization logic and is sent off-chip.

NOTE: Logic using this clock is not meant to be used in the AR2316.

Bit	Bit Name	Description
1:0		Input clock select. Resets to 3. ■ 0 = Use PLLc's clkm as input ■ 1 = Use PLLc's clkm as input ■ 2 = Use PLLc's clkc as input ■ 3 = Use the raw ref_clk as input
3:2		Video synchronization clock divider select. Resets to 0. ■ 0 = Video synchronization clock freq. equal to the input clock frequency ■ 1 = Video synchronization clock freq. equal to the input clock frequency/2 ■ 2 = Video synchronization clock freq. equal to the input clock frequency/4 ■ 3 = Video synchronization clock freq. equal to the input clock frequency/6
31:4	RES	Reserved

3.1.28 DSL Sleep Control (RST_DSL_SLEEP_CTL)

Offset: 0x0080
Internal address: 0x1100_0080
PCI address: 0x1_4080
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		Sleep enable. Resets to 0x0. Read: ■ 0 = DSL is awake ■ 1 = DSL is asleep Write: ■ 0 = No effect ■ 1 = Causes DSL to enter sleep (i.e., power-down) mode for a duration specified by the DSL sleep duration register.
3:1	RES	Reserved
4		CPU clock gating control. This bit controls whether the CPU clock is gated off during DSL sleep. Resets to 0x0. ■ 0 = CPU clock runs during DSL sleep ■ 1 = CPU clock is gated off (i.e., stops) during DSL sleep
5		AMBA clock gating control. This bit controls whether the AHB, APB, and SDRAM clocks are gated off during DSL sleep. Resets to 0x0. ■ 0 = AMBA clocks run during DSL sleep ■ 1 = AMBA clocks are gated off (i.e., stop) during DSL sleep
6		Video synchronization clock gating control. This bit controls whether the video synchronization clock is gated off during DSL sleep. Resets to 0x0. ■ 0 = Video synchronization clock runs during DSL sleep ■ 1 = Video synchronization clock is gated off (i.e., stops) during DSL sleep
7		CPU/AMBA PLL power-down control. This bit controls whether the CPU/AMBA PLL ('PLLc') is powered down during DSL sleep. Resets to 0x0. ■ 0 = PLLc remains powered up during DSL sleep ■ 1 = PLLc is powered down during DSL sleep
31:8	RES	Reserved

3.1.29 DSL Sleep Duration (RST_DSL_SLEEP_DUR)

Offset: 0x0084
Internal address: 0x1100_0084
PCI address: 0x1_4084
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0		Specifies, in units of reference clock (ref_clk) periods (typically 40 MHz/25 ns), how long DSL logic sleeps (i.e., powers down) when next enabled using bit [0] of the "DSL Sleep Control (RST_DSL_SLEEP_CTL)" register. Resets to an undefined value.

3.1.30 GPIO Input, Set 0 (RST_GPIOIN0)

Offset: 0x0088
Internal Address: 0x1100_0088
PCI Address: 0x1_4088
Access: Read-only
Cold reset: Unaffected
Warm reset: Unaffected

Bit	Bit Name	Description
22:0		Current value of the gpio_in[22:0] signals
31:23	RES	Reserved

3.1.31 GPIO Output, Set 0 (RST_GPIOOUT0)

Offset: 0x0090
Internal Address: 0x1100_0090
PCI Address: 0x1_4090
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
22:0		Value to drive on the gpio_out[22:0] signals. Resets to 0x0.
31:23	RES	Reserved

3.1.32 GPIO Direction, Set 0 (RST_GPIODIR0)

Offset: 0x0098
Internal Address: 0x1100_0098
PCI Address: 0x1_4098
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		Direction for GPIO[0]. Resets to 0x0. ■ 0 = GPIO[0] is an input ■ 1 = GPIO[0] is an output
1		Direction for GPIO[1]. Resets to 0x0. ■ 0 = GPIO[1] is an input ■ 1 = GPIO[1] is an output
...	...	...
22		Direction for GPIO[22]. Resets to 0x0. ■ 0 = GPIO[22] is an input ■ 1 = GPIO[22] is an output
31:23	RES	Reserved

3.1.33 GPIO Interrupt Control (RST_GPIOINTR)

Offset: 0x00A0
Internal address: 0x1100_00A0
PCI address: 0x1_40A0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
5:0		GPIO input select 0. This field selects the first GPIO pin to test for GPIO interrupt assertion. Values of 0-22 are valid. Resets to 0.
7:6		GPIO test select 0. This field determines how the pin selected by bits [5:0] of this register is tested to determine if a GPIO interrupt is signaled. Resets to 0. ■ 0 = Pin never generates a GPIO interrupt ■ 1 = GPIO interrupt generated when pin is low ■ 2 = GPIO interrupt generated when pin is high ■ 3 = GPIO interrupt generated when pin changes state (high-to-low or low-to-high)
13:8		GPIO input select 1. This field selects the second GPIO pin to test for GPIO interrupt assertion. Values from 0-22 are valid. Resets to 0.
15:14		GPIO test select 1. This field determines how the pin selected by bits [13:8] of this register is tested to determine if a GPIO interrupt is signaled. Resets to 0. ■ 0 = Pin never generates a GPIO interrupt ■ 1 = GPIO interrupt generated when pin is low ■ 2 = GPIO interrupt generated when pin is high ■ 3 = GPIO interrupt generated when pin changes state (high-to-low or low-to-high)
31:16	RES	Reserved

3.1.34 PCI Final Clock MUX/Divider Control (RST_PCICLK_CTL)

Offset: 0x00A4
Internal Address: 0x1100_00A0
PCI Address: 0x1_40A0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
5:0		GPIO input select 0. This field selects the first GPIO pin to test for GPIO interrupt assertion. Values from 0-22 are valid. Resets to 0.
7:6		GPIO test select 0. This field determines how the pin selected by bits [5:0] tested to determine if a GPIO interrupt is signaled. Resets to 0. ■ 0 = Pin never generates a GPIO interrupt ■ 1 = GPIO interrupt generated when pin is low ■ 2 = GPIO interrupt generated when pin is high ■ 3 = GPIO interrupt generated when pin changes state (high-to-low or low-to-high)
13:8		GPIO input select 1. This field selects the second GPIO pin to test for GPIO interrupt assertion. Values from 0–22 are valid. Resets to 0.
15:14		GPIO test select 1. This field determines how the pin selected by bits [13:8] of this register is tested to determine if a GPIO interrupt is signaled. Resets to 0. ■ 0 = Pin never generates a GPIO interrupt ■ 1 = GPIO interrupt generated when pin is low ■ 2 = GPIO interrupt generated when pin is high ■ 3 = GPIO interrupt generated when pin changes state (high-to-low or low-to-high)
31:16	RES	Reserved

3.1.35 Scratch Register 0 (RST_SCRATCH0)

Offset: 0x00A8
Internal address: 0x1100_00A8
PCI address: 0x1_40A8
Access: Read/Write
Cold reset: Unaffected
Warm reset: Unaffected
Notes: For software use

Bit	Bit Name	Description
31:0		Scratch register value. Unaffected by any reset.

3.1.36 Scratch Register 1 (RST_SCRATCH1)

Offset: 0x00AC
Internal address: 0x1100_00AC
PCI address: 0x1_40AC
Access: Read/Write
Cold reset: Unaffected
Warm reset: Unaffected
Notes: For software use

Bit	Bit Name	Description
31:0		Scratch register value. Unaffected by any reset.

3.1.37 Observation Control (RST_OBS_CTL)

Offset: 0x00B0
Internal address: 0x1100_00B0
PCI address: 0x1_40B0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		Observation mode control. Resets to 0. ■ 0 = Observation mode disabled ■ 1 = Observation mode enabled
3:1		Output select control. Resets to 0. ■ 0 = Select DSL observation bus ■ 1 = Select ADC observation bus ■ 2 = Select DAC observation bus ■ 3 = Select WMAC observation bus ■ 4 = Select ENET observation bus ■ 5–7 = Reserved
4		Observation bus direction control. Resets to 0. ■ 0 = Observation bus is an output bus ■ 1 = Observation bus is an input bus
5		RF mode control. Resets to 0. ■ 0 = RF mode disabled ■ 1 = RF mode enabled (Flash pins and GPIO's 0–3 become RFxxx pins)
7:6	RES	Reserved
8		Secondary observation bus enable. Resets to 0. ■ 0 = GPIO's [22:8,6,2:1] used as GPIO's ■ 1 = GPIO's [22:8,6,2:1] used as a secondary observation bus

Bit	Bit Name	Description
11:9		Secondary observation bus control. Resets to 0. ■ 0 = Select DSL observation bus ■ 1 = Select ADC observation bus ■ 2 = Select DAC observation bus ■ 3 = Select WMAC observation bus ■ 4 = Select ENET observation bus ■ 5–7 = Reserved
12		Clkobs/GPIO[0] control. Resets to 0. ■ 0 = GPIO[0] used as a GPIO ■ 1 = GPIO[0] used to output Clkobs
14:13		Rx_Clear/Clkc/GPIO[3] control. Resets to 0. ■ 0 = GPIO[3] used as GPIO ■ 1 = GPIO[3] used to output Rx_Clear ■ 2 = GPIO[3] used to output clkc ■ 3 = Reserved
15		LED[0]/GPIO[1] control. Resets to 0. ■ 0 = GPIO[1] used as a GPIO ■ 1 = GPIO[1] used to output LED[0]. This bit has priority over bit 8.
16		LED[1]/GPIO[2] control. Resets to 0. ■ 0 = GPIO[2] used as a GPIO ■ 1 = GPIO[2] used to output LED[1]. This bit has priority over bit 8.
17		Tsttrig/GPIO[6] control. Resets to 0. ■ 0 = GPIO[6] used as a GPIO ■ 1 = GPIO[6] used to output tsttrig. This bit has priority over bit 8.
18		BTActive/GPIO[7] control. Resets to 0. ■ 0 = GPIO[7] used as a GPIO ■ 1 = GPIO[7] used as the BTActive input
19		PCI mode control. Resets to 0. ■ 0 = PCI pads are in PCI mode ■ 1 = PCI pads are in Cardbus mode
31:20	RES	Reserved

3.1.38 General Clock Control (RST_MISCCLK_CTL)

Offset: 0x00B4
Internal address: 0x1100_00B4
PCI address: 0x1_40B4
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		pllbypass. Resets to 1. ■ 0 = pllbypass disabled ■ 1 = pllbypass enabled
1		proc_clk_sel. Resets to 0. ■ 0 = ref_clk is really the source of ref_clk referred to in the description of register RST_CPUCLK_CTL ■ 1 = the external proc_ref_clk is the source of ref_clk referred to in the description of register RST_CPUCLK_CTL
31:2	RES	Reserved

3.1.39 Client Interrupt Mask (RST_CIMR)

Offset: 0x00B8
Internal address: 0x1100_00B8
PCI address: 0x1_40B8
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Unlike the other interrupt mask registers, all bits in this register reset to 1 rather than to 0.

Bit	Bit Name	Description
0		Miscellaneous interrupt pending mask. Resets to 1.
1		WMAC interrupt pending mask. Resets to 1.
2		Ethernet interrupt pending mask. Resets to 1.
3		Local bus/PCI interrupt pending mask. Resets to 1.
4		WMAC poll interrupt pending mask. Resets to 1.
5		CPU timer interrupt pending mask. Resets to 1.
31:6	RES	Reserved

3.1.40 PLL Programming Notes

The DSL contains one PLL (PLLc), which generates the CPU clock, the AHB/APB clock, and the SDRAM clock. The PLL takes as input the 40 MHz reference clock (ref_clk), which proceeds through three conceptual stages.

After the PLL itself, an additional divider stage takes the vcoout output from the PLL and divides it for use in the rest of the system. PLLc vcoout output is fed into two dividers to yield two outputs, clkm and clkc. See Figure 3-1.'

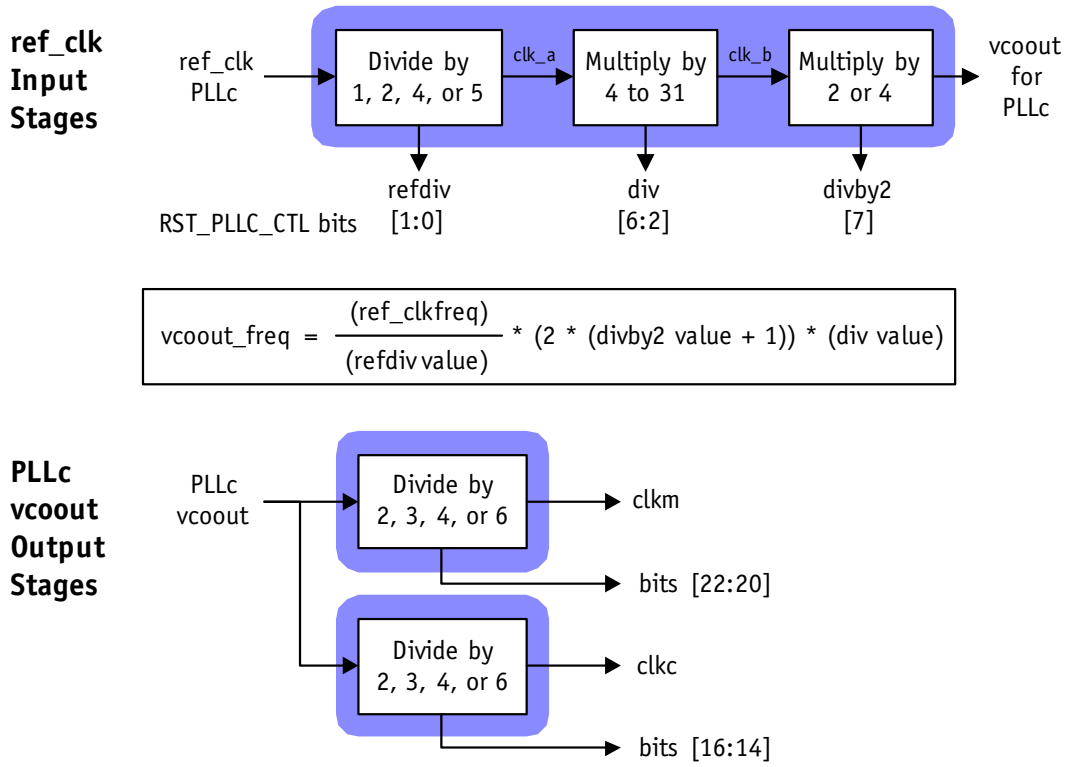


Figure 3-1. **Ref_clk and PLLc vcoout Stages**

From the PLL, the clkc and clkm outputs feed into an additional set of clock MUXes/dividers to generate the on-chip clocks. For all clocks except the PCI clock, each final MUX/divide module is identical. See Figure 3-2.

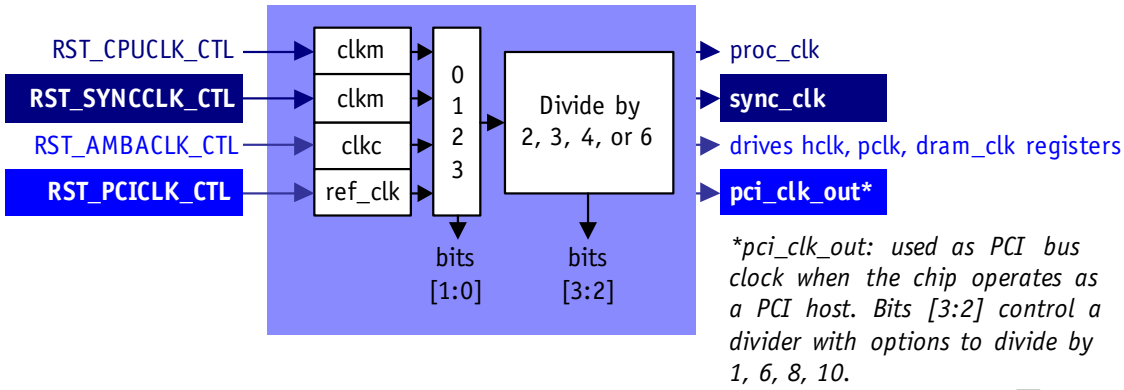


Figure 3-2. **Final Clock Divider**

3.2 SDR-DRAM Controller Registers

Table 3-2 summarizes the SDR-DRAM registers for the AR2316. These registers use:

- Internal base address: 0x1030_0000
- External PCI MBAR_0 base offset: 0x1_2000

Table 3-2. **SDR-DRAM Register Summary**

Offset	Name	Description	Page
0x0000	MEMCTL_SCONR	SDR-DRAM configuration register	page 42
0x0004	MEMCTL_STMG0R	SDR-DRAM timing register 0	page 43
0x0008	MEMCTL_STMG1R	SDR-DRAM timing register 1	page 44
0x000C	MEMCTL_SCTLR	SDR-DRAM control register	page 45
0x0010	MEMCTL_SREFR	SDR-DRAM refresh interval register	page 45

3.2.1 SDR-DRAM Configuration Register (MEMCTL_SCONR)

Offset: 0x0000
Internal address: 0x1030_0000
PCI address: 0x1_2000
Access: Read/Write
Warm reset: Unaffected

Bit	Bit Name	Description
2:0	RES	Reserved
4:3	S_BANK_ADDR _WIDTH	Specifies the number of bank address bits. ■ 0–3 = Correspond to 1–4 bits (thus select 2–16 banks) This value should be less than or equal to the MAX_S_BANK_ADDR_WIDTH compile-time parameter. If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify the bank address width of the SDRAM only.
8:5	S_ROW_ADDR _WIDTH	Specifies the number of address bits for the row address: ■ 10–15 = Correspond to 11–16 bits ■ 0–10= Reserved This value should be less than or equal to the MAX_S_ROW_ADDR_WIDTH compile-time parameter. If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify the row address width of the SDRAM only.

Bit	Bit Name	Description
12:9	S_COL_ADDR _WIDTH	Specifies the number of address bits for the column address: ■ 15 = Reserved ■ 7–14= Correspond to 8–15 bits ■ 0–6 = Reserved This value should be less than or equal to the MAX_S_ROW_ADDR_WIDTH compile-time parameter. If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify the column address width of the SDRAM only.
14:13	S_DATA_WIDTH	Specifies SDRAM data width in bits for DDR_SDRAM: ■ 00 = 8 bits ■ 01 = 16 bits ■ 10 = 32 bits ■ 11 = 64 Bits For all other SDRAMs, ■ 00 = 16 bits ■ 01 = 32 bits ■ 10 = 64 bits ■ 11 = 128 bits
17:15	S_SA	Serial presence detect address bits
18	S_SCL	Clock for serial presence detect logic
19	S_SD	Bi-directional data for serial presence detect (SPD) logic; data written into bit goes in as SPD data. During reads to this register, the bit represents data read back from SPD logic.
20	S_SDA_OE_N	Output enable for bi-directional data pin for I^2C SPD logic ■ 1 = Data written to bit [19] ■ 0 = Programs for data reads
31:21	RES	Reserved

3.2.2 SSDR-DRAM Timing Register 0 (MEMCTL_STMGOR)

PCI address: 0x1_2004
Access: Read/Write
Warm reset: Unaffected

Offset: 0x0004
Internal address: 0x1030_0004

Bit	Bit Name	Description
1:0	CAS_LATENCY	Delay in clock cycles between read command and availability of first data. Bit 26 is unused when VER_1_2A_COMPATIABLE_MODE is set to 1. ■ 0 = 1 clock ■ 1 = 2 clocks ■ 2 = 3 clocks ■ 3 = 4 clocks ■ 4 = 1.5 clocks (DDR only) ■ 5 = 2.5 clocks (DDR only) ■ 6:7 + reserved If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify the CAS_LATENCY timing value of SDRAM only.
5:2	T_RAS_MIN	Minimum delay between active and precharge commands. Values of 0–15 correspond to T_RAS_MIN of 1-16 clocks.
8:7	T_RCD	Minimum delay between active and read/write commands. Values 0–7 correspond to T_RCD values of 1–8 clocks.
11:9	T_RP	Precharge period. Values of 0–7 correspond to T_RP of 1–8 clocks.
13:12	T_WR	For writes, delay from last data in to next precharge command. Values 0–3 correspond to T_WR of 1–4 clocks.

Bit	Bit Name	Description
17:14	T_RCAR	Auto-refresh period. Minimum time between two auto-refresh commands. Values 0–15 correspond to T_RCAR of 1-16 clocks. If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify T_RCAR timing value of SDRAM only.
21:18	T_XSR	Exits self-refresh to active or auto-refresh command time. Minimum time controller should wait after taking SDRAM out of self-refresh mode before issuing any active or auto-refresh commands. Values of 1–512 correspond to T_XSR of 1–512 clocks. Not valid for SYNC-FLASH.
25:22	T_RC	Specifies the active-to-active command period. Values of 0–15 correspond to the T_RC of 1–16 clocks. If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify the T_RC timing value of SDRAM only
26	CAS_LATENCY / EXTENDED_CAS _LATENCY	Delay in clock cycles between read command and availability of first data. Bit 26 is unused when VER_1_2A_COMPATIABLE_MODE is set to 1. ■ 0 = 1 clock ■ 1 = 2 clocks ■ 2 = 3 clocks ■ 3 = 4 clocks ■ 4 = 1.5 clocks (DDR only) ■ 5 = 2.5 clocks (DDR only) ■ 6:7 + reserved If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify the CAS_LATENCY timing value of SDRAM only.
31:27	T_XSR / EXTENDED_T_XSR	Exits self-refresh to active or auto-refresh command time. Minimum time controller should wait after taking SDRAM out of self-refresh mode before issuing any active or auto-refresh commands. Values of 1–512 correspond to T_XSR of 1–512 clocks. Not valid for SYNC-FLASH. Bits 31:27 unused when VER_1_2A_COMPATIABLE_MODE set to 1.

3.2.3 SDR-DRAM Timing Register 1 (MEMCTL_STMG1R)

PCI address: 0x1_2008
Access: Read/Write
Warm reset: Unaffected

Offset: 0x0008
Internal address: 0x1030_0008

Bit	Bit Name	Description
15:0	T_INIT	Specifies the number of clock cycles to hold SDRAM inputs stable after power up, before issuing any commands. If DW_memctl controls a SyncFlash, these bits are used for the SyncFlash TRPDR timing value. This SyncFlash resets or powers down high to read/write delay. Values correspond to S_RP_N high to read/write delay minus one. If DW_memctl controls both SyncFlash and SDR-SDRAM or Mobile-SDRAM (DYNAMIC_RAM_TYPE = 4 or 5), these bits specify the both SDRAM initialization time and SyncFlash TRPDR timing value.
19:16	NUM_INIT_REF	Specifies the number of auto-refreshes during initialization. Values of 0–15 correspond to 1–16 auto-refreshes.
21:20	T_WTR	Specifies the internal write-to-read delay for DDR-SDRAMs. Values of 1–4 represent 1–4 clocks delay.
31:22	RES	Reserved

3.2.4 SDR-DRAM Control Register (MEMCTL_SCTLR)

PCI address: 0x1_200C
Access: Read/Write
Warm reset: Unaffected

Offset: 0x000C
Internal address: 0x1030_000C

Bit	Bit Name	Description
0	INITIALIZE	Forces DW_MEMCTL to initialize the SDRAM. DW_MEMCTL resets this bit to 0 once the initialization sequence completes.
1	SELF_REFRESH / DEEP_POWER_MODE	Forces DW_MEMCTL to put the SDRAM in self-refresh mode (deep-power down mode for SyncFlash). Bit can clear after writing to this bit or with the CLEAR_SR_DP pin, generated by external power management unit.
2	POWER_DOWN _MODE	Forces DW_MEMCTL to put the SDRAM in power-down mode.
3	PRECHARGE _ALGORITHM	Determines when a row is precharged: ■ 1 = Delayed precharge; the row stays open after read/write operations ■ 0 = Immediate precharge; the row precharges after read/write operation
4	FULL_REFRESH _BEFORE_SR	Controls the number of refreshes done by DW_MEMCTL before the SDRAM is put into self-refresh mode: ■ 1 = Refresh all rows before entering self-refresh mode ■ 0 = Refresh only one row before entering self-refresh mode
5	FULL_REFRESH _AFTER_SR	Controls the number of refreshes done by DW_MEMCTL after the SDRAM is taken out of self-refresh mode: ■ 1 = Refresh all rows before entering self-refresh mode ■ 0 = Refresh only one row before entering self-refresh mode
8:6[1]	READ_PIPE	Indicates the number of registers inserted in the read data path for the SDRAM to correctly latch data. Values of 0–7 indicate 0–7 registers.
9[1]	SET_MODE_REG	If set to 1, forces controller to update the SDRAM mode register. The controller clears this bit once it has finished updating the mode register.
10[1]	SYNC_FLASH_SOFT_ SEQ	Specifies type of command sequences used for SyncFlash operations: ■ 1 = Software Command Sequence (SCS) ■ 0 = Hardware Command Sequence (HCS)
11[1]	SELF_REFRESH _STATUS	Read only. If set to 1, indicates the SDRAM is in self-refresh mode. If self_refresh/deep_power_mode bit (SCTLR bit 1) is set, it may take time before SDRAM enters self-refresh mode, depending on whether all or one row refreshes before entering as defined by the bit FULL_REFRESH_BEFORE_SR. Ensure this bit is set before gating clock in self-refresh mode.
16:12[1]	NUM_OPEN_BANKS	Specifies the number of SDRAM internal banks to be open at any time. Values of 0–15 correspond to 0–15 banks open.
17[1]	S_RD_READY_MODE	SDRAM read-data-ready mode. If set to 1, indicates the SDRAM read data is sampled after S_RD_READY goes active.
18[1]	EXN_MODE_REG _UPDATE	Commands the controller to update the Mobile-SDRAM extended-mode register. Once the update is done, the controller automatically clears the bit.
31:19	RES	Reserved

[1]Bit unused when VER_1_2A_COMPATIABLE_MODE = 1

3.2.5 SDR-DRAM Refresh Interval Register (MEMCTL_SREFR)

PCI address: 0x1_2010
Access: Read/Write
Warm reset: Unaffected

Offset: 0x0010
Internal address: 0x1030_0010

Bit	Bit Name	Description
15:0	T_REF	Specifies the number of clock cycles between consecutive refresh cycles.
23:16	GPO	General purpose output signals.
31:24	GPI	General purpose input signals. If VER_1_2A_COMPATIABLE_MODE is set to 1, the enabled mode Static memory controller connects status bits from FLASH memory to GPI bits [2:0] (three GPI bits used for FLASH status because three separate FLASH memories can connect to DW_MEMCTL).

3.3 UART Registers

Table 3-3 summarizes the UART registers for the AR2316. These registers use:

- Internal base address: 0x1110_0000
- External PCI MBAR_0 base offset: 0x1_5000

Table 3-3. **UART Register Summary**

Offset	Name	Description	Page
0x0000	UART_RBR	Receive buffer	page 46
	UART_THR	Transmit holding	page 46
	UART_DLL	Divisor latch low	page 46
0x0004	UART_IER	Interrupt enable	page 46
	UART_DLH	Divisor latch high	page 46
0x0008	UART_IIR	Interrupt identity	page 47
	UART_FCR	FIFO control	page 47
0x000C	UART_LCR	Line control	page 47
0x0010	UART_MCR	Modem control	page 48
0x0014	UART_LSR	Line status	page 48
0x0018	UART_MSR	Modem status	page 49
0x001C	UART_SCR	Scratch	page 49

3.3.1 Receive Buffer Register (UART_RBR); Transmit Holding Register (UART_THR); Divisor Latch Low Register (UART_DLL)

Offset: 0x0000
Internal address: 0x1110_0000
PCI address: 0x1_5000
Access: (Varies)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
7:0	Address	Specifies address of receive buffer 0. This must be word aligned.
31:8	RES	Reserved

3.3.2 Interrupt Enable Register (UART_IER); Divisor Latch High (UART_DLH)

Offset: 0x0004
Internal address: 0x1110_0004
PCI address: 0x1_5004
Access: (Varies)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
7:0		The UART_DLH register with DLL forms a 16-bit, read/write, Divisor Latch register that contains the UART baud rate divisor. It is accessed by first setting DLAB bit [7] in the "Line Control Register (UART_LCR)". The output baud rate is: baud = (clock frequency)/(16 * divisor) UART_IER is a read/write register containing bits that enable generation of interrupts: ■ Enable Received Data Available (ERBFI) ■ Enable Transmitter Holding Register Empty (ETBEI) ■ Enable Receive Line Status (ELSI) ■ Enable Modem Status (EDSSI)
31:8	RES	Reserved

3.3.3 Interrupt Identity Register (UART_IIR); FIFO Control Register (UART_FCR)

Offset: 0x0008
Internal address: 0x1110_0008
PCI address: 0x1_5008
Access: (Varies)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
7:0		This is a read-only register that identifies the source of an interrupt. Table 3-4 summarizes details of interrupt operation
31:8	RES	Reserved

Table 3-4. **UART Interrupt Control Functions**

Identification Register			Interrupt Set and Reset Function			
Bit 2	Bit 1	Bit 0	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading line status register
1	0	0	Second	Received data available	Receiver data available or read data FIFO trigger level reached	Reading receiver buffer register or the FIFO drops below the trigger level
0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading IIR register (if source of interrupt) or writing into THR
0	0	0	Fourth	MODEM status	Clear to send, data set ready, ring indicator, or data center detect	Reading MODEM status register

3.3.4 Line Control Register (UART_LCR)

Offset: 0x000C
Internal address: 0x1110_000C
PCI address: 0x1_500C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
1–0	CLS	Controls the number of bits per character in each transmitted or received serial character.
2	STOP	Controls the number of stop bits in each transmitted or received serial character.
3	PEN	Parity Enable. When set, parity is enabled.
4	EPS	Even Parity Select. If parity is enabled, this bit selects between even and odd parity. If set to a logic 1, an even number of logic 1s is transmitted or checked. If set to a logic 0, an odd number of logic 1s is transmitted or checked.
5	Stick Parity	Not Used.
6	Break	Setting this bit sends a break signal by holding the sout line low (when not in Loopback Mode, as determined by "Modem Control Register (UART_MCR)" bit 4, until the Break bit clears. In Loopback Mode, the break condition is internally looped back to the receiver.
7	DLAB	Divisor Latch Access. Setting this bit enables reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup to access other registers.
31:8	RES	Reserved

3.3.5 Modem Control Register (UART_MCR)

Offset: 0x0010
Internal address: 0x1110_0010
PCI address: 0x1_5010
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0	DTR	Drives UART output DTR_L
1	RTS	Drives UART output RTS_L
2	OUT 1	Drives UART output U0_OUT1_L
3	OUT 2	Drives UART output U0_OUT2_L
4	LOOPBACK	When set, data on the sout line is held HIGH, while serial data output loops back to the S-in line, internally. In this mode all interrupts are fully functional.
7–5	RES	Must be filled with 0
31:8	RES	Reserved

3.3.6 Line Status Register (UART_LSR)

Offset: 0x0014
Internal address: 0x1110_0014
PCI address: 0x1_5014
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0	DR	Data Ready. When set, this bit indicates the receiver contains at least one character in the RBR. This bit is cleared when the RBR is read.
1	OE	Overrun Bit. When set, this bit indicates an overrun error has occurred because a new data character was received before the previous data was read. The OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten.
2	PE	Parity Error. This bit is set whenever there is a parity error in the receiver if the parity enable (PEN) bit in the "Line Control Register (UART_LCR)" is set.
3	FE	Framing Error. This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. The OE, PE and FE bits are reset when a read of this register is performed.
4	BI	Break Interrupt. This bit is set whenever the serial input (SIN) is held in a logic 0 state for longer than the sum of *start time + data bits + parity + stop bit*s. A break condition on `sin` causes one and only one character, consisting of all zeros, to be received by the UART. Reading the Line Status register clears the BI bit.
5	THRE	Transmitter Holding Register Empty. When set, this bit indicates the UART can accept a new character for transmission. This bit is set whenever data is transferred from the THR to the transmitter shift register and no new data has been written to the THR. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled.
6	TEMT	Transmitter Empty. This bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
7	FERR	FIFO Receiver Error. This bit is only active when FIFOs are enabled. It is set when there is at least one parity error, framing error, or break indication in the FIFO. This bit clears when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. (Not supported.)
31:8	RES	Reserved

3.3.7 Modem Status Register (UART_MSR)

Offset: 0x0018
Internal address: 0x1110_0018
PCI address: 0x1_5018
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0	DCTS	Records whether the modem control line CTS_L has changed since the last time the CPU read the register
1	DDSR	Records whether the modem control line DSR_L has changed since the last time the CPU read the register
2	TERI	Indicates RI_L has changed since the last time the CPU read the register
3	DDCD	Records whether the modem control line DCD_L has changed since the last time the CPU read the register
4	CTS	Contains information on the current state of the modem control lines. CTS is the compliment of CTS_L
5	DSR	Contains information on the current state of the modem control lines. CTS is the compliment of DSR_L
6	RI	Contains information on the current state of the modem control lines. CTS is the compliment of RI_L
7	DCD	Contains information on the current state of the modem control lines. CTS is the compliment of DCD_L
31:8	RES	Reserved

3.3.8 Scratch Register (UART_SCR)

Offset: 0x001C
Internal address: 0x1110_001C
PCI address: 0x1_501C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Notes: This register is an 8-bit read/write register for programmers to use as a temporary storage space.

Bit	Bit Name	Description
7:0	RES	Unused
31:8	RES	Reserved

3.4 Local Bus Interface Registers

Table 3-5 summarizes the local bus interface registers for the AR2316. These registers use:

- Internal base address: 0x1040_0000
- External PCI MBAR_0 base offset: 0x1_3000

Table 3-5. **Local Bus Interface Register Summary**

Offset	Name	Description	Page
0x0000	LB_PCFG	Protocol configuration	page 50
0x0008	LB_1MS	One millisecond prescaler	page 52
0x000C	LB_MCFG	Miscellaneous configuration	page 52
0x0010	LB_RxTSOFF	Receive timestamp offset	page 53
0x0014	LB_HOST	Host configuration	page 53
0x0100	LB_FTxE	Transmit chain enable	page 54
0x0104	LB_FTxD	Transmit chain disable	page 54
0x0200 + EP << 2	LB_FTxDP	Transmit descriptor pointer	page 54
0x0400	LB_FRxE	Receive chain enable	page 55
0x0404	LB_FRxD	Receive chain disable	page 55
0x0408	LB_FRxDP	Receive descriptor pointer	page 55
0x0500	LB_ISR	Interrupt status	page 56
0x0504	LB_IMR	Interrupt mask	page 57
0x0508	LB_IER	Interrupt enable	page 57
0x0600	LB_MBOX_F2H	AR2316-to-host mailbox	page 57
0x0604	LB_MBOX_H2F	Host-to-AR2316 mailbox	page 58
0x20000	LB_PIO	PIO access range	page 58

3.4.1 Protocol Configuration Register (LB_PCFG)

Offset: 0x0000
Internal address: 0x1040_0000
PCI address: 0x1_3000
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Output enable (OE) polarity. Resets to 0x1. ■ 0 = OE is high-true ■ 1 = OE is low-true
1		Chip select (CS) polarity. Resets to 0x1. ■ 0 = CS is high-true ■ 1 = CS is low-true
2	RES	Reserved
3		Ready indication (RDY) polarity. Resets to 0x1. ■ 0 = RDY is high-true ■ 1 = RDY is low-true
4		Write enable (WE) polarity. Resets to 0x1. ■ 0 = WE is high-true ■ 1 = WE is low-true
5		Wait indication (WAIT) polarity. Resets to 0x1. ■ 0 = WAIT is high-true ■ 1 = WAIT is low-true
14:6	RES	Reserved

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>16:15</td><td></td><td>Data byteswap enable. Resets to 0x0.
■ 0 = Do not byteswap the data bus
■ 1 = Byteswap the data bus for all local bus addresses
■ 2 = Byteswap the data bus, but only for accesses to the Tx and Rx data registers (local bus addresses 2 and 6). Accesses to other local bus addresses are not swapped.
■ 3 = Reserved</td></tr>
<tr><td>17</td><td></td><td>Interrupt line (INTR) polarity. Resets to 0x0.
■ 0 = INTR is high-true
■ 1 = INTR is low-true</td></tr>
<tr><td>19:18</td><td></td><td>Interrupt line (INTR) drive control. This field determines how the chip electrically drives the INTR signal pin as a function of the desired output voltage. Resets to 0x0.
<table>
<tr><th>Field Value</th><th>Desired INTR Output Level</th><th>INTR Pin State</th></tr>
<tr><td rowspan="2">0</td><td>Ground</td><td>High-Z</td></tr>
<tr><td>Vdd</td><td>High-Z</td></tr>
<tr><td rowspan="2">1</td><td>Ground</td><td>Driving</td></tr>
<tr><td>Vdd</td><td>High-Z</td></tr>
<tr><td rowspan="2">2</td><td>Ground</td><td>High-Z</td></tr>
<tr><td>Vdd</td><td>Driving</td></tr>
<tr><td rowspan="2">3</td><td>Ground</td><td>Driving</td></tr>
<tr><td>Vdd</td><td>Driving</td></tr>
</table></td></tr>
<tr><td>20</td><td></td><td>Ready (RDY) output control. Resets to 0x0.
■ 0 = Always drive LB_RDY to its active (i.e., asserted) state
■ 1 = Drive LB_RDY with the negation of LB_WAIT</td></tr>
<tr><td>21</td><td></td><td>Interrupt signalling policy. Resets to 0x0.
■ 0 = Signal interrupt using a level change from a negated level to an asserted level. Bit [17] controls the actual voltage associated with the negated and asserted levels.
■ 1 = Signal interrupt using a pulse consisting of a transition from a negated level to an asserted level and then back to a negated level. Bit [17] controls the actual voltage associated with the negated and asserted levels.</td></tr>
<tr><td>22</td><td></td><td>Slave bus interface enable. Resets to 0x0.
■ 0 = Ignores the local bus (i.e., the AR2316 acts as if LB_CS always is negated)
■ 1 = Obeys and responds to the local bus normally.</td></tr>
<tr><td>23</td><td></td><td>Read data setup to LB_WAIT control. Resets to 0.
■ 0 = Does not enforce any setup delay between the time the AR2316 begins driving the LB_DATA lines in response to a local bus read and the time it negates the LB_WAIT signal (or, equivalently, asserts LB_RDY). In this setting, the AR2316 negates LB_WAIT coincidently with driving the read data on LB_DATA. For many hosts, this setting works because the host must first internally sample LB_WAIT negated before it captures the read data from LB_DATA, thereby effectively providing a setup delay within the host itself.
■ 1 = Enforce a one hclk setup delay between the time the AR2316 begins driving the LB_DATA lines in response to a local bus read and the time it negates the LB_WAIT signal (or, equivalently, asserts LB_RDY).</td></tr>
<tr><td>24</td><td></td><td>CS Burst mode enable. Resets to 0x0
■ 0 = Deasserts chip select after every host mode transaction.
■ 1 = Keeps chip selected asserted between reads/writes in a burst.</td></tr>
<tr><td>29:25</td><td></td><td>OE/WE timeout. This value specifies the number of cycles to wait from assertion of OE or WE to the deassertion of WAIT or RDY.
The number of cycles for this timeout is 2^N, so if the value of this timeout is set to 8, then the local bus interface times out after 256 cycles (28)If N is set to 0, or is larger than 24, then the timeout logic is disabled. (See C in Figure 3-3.)</td></tr>
<tr><td>30</td><td></td><td>Host diagnostic mode. Resets to 0x0. This register holds off the lclbus_Rxep module until the transaction has completed on the local bus interface. If a transaction times out on the local bus interface, then the Rx descriptor updates to indicate DMA error.</td></tr>
<tr><td>31</td><td>RES</td><td>Reserved</td></tr>
</table>

3.4.2 One Millisecond Prescaler (LB_1MS)

Offset: 0x0080
Internal address: 0x1040_0008
PCI address: 0x1_3008
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
17:0		Number of AHB clock (hclk) cycles in 1 ms. Resets to 0x0, disabling generation of the 1 ms timer.
31:18	RES	Reserved

3.4.3 Miscellaneous Configuration (LB_MCFG)

Offset: 0x000C
Internal address: 0x1040_000C
PCI address: 0x1_300C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		TxD handling for fragmented data blocks. This bit controls how the Tx endpoints handle the situation of TxD being set when the DMA logic is processing a fragmented data block (i.e., a data block that is so large that it must fragment across the data buffers associated with several Tx descriptors' PABs). Resets to 0x0. ■ 0 = Do not obey TxD until DMA engine completes processing fragmented data block ■ 1 = Obey TxD immediately, even if DMA logic is in the middle of processing fragmented data block **WARNING:** Selecting this setting leaves the DMA logic in an inconsistent state should SW set TxD when the DMA engine is processing a fragmented data block.
1		Receive data available interrupt enable. This bit controls whether the local bus INTR line is asserted when receive data is available. Resets to 0x0. ■ 0 = Do not assert the local bus INTR signal even when Rx data is available ■ 1 = Assert the local bus INTR signal whenever Rx data is available.
2		Mailbox write interrupt enable. This bit controls whether the local bus INTR line is asserted when the CPU writes the AR2316-to-host local bus mailbox (LB_MBOX_F2H) register. To clear the local bus INTR assertion, the local bus master must perform a read or a write to the mailbox register. Resets to 0x0. ■ 0 = Do not assert the local bus INTR signal when the LB_MBOX_F2H register. ■ 1 = Assert the local bus INTR signal when the CPU writes the LB_MBOX_F2H register.
3		Mailbox read interrupt enable. This bit controls whether the local bus INTR line is asserted when the CPU reads the host-to-AR2316 local bus mailbox (LB_MBOX_H2F) register. To clear the local bus INTR assertion, the local bus master must perform a read or a write to the mailbox register. Resets to 0x0. ■ 0 = Do not assert local bus INTR signal when CPU reads the LB_MBOX_H2F register. ■ 1 = Assert local bus INTR signal when CPU reads the LB_MBOX_H2F register.
4		Tx/Rx descriptor byteswap control. Resets to <CPU_BIG_ENDIAN_RST>. See RST_BYTESWAP_CTL register bit [10] for more information. ■ 0 = Do not byteswap Tx or Rx descriptors ■ 1 = Byteswap both Tx and Rx descriptors
6:5	RES	Reserved
23:7		Local bus timeout value. Specifies, in units of 128 AHB clock (hclk) cycles, the amount of time for which a local bus transaction is pending before it times out. A value of 0x0 (the reset value) disables the local bus timeout logic and permits a local bus transaction to begin pending indefinitely. Resets to 0x0.
26:24		Observation port MUX select. Resets to 0x0.
31:27	RES	Reserved

3.4.4 Rx Timestamp Offset (LB_RxTSOFF)

Offset: 0x0010
Internal address: 0x1040_0010
PCI address: 0x1_3010
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
23:0		Rx timestamp offset. This value specifies by how many timestamp units the receiving node's timestamp must exceed the current TDP's timestamp before the Rx DMA engine releases the TDP's data onto the local bus. Resets to 0x0.
31:24	RES	Reserved

3.4.5 Host Configuration (LB_HOST)

Offset: 0x0014
Internal address: 0x1040_0014
PCI address: 0x1_3014
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
7:0		CS to OE/WE timing. This value specifies the number of cycles between CS asserting and OE or WE asserting. (See *A* in Figure 3-3.)
15:8		OE/WE to WAIT/RDY timing. This value specifies the number of cycles after assertion of OE/WE to wait for WAIT/RDY. If this timing is met, it does not wait for the WAIT/RDY and assumes that the slave device is ready with the data. If this value is set to 0, then it does not assume that the slave device is ready with the data. (See B in Figure 3-3.)
23:16		OE/WE to CS timing. This value specifies the number of cycles between OE or WE deasserting to CS deasserting. When the CS burst mode is enabled in the LB_PCFG register, this value is also used to determine the number of cycles from the deassertion of OE/WE to the assertion of the next OE/WE. (See D in Figure 3-3.)
31:24		CS deassert to CS assert timing. This value specifies the number of cycles between CS deasserting to CS asserting. (See E in Figure 3-3.)

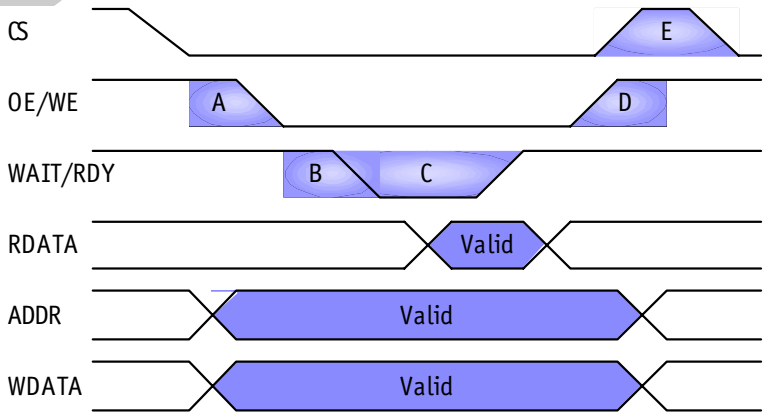


Figure 3-3. Host Configuration Timing

3.4.6 Tx Chain Enable (LB_FTxE)

Offset: 0x0100
Internal address: 0x1040_0100
PCI address: 0x1_3100
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Tx enable bit for endpoint 0. Resets to 0x0. Write: ■ 0 = No effect ■ 1 = Sets endpoint 0's FTxE bit
1		Tx enable bit for endpoint 1. Resets to 0x0. Write: ■ 0 = No effect ■ 1 = Sets endpoint 1's FTxE bit
2		Tx enable bit for endpoint 2. Resets to 0x0. Write: ■ 0 = No effect ■ 1 = Sets endpoint 2's FTxE bit
3		Tx enable bit for endpoint 3. Resets to 0x0. Write: ■ 0 = No effect ■ 1 = Sets endpoint 3's FTxE bit
31:4	RES	Reserved

3.4.7 Tx Chain Disable (LB_FTxD)

Offset: 0x0104
Internal address: 0x1040_0104
PCI address: 0x1_3104
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Notes: To stop transmission for endpoint *N*:

1. Write a 1 to endpoint *N*'s FTxD bit.
2. Poll the LB_FTxE register until endpoint *N*'s FTxE bit is clear.
3. Write a 0 to endpoint *N*'s FTxD bit; at this point, endpoint *N* has shut down and has no pending DMA transfers.

When *N*'s FTxD bit is set, software must not write a 1 to *N*'s FRxE bit as it causes an undefined operation. The software must set and endpoint's FTxE bit only when the FTxD bit is clear. However, writing a 0 to this bit while FRxD is set has no effect on *N*.

Bit	Bit Name	Description
0		Tx disable bit for endpoint 0. Resets to 0x0.
1		Tx disable bit for endpoint 1. Resets to 0x0.
2		Tx disable bit for endpoint 2. Resets to 0x0.
3		Tx disable bit for endpoint 3. Resets to 0x0.
31:4	RES	Reserved

3.4.8 Tx Descriptor Pointer (LB_FTxDP)

Offset: 0x0200+ (EP << 2)
Internal address: 0x1040_0200 + (EP << 2)
PCI address: 0x1_3200 + (EP << 2)
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: *EP* is the transmit endpoint number. *EP* values of 0–3 are valid.

Bit	Bit Name	Description
1:0	RES	Reserved
31:2		Tx descriptor pointer. Points to the next AR2316 Tx descriptor used by the endpoint's DMA engine.

3.4.9 Rx Chain Enable (LB_FRxE)

Offset: 0x0400
Internal address: 0x1040_0400
PCI address: 0x1_3400
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Rx enable bit for endpoint 0Resets to 0x0. Write: ■ 0 = No effect ■ 1 = Sets endpoint 0's FRxE bit
31:1	RES	Reserved

3.4.10 Rx Chain Disable (LB_FRxD)

Offset: 0x0404
Internal address: 0x1040_0404
PCI address: 0x1_3404
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: To stop transmission for endpoint *N*:

Write a 1 to endpoint *N*'s FRxD bit

Poll the LB_FRxE register until endpoint *N*'s FRxE bit is clear

Write a 0 to endpoint *N*'s FRxD bit; at this point, endpoint *N* has shut down and has no pending DMA transfers

When *N*'s FRxD bit is set, software must not write a 1 to *N*'s FRxE bit as it causes an undefined operation. However, writing a 0 to this bit while FRxD is set has no effect on *N*.

Bit	Bit Name	Description
0		Rx disable bit for endpoint 0Resets to 0x0.
31:1	RES	Reserved

3.4.11 Rx Descriptor Pointer (LB_FRxDP)

Offset: 0x0408
Internal address: 0x1040_0408
PCI address: 0x1_3408
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
1:0	RES	Reserved
31:2		Rx descriptor pointer. Points to the next AR2316 Rx descriptor used by the endpoint's DMA engine.

3.4.12 Interrupt Status (LB_ISR)

Offset: 0x0500
Internal address: 0x1040_0500
PCI address: 0x1_3500
Access: Read/write-one-to-clear
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Tx descriptor interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor in which the InterReq bit was set. Resets to 0x0.
1		Tx OK interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor and no error occurred during the associated data transfer. Resets to 0x0.
2		Tx error interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor and one or more errors occurred during the associated data transfer. Resets to 0x0.
3		Tx end-of-list interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor and the descriptor's LinkPtr is NULL. Resets to 0x0.
4		Rx descriptor interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor in which the InterReq bit was set. Resets to 0x0.
5		Rx OK interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor and no error occurred during the associated data transfer. Resets to 0x0.
6		Rx error interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor and one or more errors occurred during the associated data transfer. Resets to 0x0.
7		Rx end-of-list interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor and the descriptor's LinkPtr is NULL. Resets to 0x0.
8		Tx truncated data interrupt. Asserted when the host attempts to begin a new transmit data block using a write to address 0 before it has supplied all data for the previous data block. Resets to 0x0.
9		Tx descriptor starvation interrupt. Asserted when the host begins a new data block but the associated Tx endpoint's DMA engine has no Tx descriptor available. Resets to 0x0.
10		Local bus timeout interrupt. Asserted when a local bus transaction is pending for a duration specified by the local bus timeout value field in the LB_MCFG register. Resets to 0x0.
11		Local bus protocol violation interrupt. Asserted when the host generates an unexpected operation on the local bus. In addition to setting this bit, one or more of bits [10:8] may set also, depending on the exact type of error. Resets to 0x0.
12		Mailbox write interrupt. Asserted when the local bus master writes the host-to-AR2316 local bus mailbox register (LB_MBOX_H2F). Resets to 0x0.
13		Mailbox read interrupt. Asserted when the local bus master reads the AR2316-to-host local bus mailbox register (LB_MBOX_F2H). Resets to 0x0.
14		Local bus host mode interface timeout on PIO read. Asserted when AR2316 is in host mode and a slave device does not respond to a PIO read transaction within the number of cycles specified by the OE/WE timeout field in the LB_PCFG register.
15		Local bus host mode interface timeout on PIO write. Asserted when AR2316 is in host mode and a slave device does not respond to a PIO write transaction within the number of cycles specified by the OE/WE timeout field in the LB_PCFG register.
16		Local bus host mode interface timeout on Tx DMA. Asserted while in host mode and a slave device does not respond to a Tx DMA transaction within the number of cycles specified by the OE/WE timeout field in the LB_PCFG register.
17		Local bus host mode interface timeout on Rx DMA. Asserted while in host mode and a slave device does not respond to a Rx DMA transaction within the number of cycles specified by the OE/WE timeout field in the LB_PCFG register.
18		Local bus host mode external interrupt. Asserted while in host mode and a slave device asserts interface interrupt signal.
31:16	RES	Reserved

3.4.13 Interrupt Mask (LB_IMR)

Offset: 0x0504
Internal address: 0x1040_0504
PCI address: 0x1_3504
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: A value of 0 prevents an interrupt from being signaled due to the associated bit being set in the ISRA. A value of 1 allows an interrupt to signal whenever the corresponding IMR bit is 1. The IMR setting has no effect on the setting/clearing of bits in the ISR. The only effect of the IMR is to determine what subset of ISR bits are considered when generating the local bus block's interrupt indication.

Bit	Bit Name	Description
0		Tx descriptor interrupt mask. Resets to 0x0.
1		Tx OK interrupt mask. Resets to 0x0.
2		Tx error interrupt mask. Resets to 0x0.
3		Tx end-of-list interrupt mask. Resets to 0x0.
4		Rx descriptor interrupt mask. Resets to 0x0.
5		Rx OK interrupt mask. Resets to 0x0.
6		Rx error interrupt mask. Resets to 0x0.
7		Rx end-of-list interrupt mask. Resets to 0x0.
8		Tx truncated data interrupt mask. Resets to 0x0.
9		Tx descriptor starvation interrupt mask. Resets to 0x0.
10		Local bus timeout interrupt mask. Resets to 0x0.
11		Local bus protocol violation interrupt mask. Resets to 0x0.
12		Mailbox write interrupt mask
13		Mailbox read interrupt mask
14		Local bus host mode interface timeout on PIO read mask. Resets to 0x0
15		Local bus host mode interface timeout on PIO write mask. Resets to 0x0
16		Local bus host mode interface timeout on Tx DMA mask. Resets to 0x0
17		Local bus host mode interface timeout on Rx DMA mask. Resets to 0x0
18		Local bus host mode external interrupt. Resets to 0x0.
31:16	RES	Reserved

3.4.14 Interrupt Enable (LB_IER)

Offset: 0x0508
Internal address: 0x1040_0508
PCI address: 0x1_3508
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Global interrupt enable. Resets to 0x0. ■ 0 = Disable the local bus from asserting an interrupt ■ 1 = Enable the local bus to assert an interrupt for any source with an IMR bit of 1
31:1	RES	Reserved

3.4.15 AR2316-to-Host Mailbox (LB_MBOX_F2H)

Offset: 0x0600
Internal address: 0x1040_0600
PCI address: 0x1_3600
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: The CPU can read and write the register. The local bus master can read this register by issuing a local bus read to local bus address 8.

These operations have side effects useful for implementing mailbox-based communication between the CPU and the local bus master:

- A read by the CPU has no side effects
- A write by the CPU optionally asserts local bus interrupt (INTR) line; see LB_MCFG [2]
- A read by the local bus master clears any pending local bus interrupt assertion due to a previous CPU write to the AR2316-to-host mailbox register (LB_MBOX_F2H)
- Sets interrupt status register (LB_ISR) bit [13]

Bit	Bit Name	Description
15:0		AR2316-to-host mailbox data. Resets to 0x0.
31:16	RES	Reserved

3.4.16 Host-to-AR2316 Mailbox (LB_MBOX_H2F)

Offset: 0x0604
Internal address: 0x1040_0604
PCI address: 0x1_3604
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: The CPU can read and write this register. The local bus master can only read this register, by issuing a local bus read to local bus address 8. These operations have side effects useful for implementing mailbox-based communication between the CPU and the local bus master:

- A read by the CPU has no side effects
- A write by the CPU optionally asserts the local bus interrupt (INTR) line; see LB_MCFG register bit [2]
- A read by the local bus master clears any pending local bus interrupt assertion due to a previous CPU write to the AR2316-to-host mailbox register (LB_MBOX_F2H)
- Sets interrupt status register (LB_ISR) bit [12]

Bit	Bit Name	Description
15:0		Host-to-AR2316 mailbox data. Resets to 0x0.
31:16	RES	Reserved

3.4.17 PIO Access Range (LB_PIO)

Offset: 0x20000
Internal address: 0x1042_0000
PCI address: N/A
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: PIO provides access from the processor to the local bus interface without the DMA process, and allows single reads and writes. The internal address bits [16:2] specify the local bus address [14:0]. The lower 16 bits of the data are valid for both reads and writes.

3.5 PCI Interface Registers

Table 3-6 and Table 3-7 summarize the PCI interface registers for the AR2316. The PCI interface registers come in two groups, which use different PCI MBAR_0 base offsets.

Group 0

- Internal base address: 0x1010_0000
- External PCI MBAR_0 base offset: 0x1_0000

Table 3-6. **Group 0 PCI Interface Register Summary**

Offset	Name	Description	Page
0x0008	PCI_1MS	One millisecond prescaler	page 59
0x000C	PCI_MCFG	Miscellaneous configuration	page 59
0x0010	PCI_RxTSOFF	Receive timestamp offset	page 60
0x0014	PCI_NCCFG	PCI non-cachable segment configuration	page 61
0x0100	PCI_FTxE	Transmit chain enable	page 61
0x0104	PCI_FTxD	Transmit chain disable	page 62
0x0200 + EP << 2	PCI_FTxDP	Transmit descriptor pointer	page 62
0x0400	PCI_FRxE	Receive chain enable	page 62
0x0404	PCI_FRxD	Receive chain disable	page 62
0x0408	PCI_FRxDP	Receive descriptor pointer	page 63
0x0500	PCI_ISR	Interrupt status	page 63
0x0504	PCI_IMR	Interrupt mask	page 64
0x0508	PCI_IER	Interrupt enable	page 65
0x050C	PCI_HIMR	Host interrupt mask	page 65
0x0510	PCI_HIER	Host interrupt enable	page 66
0x0800	PCI_PTxE	PCI transmit chain enable	page 66
0x0804	PCI_PTxD	PCI transmit chain disable	page 66
0x0810 + EP << 2	PCI_PTxDP	PCI transmit descriptor pointer	page 67
0x0900	PCI_PRxE	PCI receive chain enable	page 67
0x0904	PCI_PRxD	PCI receive chain disable	page 67
0x0908	PCI_PRxDP	PCI receive descriptor pointer	page 67

Group 1

- Internal base address: 0x1010_0000
- External PCI MBAR_0 base offset: 0x0_0000

Table 3-7. **Group 1 PCI Interface Register Summary**

Offset	Name	Description	Page
0x4000	PCI_RC	Reset control	page 68
0x4004	PCI_SCR	Sleep control	page 68
0x4008	PCI_INTPEND	PCI clock domain interrupt pending	page 69
0x400C	PCI_SFR	Sleep force	page 69
0x4010	PCI_CFG	PCI clock domain configuration/status	page 69
0x4020	PCI_SREV	Silicon revision	page 71
0x4024	PCI_SLE	Sleep enable alias	page 71
0x4028	PCI_TxEPOST	TxE write posting	page 72
0x402C	PCI_QSM	QCU sleep mask	page 72
0x4030	PCI_DBG_0	PCI debug 0	page 72
0x4060	PCI_SPC_ROA_0	Sleep performance counter 0 read-only alias	page 73
0x4064	PCI_SPC_ROA_1	Sleep performance counter 1 read-only alias	page 73
0x5000–0x50FC		CIS tuples	page 73

3.5.1 One Millisecond Prescaler (PCI_1MS)

Offset: 0x0008
Internal address: 0x1010_0008
PCI address: 0x1_0008
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
17:0		Number of AHB clock (hclk) cycles in 1 ms; resets to 0x0, disabling 1 ms timer generation
31:18	RES	Reserved

3.5.2 Miscellaneous Configuration (PCI_MCFG)

Offset: 0x000C
Internal address: 0x1010_000C
PCI address: 0x1_000C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		TxD handling for fragmented data blocks; bit controls how Tx endpoints handle a situation of TxD being set while DMA logic processes a fragmented data block (i.e., a data block so large it must fragment across data buffers associated with several Tx descriptors' PABs). Resets to 0x0. ■ 0 = Do not obey TxD until DMA engine completes processing fragmented data block ■ 1 = Obey TxD immediately, even if DMA logic is in the middle of processing a fragmented data block **WARNING:** Selecting this setting leaves DMA logic in an inconsistent state if software sets TxD while the DMA engine processes a fragmented data block.
1		PCI configuration/memory space select; controls whether references to the AHB PCI external address space (AHB 0x8000_0000–0xBFFF_FFFF) generate PCI memory read/write transactions or PCI configuration read/write transactions on PCI bus. Resets to 0x0. ■ 0 = Reads to the AHB 'PCI external' address space generate PCI memory read transactions on the PCI bus; writes to the AHB PCI external address space generate PCI memory write transactions on the PCI bus. ■ 1 = Reads to the AHB PCI external address space generate PCI configuration read transactions on the PCI bus; writes to the AHB PCI external address space generate PCI 'configuration write' transactions on the PCI bus.

Bit	Bit Name	Description
3:2		PCI external segment select. The value in this field controls the value of bits [31:30] of the address issued on the PCI bus in response to AHB transactions to the PCI external address space (addresses 0x8000_0000 – 0xBFFF_FFFF). Resets to 0x0.
5:4		PCI reset pin (PCI_RST#) control. Resets to 0x0. ■ 0 = Treat the PCI_RST# pin as an input ■ 1 = Actively drive the PCI_RST# pin to ground ■ 2 = Actively drive the PCI_RST# pin to VDD ■ 3 = Reserved
7:6		PCI arbiter early grant control. An early grant occurs when the PCI arbiter issues a grant (asserts PCI_GNT#) to a requester before the current PCI transaction has completed on the PCI bus. Early grants are a normal part of standard PCI operation and external PCI clients should support early grants correctly. However, the feature can be disabled if necessary using this field. Resets to 0x0. ■ 0 = Allow the PCI arbiter to issue early grants ■ 1 = Prevent the PCI arbiter from issuing the next grant until PCI_FRAME# is negated. ■ 2 = Prevent the PCI arbiter from issuing the next grant until the PCI bus is idle (i.e., PCI_FRAME# and PCI_IRDY# both are negated) ■ 3 = Reserved
11:8		PCI arbiter inter-grant delay control. This setting controls the minimum number of cycles the PCI arbiter waits between the start of a PCI transaction and when the arbiter may issue the next grant. Resets to 0x0.
12		PCI external access cache disable. Resets to 0x0. ■ 0 = Enable the read cache and write buffer for PCI external accesses ■ 1 = Disable the read cache and write buffer for PCI external accesses. Each AHB reference to PCI external space (AHB addresses 0x8000_0000– 0xBFFF_FFFF) generate a single-word read/write on the PCI bus.
15:13		PCI external write buffer spill timeout. This field specifies the maximum number of AHB clock (hclk) cycles that may elapse between write buffer pushes before the write buffer spills (flushes) to the PCI bus. Resets to 0x2. ■ 0 = Spill timeout is 32 hclk cycles ■ 1 = Spill timeout is 64 hclk cycles ■ 2 = Spill timeout is 128 hclk cycles ■ 3 = Spill timeout is 256 hclk cycles ■ 4 = Spill timeout is 512 hclk cycles ■ 5 = Spill timeout is 1024 hclk cycles ■ 6 = Spill timeout is 4096 hclk cycles ■ 7 = Spill timeout is infinite
18:16		Observation port MUX select. Resets to 0x0.
19		Tx/Rx descriptor byteswap control. Resets to <CPU_BIG_ENDIAN_RST>. See RST_BYTESWAP_CTL register bit [10] for more information. ■ 0 = Do not byteswap Tx or Rx descriptors ■ 1 = Byteswap both Tx and Rx descriptors
20		PCI Tx/Rx descriptor byteswap control. Resets to 0x0. ■ 0 = Do not byteswap PCI Tx or Rx descriptors ■ 1 = Byteswap both PCI Tx and Rx descriptors
31:21	RES	Reserved

3.5.3 Rx Timestamp Offset (PCI_RxTSOFF)

Offset: 0x0010
Internal address: 0x1010_0010
PCI address: 0x1_0010
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
23:0		Rx timestamp offset. This value specifies by how many timestamp units the receiving node's timestamp must exceed the current TDP's timestamp before the Rx DMA engine releases the TDP's data onto the PCI bus. Resets to 0x0.
31:24	RES	Reserved

3.5.4 PCI Non-Cachable Segment Configuration (PCI_NCCFG)

Offset: 0x0014
Internal address: 0x1010_0014
PCI address: 0x1_0014
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
4:0		Non-cachable segment size. Resets to 12. ■ 0–11 = Reserved ■ 12 = 4 KB ■ 13 = 8 KB ... ■ 20 = 1 MB ... ■ 30 = 1 GB ■ 31 = Reserved
5		Non-cachable segment enable. Resets to 0x0. ■ 0 = Disable the non-cachable segment. All references to the AHB PCI external space are assumed cachable. ■ 1 = Enable the non-cachable segment. All references to the AHB PCI external space are tested to determine whether they are cachable.
11:6	RES	Reserved
29:12		Base address of non-cachable segment. This value is combined with the segment size value in bits [4:0] of this register then compared to bits [29:12] of the AHB address to determine if the reference to the AHB PCI external space is cachable. Because the AHB PCI external space occupies AHB addresses 0x8000_0000–0xBFFF_FFFF, bits [31:30] always are equal to 0x2, and therefore do not participate in the base address comparison. All bits of this field masked (ignored) as a result of the non-cachable segment size value must be set to 0. Resets to 0x0.
31:30	RES	Reserved

3.5.5 Tx Chain Enable (PCI_FTxE)

Offset: 0x0100
Internal address: 0x1010_0100
PCI address: 0x1_0100
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Tx enable bit for endpoint 0. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint zero's FTxE bit
1		Tx enable bit for endpoint 1. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint one's FTxE bit
2		Tx enable bit for endpoint 2. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint two's FTxE bit
3		Tx enable bit for endpoint 3. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint three's FTxE bit
31:4	RES	Reserved

3.5.6 Tx Chain Disable (PCI_FTxD)

Offset: 0x0104
Internal address: 0x1010_0104
PCI address: 0x1_0104
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: To stop transmission for endpoint *N*:

1. Write a 1 to endpoint *N*'s FTxD bit
2. Poll the LB_FTxE register until endpoint *N*'s FTxE bit is clear
3. Write a 0 to endpoint *N*'s FTxD bit; at this point, endpoint *N* has shut down and has no pending DMA transfers

When *N*'s FTxD bit is set, software must not write a 1 to *N*'s FTxE bit as it causes an undefined operation. However, writing a 0 to this bit while FTxD is set has no effect on *N*.

Bit	Bit Name	Description
0		Tx disable bit for endpoint 0. Resets to 0x0.
1		Tx disable bit for endpoint 1. Resets to 0x0.
2		Tx disable bit for endpoint 2. Resets to 0x0.
3		Tx disable bit for endpoint 3. Resets to 0x0.
31:4	RES	Reserved

3.5.7 Tx Descriptor Pointer (PCI_FTxDP)

Offset: 0x0200 + (EP << 2)
Internal address: 0x1010_0200 + (EP << 2)
PCI address: 0x1_0200 + (EP << 2)
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: *EP* is the Tx endpoint number. EP values of 0–3 are valid.

Bit	Bit Name	Description
1:0	RES	Reserved
31:2		Tx descriptor pointer. Points to next Tx descriptor used by the endpoint's DMA engine.

3.5.8 Rx Chain Enable (PCI_FRxE)

Offset: 0x0400
Internal address: 0x1010_0400
PCI address: 0x1_0400
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Rx enable bit for endpoint 0. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint 0's FRxE bit
31:1	RES	Reserved

3.5.9 Rx Chain Disable (PCI_FRxD)

Offset: 0x0404
Internal address: 0x1010_0404
PCI address: 0x1_0404
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: To stop transmission for endpoint *N*:

1. Write a 1 to endpoint *N*'s FRxD bit
2. Poll the LB_FRxE register until endpoint *N*'s FRxE bit is clear
3. Write a 0 to endpoint *N*'s FRxD bit; at this point, endpoint *N* has shut down and has no pending DMA transfers

When *N*'s FRxD bit is set, software must not write a 1 to *N*'s FRxE bit as it causes an undefined operation. However, writing a 0 to this bit while FRxD is set has no effect on *N*.

Bit	Bit Name	Description
0		Rx disable bit for endpoint 0. Resets to 0x0.
31:1	RES	Reserved

3.5.10 Rx Descriptor Pointer (PCI_FRxDP)

Offset: 0x0408
Internal address: 0x1010_0408
PCI address: 0x1_0408
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
1:0	RES	Reserved
31:2		Rx descriptor pointer. Points to the next Rx descriptor used by the endpoint's DMA engine.

3.5.11 Interrupt Status (PCI_ISR)

Offset: 0x0500
Internal address: 0x1010_0500
PCI address: 0x1_0500
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Tx descriptor interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor in which the InterReq bit was set. Resets to 0x0.
1		Tx OK interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor and no error occurred during the associated data transfer. Resets to 0x0.
2		Tx error interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor and one or more errors occurred during the associated data transfer. Resets to 0x0.
3		Tx end-of-list interrupt. Asserted whenever one of the Tx endpoints completes a Tx descriptor and the descriptor's LinkPtr is NULL. Resets to 0x0.
4		Rx descriptor interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor in which the InterReq bit was set. Resets to 0x0.
5		Rx OK interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor and no error occurred during the associated data transfer. Resets to 0x0.
6		Rx error interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor and one or more errors occurred during the associated data transfer. Resets to 0x0.
7		Rx end-of-list interrupt. Asserted whenever the Rx endpoint completes a Rx descriptor and the descriptor's LinkPtr is NULL. Resets to 0x0.
8	RES	Reserved
9		Tx descriptor starvation interrupt. Asserted when a Tx endpoint's DMA engine has an active PCI Tx descriptor but has no Tx descriptor available. Resets to 0x0.
15:10	RES	Reserved
16		PCI transmit descriptor interrupt. Asserted whenever one of the Tx endpoints completes a PCI Tx descriptor in which the InterReq bit was set. Resets to 0x0.
17		PCI transmit OK interrupt. Asserted whenever one of the Tx endpoints completes a PCI Tx descriptor and no error occurred during the associated data transfer. Resets to 0x0.
18		PCI transmit error interrupt. Asserted whenever one of the Tx endpoints completes a PCI Tx descriptor and one or more errors occurred during the associated data transfer. Resets to 0x0.
19		PCI transmit end-of-list interrupt. Asserted whenever one of the Tx endpoints completes a PCI Tx descriptor and the descriptor's LinkPtr is NULL. Resets to 0x0.
20		PCI receive descriptor interrupt. Asserted whenever the Rx endpoint completes a PCI Rx descriptor in which the InterReq bit was set. Resets to 0x0.
21		PCI receive OK interrupt. Asserted whenever the Rx endpoint completes a PCI Rx descriptor and no error occurred during the associated data transfer. Resets to 0x0.

Bit	Bit Name	Description
22		PCI receive error interrupt. Asserted whenever the Rx endpoint completes a PCI Rx descriptor and one or more errors occurred during the associated data transfer. Resets to 0x0.
23		PCI receive end-of-list interrupt. Asserted whenever the Rx endpoint completes a PCI Rx descriptor and the descriptor's LinkPtr is NULL. Resets to 0x0.
24		PCI Rx descriptor starvation interrupt. Asserted when receive data is ready to DMA to the PCI bus, but the Rx endpoint's DMA engine has no PCI Rx descriptor available. Resets to 0x0.
25		PCI external interrupt pending. This bit indicates whether an external device is asserting the PCI_INTA# signal. It is valid only when the AR2316 is operating as a PCI host; see bit [4] of the RST_IF_CTL register. When the AR2316 is operating as a PCI client, this bit is forced to zero. Resets to 0x0.
26		PCI master abort interrupt. This bit is set when the PCI core signals that a master abort occurred on the PCI bus. Resets to 0x0.
31:27	RES	Reserved

3.5.12 Interrupt Mask (PCI_IMR)

Offset: 0x0504
Internal address: 0x1010_0504
PCI address: 0x1_0504
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: A value of 0 prevents an interrupt from being signaled due to the associated bit being set in the ISR. A value of 1 allows an interrupt to signal whenever the corresponding IMR bit is 1. The IMR setting has no effect on the setting/clearing of bits in the ISR. The only effect of the IMR is to determine what subset of ISR bits are considered when generating the PCI interface block's interrupt indication.

Bit	Bit Name	Description
0		Tx descriptor interrupt mask. Resets to 0x0.
1		Tx OK interrupt mask. Resets to 0x0.
2		Tx error interrupt mask. Resets to 0x0.
3		Tx end-of-list interrupt mask. Resets to 0x0.
4		Rx descriptor interrupt mask. Resets to 0x0.
5		Rx OK interrupt mask. Resets to 0x0.
6		Rx error interrupt mask. Resets to 0x0.
7		Rx end-of-list interrupt mask. Resets to 0x0.
8	RES	Reserved
9		Tx descriptor starvation interrupt mask. Resets to 0x0.
15:10	RES	Reserved
16		PCI transmit descriptor interrupt mask. Resets to 0x0.
17		PCI transmit OK interrupt mask. Resets to 0x0.
18		PCI transmit error interrupt mask. Resets to 0x0.
19		PCI transmit end-of-list interrupt mask. Resets to 0x0.
20		PCI receive descriptor interrupt mask. Resets to 0x0.
21		PCI receive OK interrupt mask. Resets to 0x0.
22		PCI receive error interrupt mask. Resets to 0x0.
23		PCI receive end-of-list interrupt mask. Resets to 0x0.
24		PCI Rx descriptor starvation interrupt mask. Resets to 0x0.
25		PCI external interrupt pending mask. Resets to 0x0.
26		PCI master abort interrupt mask. Resets to 0x0.
31:27	RES	Reserved

3.5.13 Interrupt Enable (PCI_IER)

Offset: 0x0508
Internal address: 0x1010_0508
PCI address: 0x1_0508
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Global interrupt enable. Resets to 0x0. ■ 0 = Disable the PCI interface from asserting an interrupt ■ 1 = Enable the PCI interface to assert an interrupt for any interrupt source for which the corresponding IMR bit is a 1.
31:1	RES	Reserved

3.5.14 Host Interrupt Mask (PCI_HIMR)

Offset: 0x050C
Internal address: 0x1010_050C
PCI address: 0x1_050C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: A value of 0 prevents an interrupt from being signaled due to the associated bit being set in the ISR. A value of 1 allows a host interrupt to signal whenever the corresponding HIMR bit is 1. The HIMR setting has no effect on the setting/clearing of bits in the ISR. The only effect of the HIMR is to determine what subset of ISR bits are considered when generating the PCI interface block's host interrupt indication.

Bit	Bit Name	Description
0		Tx descriptor interrupt mask. Resets to 0x0.
1		Tx OK interrupt mask. Resets to 0x0.
2		Tx error interrupt mask. Resets to 0x0.
3		Tx end-of-list interrupt mask. Resets to 0x0.
4		Rx descriptor interrupt mask. Resets to 0x0.
5		Rx OK interrupt mask. Resets to 0x0.
6		Rx error interrupt mask. Resets to 0x0.
7		Rx end-of-list interrupt mask. Resets to 0x0.
8	RES	Reserved
9		Tx descriptor starvation interrupt mask. Resets to 0x0.
15:10	RES	Reserved
16		PCI transmit descriptor interrupt mask. Resets to 0x0.
17		PCI transmit OK interrupt mask. Resets to 0x0.
18		PCI transmit error interrupt mask. Resets to 0x0.
19		PCI transmit end-of-list interrupt mask. Resets to 0x0.
20		PCI receive descriptor interrupt mask. Resets to 0x0.
21		PCI receive OK interrupt mask. Resets to 0x0.
22		PCI receive error interrupt mask. Resets to 0x0.
23		PCI receive end-of-list interrupt mask. Resets to 0x0.
24		PCI Rx descriptor starvation interrupt mask. Resets to 0x0.
25		PCI external interrupt pending mask. Resets to 0x0.
26		PCI master abort interrupt mask. Resets to 0x0.
31:27	RES	Reserved

3.5.15 Host Interrupt Enable Register (PCI_HIER)

Offset: 0x0510
Internal address: 0x1010_0510
PCI address: 0x1_0510
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		Global interrupt enable. Resets to 0x0. ■ 0 - Disable the PCI interface from asserting a host interrupt ■ 1 - Enable the PCI interface to assert a host interrupt for any interrupt source for which the corresponding HIMR bit is a 1.
31:1	RES	Reserved

3.5.16 PCI Tx Chain Enable (PCI_PTxE)

Offset: 0x0800
Internal address: 0x1010_0800
PCI address: 0x1_0800
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		PCI transmit enable bit for endpoint 0. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint 0's PTxE bit
1		PCI transmit enable bit for endpoint 1. Resets to 0x0. ■ 0 = No effect 1 = Sets endpoint 1's PTxE bit
2		PCI transmit enable bit for endpoint 2. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint 2's PTxE bit
3		PCI transmit enable bit for endpoint 3. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint 3's PTxE bit
31:4	RES	Reserved

3.5.17 PCI Tx Chain Disable (PCI_PTxD)

Offset: 0x0804
internal address: 0x1010_0804
PCI address: 0x1_0804
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: To stop transmission for endpoint *N*:

1. Write a 1 to endpoint *N*'s FTxD bit.
2. Poll the LB_FTxE register until endpoint *N*'s FTxE bit is clear.
3. Write a 0 to endpoint *N*'s FTxD bit; at this point, endpoint *N* has shut down and has no pending DMA transfers.

When N's FTxD bit is set, software must not write a 1 to N's FRxE bit as it causes an undefined operation. The software must set and endpoint's FTxE bit only when the FTxD bit is clear. However, writing a 0 to this bit while FRxD is set has no effect on *N*.

Bit	Bit Name	Description
0		PCI transmit disable bit for endpoint 0. Resets to 0x0.
1		PCI transmit disable bit for endpoint 1. Resets to 0x0.
2		PCI transmit disable bit for endpoint 2. Resets to 0x0.
3		PCI transmit disable bit for endpoint 3. Resets to 0x0.
31:4	RES	Reserved

3.5.18 PCI Tx Descriptor Pointer (PCI_PTxDP)

Offset: 0x0810 + (EP << 2)
Internal address: 0x1010_0810 + (EP << 2)
PCI address: 0x1_0810 + (EP << 2)
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
1:0	RES	Reserved
31:2		PCI transmit descriptor pointer. Points to the next PCI Tx descriptor used by the endpoint's DMA engine.

3.5.19 PCI Rx Chain Enable (PCI_PRxE)

Offset: 0x0900
Internal address: 0x1010_0900
PCI address: 0x1_0900
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
0		PCI receive enable bit for endpoint 0. Resets to 0x0. ■ 0 = No effect ■ 1 = Sets endpoint 0's PRxE bit
31:1	RES	Reserved

3.5.20 PCI Rx Chain Disable (PCI_PRxD)

Offset: 0x0904
Internal address: 0x1010_0904
PCI address: 0x1_0904
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: To stop transmission for endpoint *N*:

1. Write a 1 to endpoint *N*'s FRxD bit
2. Poll the LB_FRxE register until endpoint *N*'s FRxE bit is clear
3. Write a 0 to endpoint *N*'s FRxD bit; at this point, endpoint *N* has shut down and has no pending DMA transfers

When *N*'s FRxD bit is set, software must not write a 1 to *N*'s FRxE bit as it causes an undefined operation. However, writing a 0 to this bit while FRxD is set has no effect on *N*.

Bit	Bit Name	Description
0		PCI receive disable bit for endpoint 0. Resets to 0x0.
31:1	RES	Reserved

3.5.21 PCI Rx Descriptor Pointer (PCI_PRxDP)

Offset: 0x0908
Internal address: 0x1010_0908
PCI address: 0x1_0908
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
1:0	RES	Reserved
31:2		PCI receive descriptor pointer. Points to the next PCI Rx descriptor used by the endpoint's DMA engine.

3.5.22 Reset Control (PCI_RC)

Offset: 0x4000
Internal address: 0x1010_4000
PCI address: 0x0_4000
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: Part of PCI_CLK domain. See the Reset Control (RC) Register Usage section in **ip/mac/doc/mac_registers.Txt** for the recommended use of this register.

Bit	Bit Name	Description
0		Warm reset to MAC. Gated by bit 18 (WMAC/WBB warm reset alias gating control) of RST_IF_CTL when is the PCI host. Resets to 0x1.
1		Warm reset to baseband logic. Gated by bit 18 (WMAC/WBB warm reset alias gating control) of RST_IF_CTL when is the PCI host. Resets to 0x1.
3:2	RES	Reserved
4		Warm reset to PCI core (auto-cleared after 64 PCI clocks). Resets to 0x0.
31:5	RES	Reserved

3.5.23 Sleep Control (PCI_SCR)

Offset: 0x4004
Internal address: 0x1010_4004
PCI address: 0x0_4004
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: If the PCI bit is set in the reset control register, then this register resets as though cold reset had been asserted. Otherwise, this register is unaffected.
Notes: Part of PCI_CLK domain.

Bit	Bit Name	Description
15:0		Sleep duration, in units of 4096 sleep clocks (if the sleep clock rate is 32 MHz, then 4096 sleep clocks is 128 µs, or 1/8th of an 802.11 TU. Other sleep clock rates yield different durations). Resets to an undefined value.
17:16		Sleep enable. Resets to 0x1 (force sleep). ■ 0 = Force wake (i.e., force negation of SLEEP_EN signal to clkgen) ■ 1 = Force sleep (i.e., force assertion of SLEEP_EN signal to clkgen) ■ 2 = Allow sleep logic to control sleep/wake state (normal operation) ■ 3 = Reserved
18		Sleep duration timing policy. Resets to 0x0. ■ 0 = Sleep counter resets at each occurrence of TBTT when the chip is awake ■ 1 = Sleep counter resets at each occurrence of TBTT when the chip is awake and the sleep duration has already expired
19		Sleep duration write handling policy. Resets to 0x0. ■ 0 = Sleep counter set to the value of bits [15:0] each time the SCR is written. ■ 1 = Sleep counter set to zero (i.e., expires) each time the SCR is written
20		Sleep policy mode. Resets to 0x0. ■ 0 = Use station in a BSS sleep policy mode ■ 1 = Use ad hoc sleep policy mode
21		Sleep performance counter MIB interrupt enable. Resets to 0x0. ■ 0 = The sleep performance counter logic never generates a MIB interrupt, regardless of the values of the various sleep performance counter registers. ■ 1 = When the most-significant bit of any of the sleep performance counter registers (SPC_x) becomes set, the logic signals a MIB interrupt.
31:22	RES	Reserved

3.5.24 PCI Clock Domain Interrupt Pending (PCI_INTPEND)

Offset: 0x4008
Internal address: 0x1010_4008
PCI address: 0x0_4008
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: Part of PCI_CLK domain.

Bit	Bit Name	Description
0		Indicates whether the MAC is asserting the PCI INTA# signal. Resets to 0x0. ■ 0 = The MAC is not asserting INTA# ■ 1 = The MAC is asserting INTA# Note that if this bit is asserted, the ISR registers must be read to determine what interrupts are pending, and to clear the INTA# assertion.
31:1	RES	Reserved

3.5.25 Sleep Force (PCI_SFR)

Offset: 0x400C
Internal address: 0x1010_400C
PCI address: 0x0_400C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: If the PCI bit is set in the reset control register, then this register resets as though cold reset had been asserted. Otherwise, this register is unaffected.
Notes: Part of PCI_CLK domain.

Bit	Bit Name	Description
0		■ 0 = has no effect ■ 1 = Sleep mode entered immediately
1		■ 0 = has no effect ■ 1 = Sleep mode exited immediately
31:2	RES	Reserved

3.5.26 PCI Clock Domain Configuration/ Status (PCI_CFG)

Offset: 0x4010
Internal address: 0x1010_4010
PCI address: 0x0_4010
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: If the PCI bit is set in the reset control register, then this register resets as though cold reset had been asserted. Otherwise, this register is unaffected. Bits [1] and [2] are exceptions to this rule; see field descriptions for more details.
Notes: Part of PCI_CLK domain.

Bit	Bit Name	Description
0	RES	Reserved
1		Sleep clock select. Resets to 0x0 only on cold reset, but is overwritten by SLEEP_CLK_SEL bit value in the EEPROM, if EEPROM loading is enabled. Unaffected by warm reset. ■ 0 = Use the 32 MHz REFCLK input from the RF chip as the sleep clock ■ 1 = Use the clock connected to the MAC's external sleep clock input as the sleep clock. The external sleep clock input is a pin on the MAC/PHY chip to which an alternate (and typically much slower) clock may connect.
2		CLKRUN enable. Resets to 0x0 only on cold reset, but is overwritten by CLKRUN_ENABLE bit value in the EEPROM, if EEPROM loading is enabled. Unaffected by warm reset. ■ 0 = Force host to keep the PCI clock running continuously ■ 1 = Permit host to halt PCI clock when MAC is able to do so
4:3	RES	Reserved

Bit	Bit Name	Description
6:5		Association status (for LED control). Resets to 0x0. ■ 0 = Station is not associated and is not presently attempting to associate ■ 1 = Station is not associated but is presently attempting to associate ■ 2 = Station is associated ■ 3 = Reserved
9:7		PCI observation bus MUX select. Resets to 0x0.
10		Disable fix for bad PCI CBE# generation. Resets to 0x0. ■ 0 = Enable the fix ■ 1 = Disable the fix and potentially allow a bad CBE value to appear on the PCI bus
11		Enable interrupt line assertion when asleep. Resets to 0x0. ■ 0 = MAC does not assert INTA# when asleep or preparing to sleep ■ 1 = MAC asserts INTA# even if it is asleep or preparing to sleep
12		Enable fix for incorrect PCI command generation under certain PCI bus retry scenarios. See bug 6983 for more details. Resets to 0x0. ■ 0 = Disable the fix ■ 1 = Enable the fix
13		Disable logic to force chip awake when an interrupt is pending. Resets to 0x0. ■ 0 = Allow this logic to operate normally, in which case the chip is forced awake while an interrupt is pending ■ 1 = Disable this logic, in which case the chip is permitted to sleep even when an interrupt is pending
14		LED hysteresis on sleep exit disable. Attempts to correct an issue in which the LEDs blink too fast when the chip is simply exiting sleep mode, receiving a beacon, and going back to sleep. Resets to 0x0. ■ 0 = Enable the fix. On exit from sleep mode, the LEDs continue to behave as if the chip were still in sleep mode for ~20ms ■ 1 = Disable the fix. On exit from sleep mode, the LEDs immediately transitions to normal (bps) operation.
15		Power management state D0 to D3 transition handling policy. This bit controls whether the sleep enable field (bits [17:16]) of "Sleep Control (PCI_SCR)" is forced to the force sleep setting when the power management state in bits [1:0] of the PCI configuration space PMCSR transitions from power state D0 to power state D3. Resets to 0x0. ■ 0 = A D0 to D3 transition forces the SCR sleep enable field to the force sleep setting ■ 1 = A D0 to D3 transition leaves the SCR sleep enable field unchanged.
16		Sleep/power-down indication ■ 0 = The MAC is awake ■ 1 = The MAC is asleep
19:17		LED mode select. The association status field (bits [6:5]) must be set to the station is associated setting for this field to affect the LEDs. Resets to 0x0. ■ 0 = Blink rate is proportional to bps, and for received frames, count the bytes only from those frames that pass the PCU's Rx filter ■ 1 = Blink rate is proportional to bps, and for received frames, count the bytes from all frames on the air, regardless of whether the frames pass the PCU's Rx filter ■ 2 = Blink the power LED each time a byte is transmitted. Blink the network LED each time a byte is received, regardless of whether the frame passes the PCU Rx filter. For debugging. ■ 3 = Blink the LEDs randomly. ■ 4–7 = Reserved
22:20		LED blink threshold select. Resets to 0x0. LEDs have blink rates (blink threshold, slowest, three intermediate rates, and fastest). When the LED mode select is set to one of the two bytes-per-second modes, this field determines the mapping from bps of data transfer to each of the six LED blink rates. This field has no effect if the LED mode select field is not set to one of the bps modes. Table 3-8 lists the range of bps values to achieve each LED blink rate for each setting of the LED blink rate threshold field.
23		LED slowest blink rate mode. Resets to 0x0. ■ 0 = When using slowest blink rate, blink the LEDs ■ 1 = When using slowest blink rate, keep the LEDs off

Bit	Bit Name	Description
25:24		Sleep clock rate indication. Resets to 0x0. ■ 0 = Sleep clock is ~32 MHz ■ 1 = Sleep clock is ~4 MHz ■ 2 = Sleep clock is ~1 MHz ■ 3 = Sleep clock is ~32 KHz
31:26	RES	Reserved

Table 3-8. **LED Blink Rates**

LED	Blink Threshold	Slowest	1	2	3	Fastest
0	<8 K	8 K – 512 K	512 K – 1 M	1 M – 2 M	2 M – 4 M	>4 M
1	<4 K	4 K – 256 K	256 K – 512 K	512 K – 1 M	1 M – 2 M	>2 M
2	<2 K	2 K – 128 K	128 K – 256 K	256 K – 512 K	512 K – 1 M	>1 M
3	<2 K	2 K – 32 K	32 K – 64 K	64 K – 256 K	256 K – 1 M	>1 M
4	<4 K	4 K – 64 K	64 K – 128 K	128 K – 512 K	512 K – 2 M	>2 M
5	<8 K	8 K – 64 K	64 K – 128 K	128 K – 512 K	512 K – 2 M	>2 M
6	<8 K	8 K – 128 K	128 K – 256 K	256 K – 1 M	1 M – 2 M	>2 M
7	<4 K	4 K – 64 K	64 K – 128 K	128 K – 256 K	256 K – 1 M	>1 M

3.5.27 Silicon Revision (PCI_SREV)

Offset: 0x4020
Internal address: 0x1010_4020
PCI address: 0x0_4020
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Part of PCI_CLK domain. See **//depot/ip/mac/doc/srev.Txt** for a list of chip version and revision levels.

Bit	Bit Name	Description
3:0		Chip revision level (0=initial tapeout, etc.)
7:4		Chip version indication
31:8	RES	Reserved

3.5.28 Sleep Enable Alias (PCI_SLE)

Offset: 0x4024
Internal address: 0x1010_4024
PCI address: 0x0_4024
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: If the PCI bit is set in the reset control register, then this register resets as though cold reset had been asserted. Otherwise, this register is unaffected.
Notes: Part of PCI_CLK domain. This register allows the sleep enable field of the "Sleep Control (PCI_SCR)" alter without causing a reload of the sleep duration counter in the MAC sleep logic. Writes to this register change the same physical register bits as a write to the sleep control register.

Bit	Bit Name	Description
15:0	RES	Reserved
17:16		Sleep enable. See description in "Sleep Control (PCI_SCR)" on page 68.
31:18	RES	Reserved

3.5.29 TxE Write Posting (PCI_TxEPOST)

Offset: 0x4028
Internal address: 0x1010_4028
PCI address: 0x0_4028
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: If the PCI bit is set in the reset control register, then this register resets as though cold reset had been asserted. Otherwise, this register is unaffected.
Notes: Part of PCI_CLK domain.

Bit	Bit Name	Description
9:0		Values to write to the TxE bits. Bit Q of this field (Q=[0...9]) corresponds to QCU Q's TxE bit. Resets to 0x0.
15:10	RES	Reserved
16		Valid indication. When set, indicates that a posted TxE write has not yet completed. When clear, indicates that no posted TxE writes are pending. Resets to 0x0.
31:17	RES	Reserved

3.5.30 QCU Sleep Mask (PCI_QSM)

Offset: 0x402C
Internal address: 0x1010_402C
PCI address: 0x0_402C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: If the PCI bit is set in the reset control register, then this register resets as though cold reset had been asserted. Otherwise, this register is unaffected.
Notes: Part of PCI_CLK domain.

Bit	Bit Name	Description
9:0		Selects which QCUs control when the MAC can sleep. The MAC does not sleep until all selected QCUs have their TxE bits clear and no pending frames. Resets to 0x3FF, which selects all QCUs.
31:10	RES	Reserved

3.5.31 PCI Debug 0 (PCI_DBG_0)

Offset: 0x4030
Internal address: 0x1010_4030
PCI address: 0x0_4030
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Part of PCI_CLK domain.

Bit	Bit Name	Description
2:0		mac_sleep state
5:3		mac_sleep state_coord
31:6	RES	Reserved

3.5.32 Sleep Performance Counter 0 Read-Only Alias (PCI_SPC_ROA_0)

Offset: 0x4060
Internal address: 0x1010_4060
PCI address: 0x0_4060
Access: Read-only; no write access, and reads do not clear the counter
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: See the SPC_0 register at offset 0x005C for read-and-clear access to this register

Bit	Bit Name	Description
23:0		The total number of cycles, in units of 256 sleep clocks, for which the chip was awake (the core clock was running). Resets to 0x0.
31:24	RES	Reserved

3.5.33 Sleep performance Counter 1 Read-Only Alias (PCI_SPC_ROA_1)

Offset: 0x4064
Internal address: 0x1010_4064
PCI address: 0x0_4064
Access: Read-only; no write access and reads do not clear the counter
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)
Notes: See the SPC_1 register at offset 0x0060 for read-and-clear access to this register.

Bit	Bit Name	Description
23:0		The total number of cycles, in units of 256 sleep clocks, for which the chip was asleep (the core clock was stopped). Note that if the baseband sleep control logic is programmed such that it does not shut off the core clock when the MAC requests it to, then the SPC_1 counter does not increment, because the chip remains awake even though the MAC sleep logic instructs the baseband logic to turn off the core clock. Resets to 0x0.
31:24	RES	Reserved

3.5.34 CIS Tuples

Offset: 0x5000–0x50FC
Internal addresses: 0x1010_5000 - 0x1010_50FC
PCI address: 0x0_5000 - 0x0_50FC

Table 3-9. **CIS Tuples**

Tuple	Offset
0	0x5000
1	0x5004
2	0x5008
...	...
62	0x50f8
63	0x50FC

3.6 SPI Flash Interface Registers

Table 3-10 summarizes the SPI flash interface registers for the AR2316. These registers use:

- Internal base address: 0x1130_0000
- External PCI MBAR_0 base offset: 0x1_7000

Table 3-10. **SPI Flash Interface Register Summary**

Offset	Name	Description	Page
0x0000	SPI_CS	SPI control/status	page 74
0x0004	SPI_AO	SPI address/opcode	page 75
0x0008	SPI_D	SPI data	page 75

3.6.1 SPI Control/Status (SPI_CS)

Offset: 0x0000
Internal address: 0x1130_0000
PCI address: 0x1_7000
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
3:0		Tx byte count. Determines the number of bytes transmitted from the AR2316 to the SPI device. Values of 1–8 are valid, other values are illegal. Resets to an undefined value.
7:4		Rx byte count. Determines the number of bytes received from the SPI device into the AR2316. Values of 0–8 are valid, other values are illegal. Resets to an undefined value.
8		SPI transaction start. Only writes to this field are meaningful; reads always return 0. Resets to 0x0. Writes: ■ 0 = No effect ■ 1 = Starts SPI transaction defined by the Tx byte count, Rx byte count, SPI_AO, and SPI_D registers.
15:9	RES	Reserved
16		Transaction busy indication. Read-only; writes to this bit are ignored. Resets to 0x0. ■ 0 = No SPI transaction is ongoing. Software may start a new SPI transaction by writing to the SPI transaction start bit within this register. ■ 1 = An SPI transaction presently is underway. Software must not try to start a new SPI transaction. Software may not alter the value of any field of the SPI_CS, SPI_AO, or SPI_D registers.
18:17		Automatically-determined SPI address size. Read-only; writes to this bit are ignored. Resets to an undefined value, but then updates after the autosizing process completes. ■ 0 = SPI address size is 16 bits ■ 1 = SPI address size is 24 bits ■ 2 = Reserved ■ 3 = Automatic SPI address size determination failed. Typical because: – The SPI device is missing – The SPI device is unprogrammed – The SPI device is programmed with an incorrect SPI_MAGIC value
20:19		SPI autosize override. Resets to 0x0. ■ 0 = Use automatically-determined SPI address size (see bits [18:17]) ■ 1 = Force SPI address size to 16 bits ■ 2 = Force SPI address size to 24 bits ■ 3 = Reserved
23:21	RES	Reserved
25:24		SPI clock frequency select. Resets to 0x11. ■ 0 = SPI clock frequency is proc_clk/8 ■ 1 = SPI clock frequency is proc_clk/16 ■ 2 = SPI clock frequency is proc_clk/32 ■ 3 = SPI clock frequency is proc_clk/64
31:26	RES	Reserved

3.6.2 SPI Address/Opcode (SPI_A0)

Offset: 0x0004
Internal address:
PCI address:
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
7:0		SPI opcode. Usually this field specifies the 8-bit opcode (instruction) to transmit to the SPI device as the first part of an SPI transaction.
31:8		Address. Usually this field specifies the 24-bit address to transmit to the SPI device.

3.6.3 SPI Data (SPI_D)

Offset: 0x0008
Internal address: 0x1130_0008
PCI address: 0x1_7008
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
31:0		SPI data. This register usually specifies a series of up to four data bytes to transmit to or receive from the SPI device. Resets to an undefined value.

3.6.4 SPI Register Notes

An SPI transaction has three phases: an opcode transmit phase (always a single byte), followed by an optional address 0-3 byte transmit phase and optional 0-4 byte data transmit or receive phase. Thus an SPI transaction is a 1- to 8-byte transmit phase from the AR2316 to the SPI device followed by a 0- to 8-byte receive phase from the SPI device into the AR2316.

The SPI_CS register transmit byte count field controls the size (in bytes) of the transmit phase. Each transmitted byte's source is fixed.

Table 3-11. **SPI_CS Transmitted Byte Source**

Byte	Source
0	SPI_AO[7:0] (SPI opcode field)
1	SPI_AO[31:24] (high byte of the SPI address field)
2	SPI_AO[23:16] (middle byte of the SPI address field)
3	SPI_AO[15:8] (low byte of the SPI address field)
4	SPI_D[7:0] (low byte of the SPI data register)
5	SPI_D[15:8] (next byte of the SPI data register)
6	SPI_D[23:16] (next byte of the SPI data register)
7	SPI_D[31:24] (high byte of the SPI data register)

The SPI_CS register receive byte count field controls the size (in bytes) of the receive phase. Each received byte's source is fixed.

Table 3-12. **SPI_CS Received Byte Source**

Byte	Source
0	SPI_D[7:0] (low byte of the SPI data register)
1	SPI_D[15:8] (next byte of the SPI data register)
2	SPI_D[23:16] (the byte of the SPI data register)
3	SPI_D[31:24] (high byte of the SPI data register)
4	SPI_AO[7:0] (SPI opcode field)
5	SPI_AO[15:8] (low byte of the SPI address field)
6	SPI_AO[23:16] (middle byte of the SPI address field)
7	SPI_AO[31:24] (high byte of the SPI address field)

1. Write appropriate values to the SPI_AO and SPI_D registers.
2. Write appropriate values into the transmit byte count and received byte count fields of the SPI_CS register.
3. Write a 1 to the SPI transaction SPI_CS register start bit (can combine with step 2).
4. To poll: poll the transaction busy indication bit in the SPI_CS register until set, indicating the SPI transaction is complete.
5. If a receive phase is included, retrieve the received data by reading the appropriate bytes from the SPI_D and SPI_AO registers.

4. Package Dimensions

The AR2316 is packaged in a JEDEC M0-205 compliant 233 PBGA package. The body size is 15 mm by 15 mm, and the ball pitch is 0.8 mm.

The PBGA package “PBGA233” drawings and dimensions are provided in Figure 4-1, and Table 4-1.

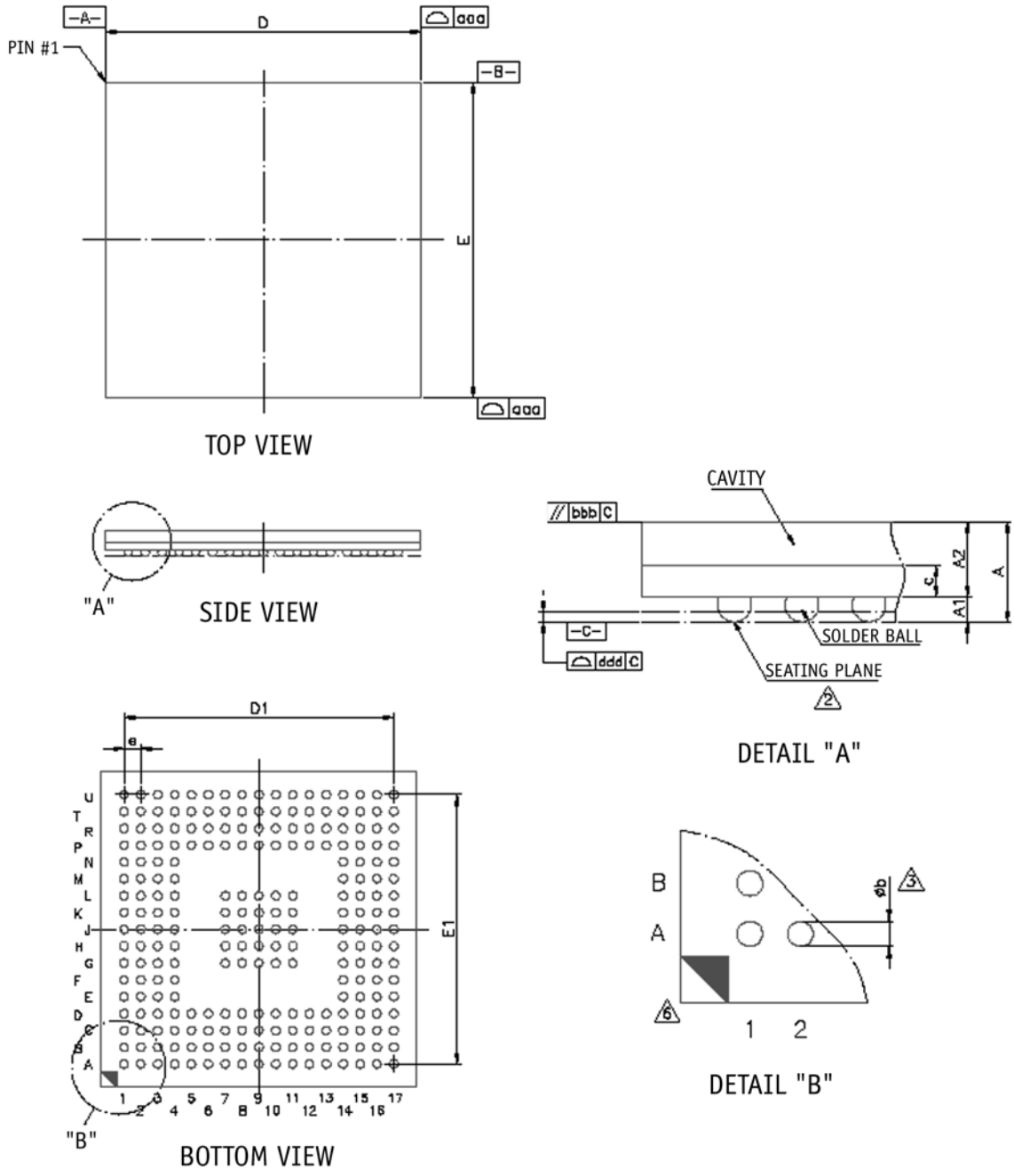


Figure 4-1. **PBGA Package “233” Views**

Table 4-1. **PBGA Package "233" Dimensions**

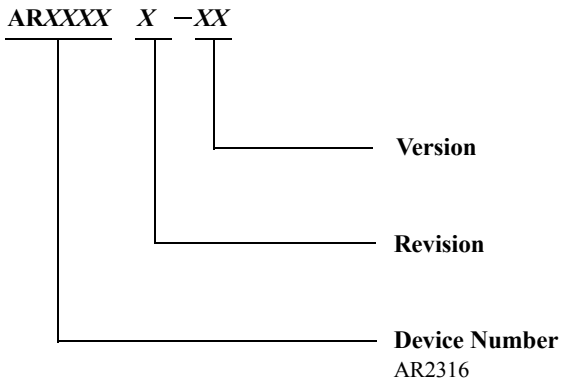
Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.4	mm	—	—	0.055	inches
A1	0.22	—	0.32	mm	0.0086	—	0.0125	inches
A2	0.38 REF			mm	0.0149			inches
A3	0.7 REF			mm	0.0275			inches
b	0.32	—	0.42	mm	0.0125	—	0.0165	inches
D	15.00 BASIC			mm	0.590 BASIC			inches
E	15.00 BASIC			mm	0.590 BASIC			inches
e	0.80 BASIC			mm	0.031 BASIC			inches
D1	12.80 BASIC			mm	0.503 BASIC			inches
E1	12.80 BASIC			mm	0.503 BASIC			inches

Notes:

1. The controlling dimension is mm.
   Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
   Datum C and seating plane are defined by the spherical crowns of the solder balls.
   There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.
   Reference document: JEDEC MO-205
   The pattern of pin 1 fiducial is for reference only.

5. Ordering Information

The order number is determined by the selection of these options. See the following example.



An order number, AR2316A-*00* specifies a current version of the AR2316.

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Document Number: 981-00030-001

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