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Excelpoint FA
Nov. 2009

Agenda



➤ **BC6888 Overview**

- CSR Roadmap
- Features
- Functional Block

➤ **BC6888 Bluetooth Reference Design**

- Schematic Design Guideline
- Layout Guideline

➤ **Bluetooth Performance**

- Power Consumption
- Migrate from BC3A18 to BC6888

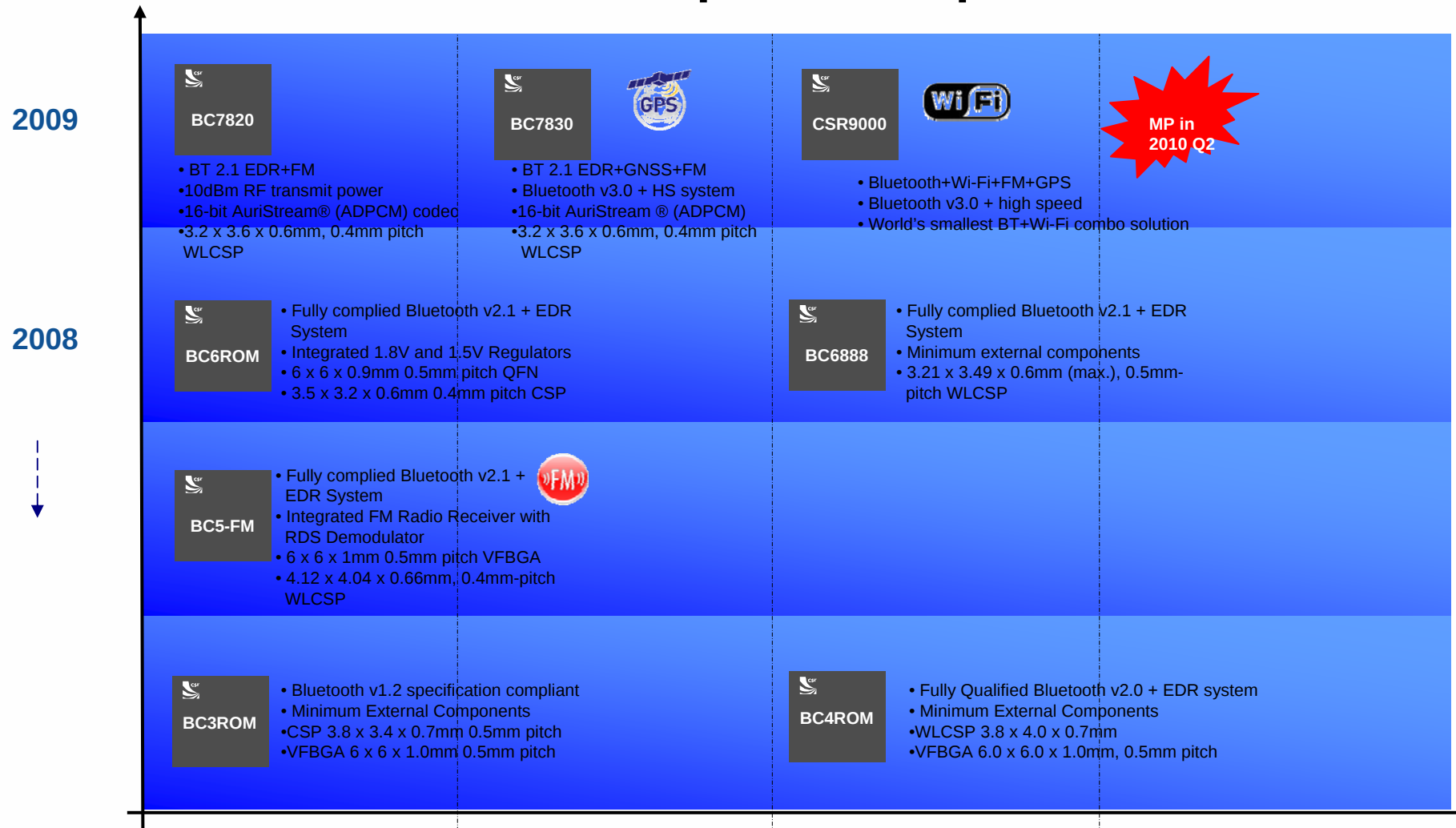
➤ **Summary**



BC6888 Overview



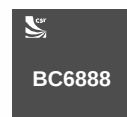
CSR Bluetooth ROM Chip Road Map



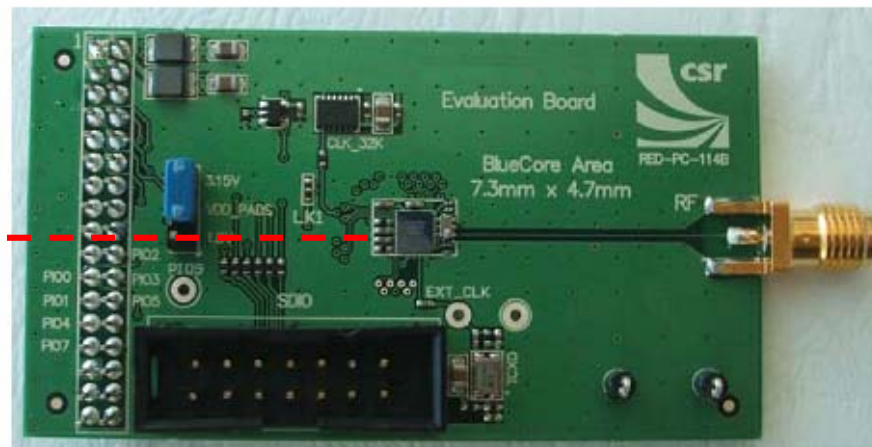
CSR BC6888 Features

Bluetooth Radio

- Bluetooth v2.1 + EDR Specification compliant
- +9dBm maximum RF transmit power
- Receiver sensitivity of -90dBm
- Support for 802.11 coexistence
- Class1 Performance without external PA/LNA



3.21 x 3.49 x 0.6mm (max.)
0.5mm-pitch WLCSP



CSR BC6888 Features

Baseband and Software

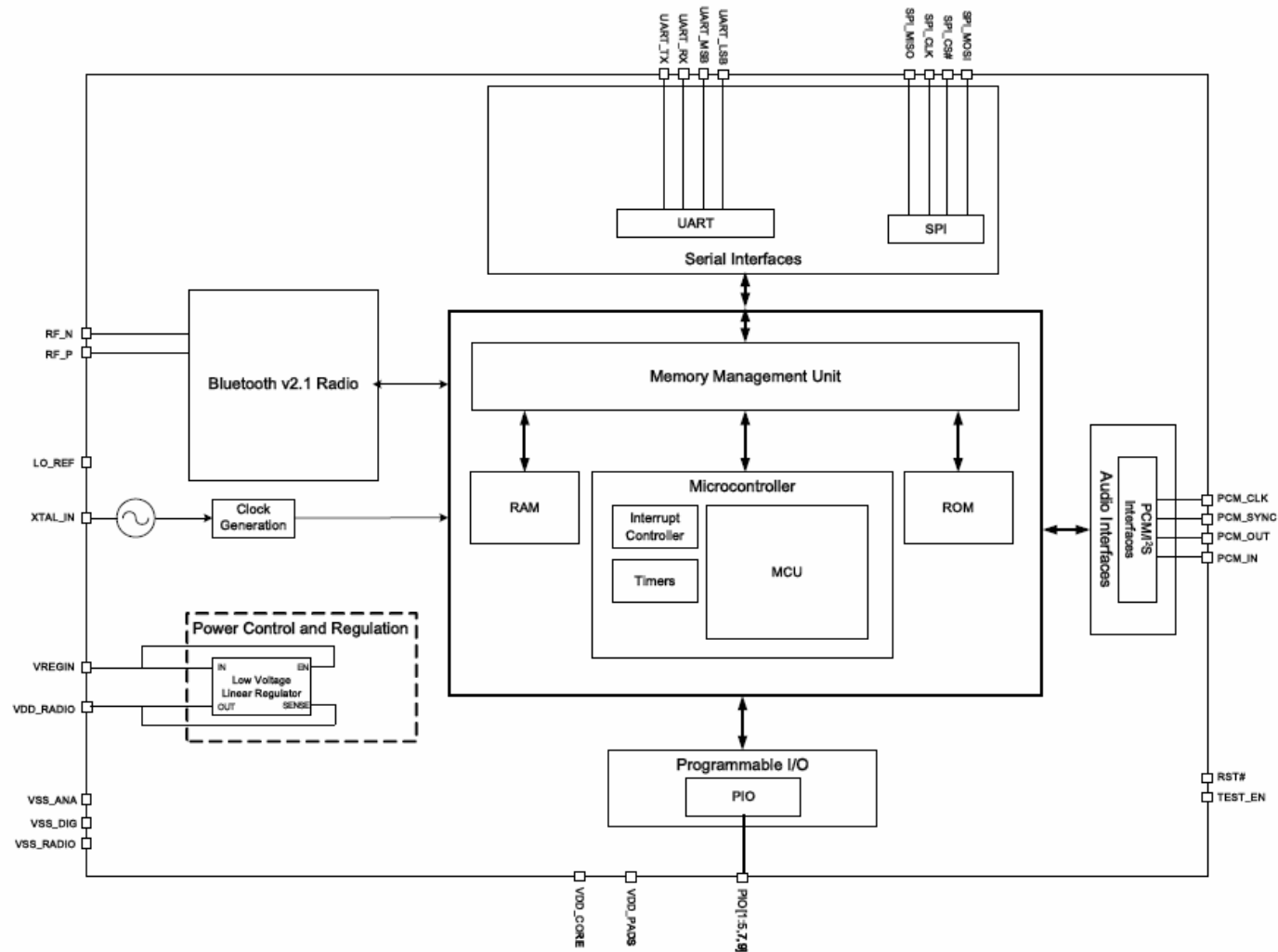
- AuriStream (16, 24, 32, 40 kbps) codec
- Internal 48kbyte RAM, allows full speed data transfer
- SPI interface up to 4Mbits/s for system debugging
- UART interface with programmable data rate up to 4Mbaud
- Bi-directional serial programmable audio interface supporting PCM and I2S formats

Auxiliary Features

- Clock request output to control an external clock
- On-chip low dropout linear regulator producing 1.5V core voltage from 1.8V
- Standard HCI over UART



Functional Block



BC6888 Reference Design



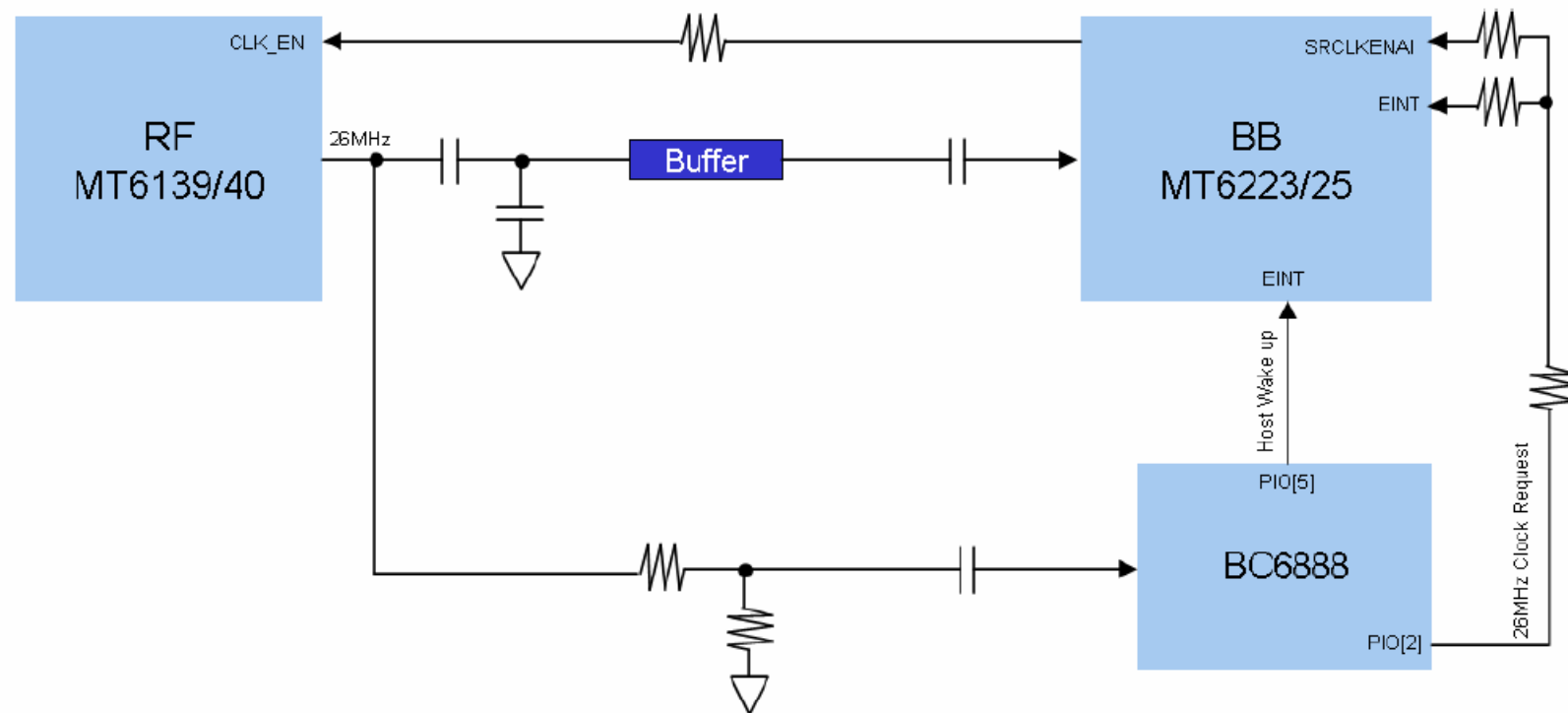
CSR Design Review Process

CSR have successfully supported many customers when it comes to implementation. Regarding RF design, we normally help customers' development with Design Review Process which includes:

- Provide CSR Reference Design
- Review Schematic/Gerbers
- Perform RF Evaluation on customer's prototype

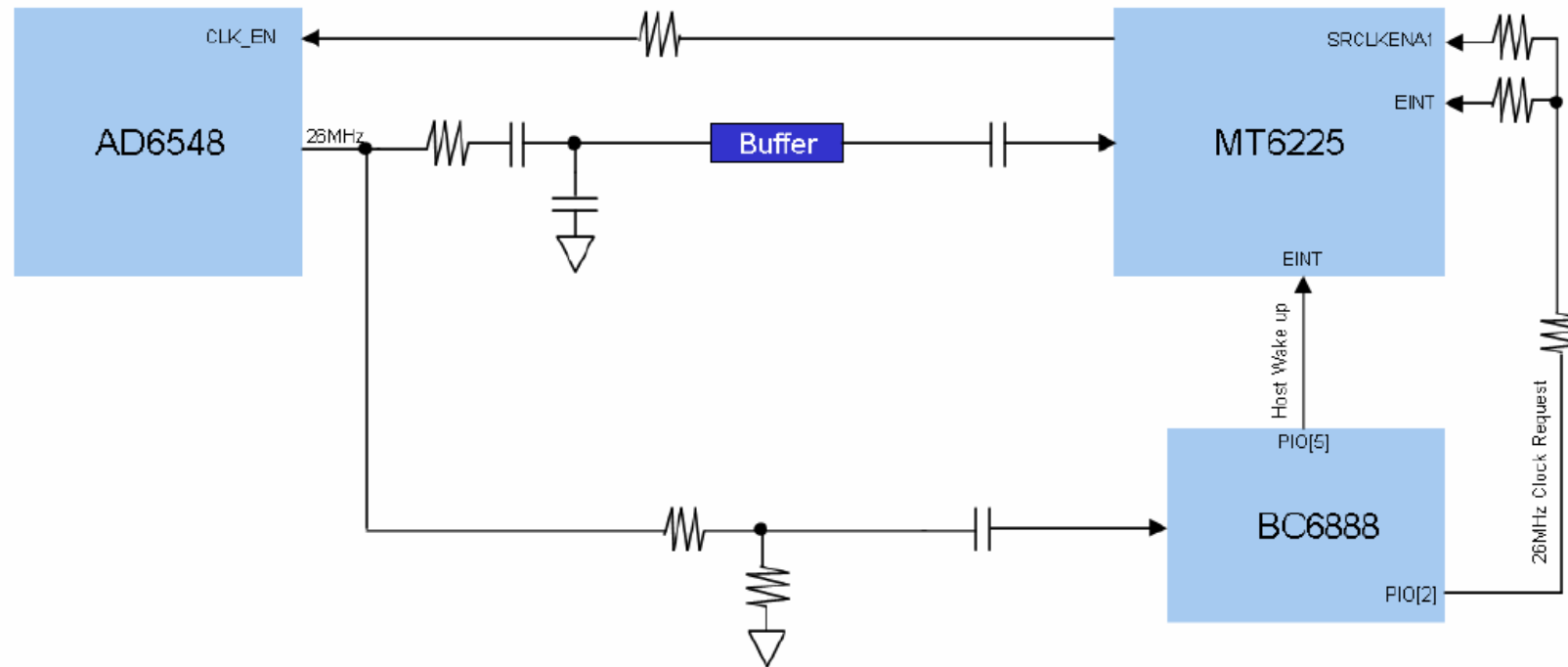


Schematic Design Guide



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Schematic Design Guide



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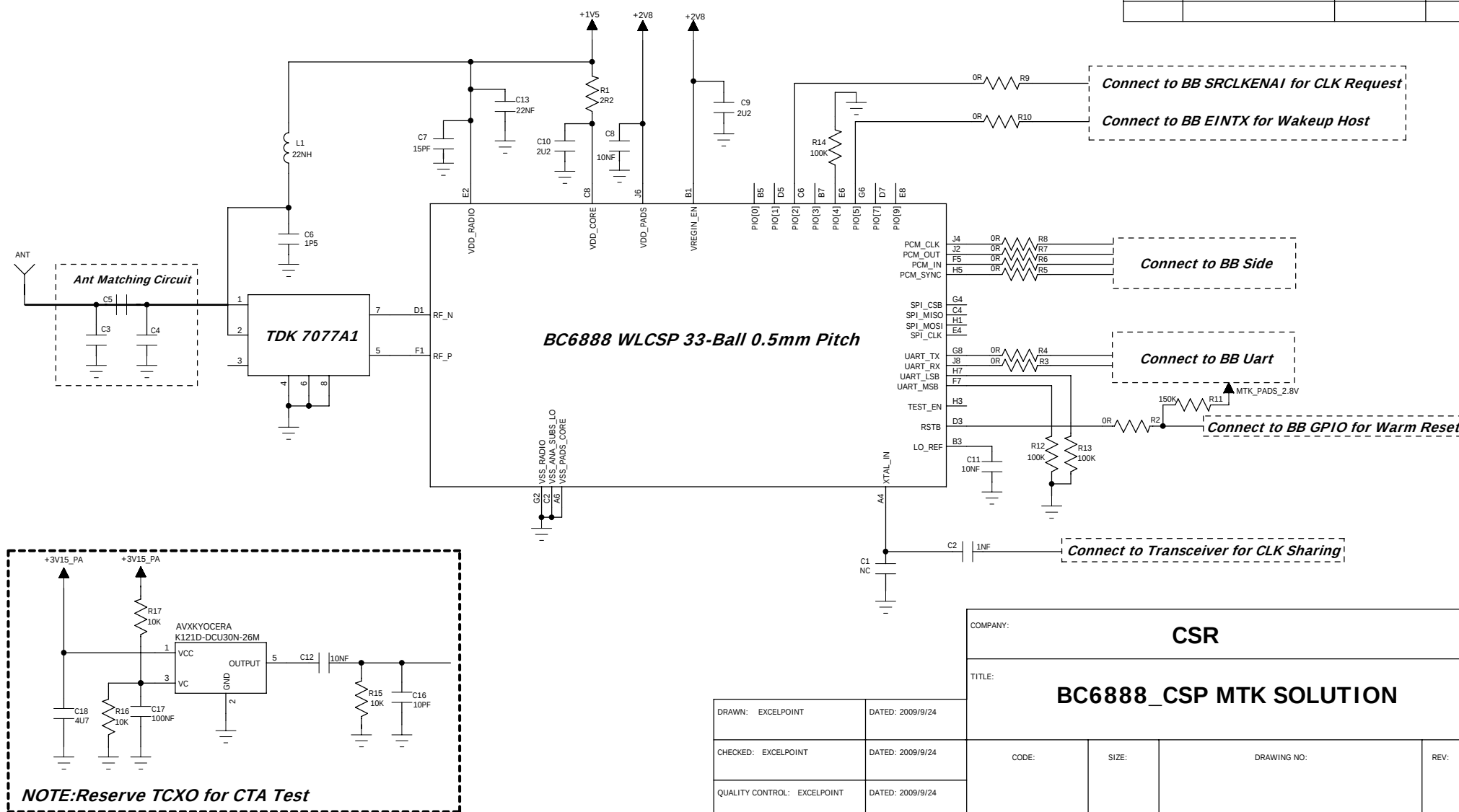
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REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:



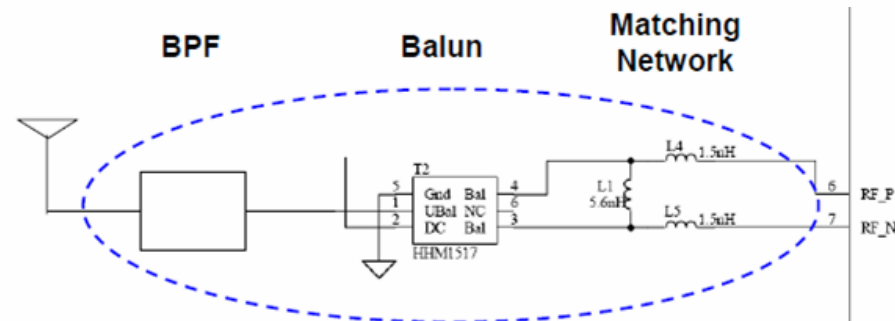
DRAWN: EXCELPPOINT	DATED: 2009/9/24
CHECKED: EXCELPPOINT	DATED: 2009/9/24
QUALITY CONTROL: EXCELPPOINT	DATED: 2009/9/24
RELEASED: EXCELPPOINT	DATED: 2009/9/24

COMPANY: CSR			
TITLE: BC6888_CSP MTK SOLUTION			
CODE:	SIZE:	DRAWING NO:	REV:
SCALE:			SHEET: OF

Schematic Design Guide- Radio

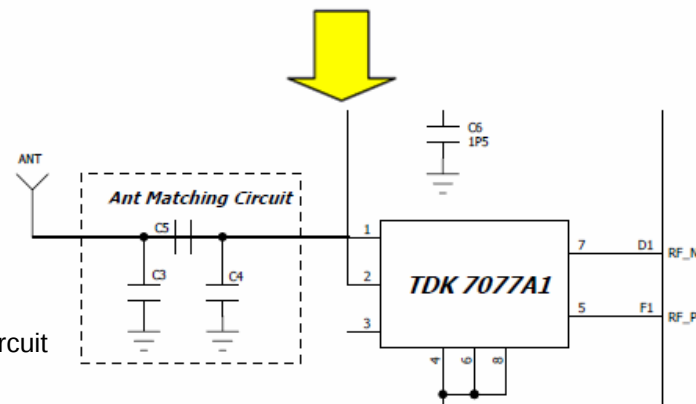
CSR recommend TDK7077A1 Combo-Balun solution for Mobile Application. This solution should give the following benefits; area, easy implementation, component count and cheaper cost.

Discrete Balun
(5 components)



Combo Balun
(1 component)

TDK7077A1 contains:
BPF + Balun + matching circuit



Schematic Design Guide – Host Interface Select

Pull PIO[4] low to select the UART.

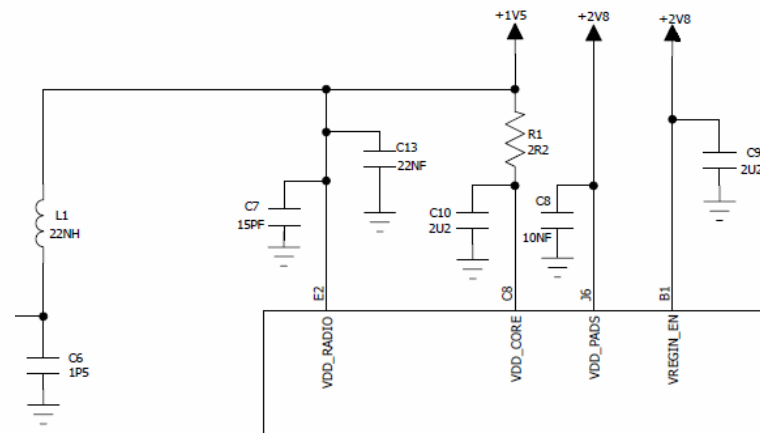
To select BCSP, connect 100KR pull-downs to both UART_MSB and UART_LSB.

UART_MSB	UART_LSB	UART Protocol
0	0	BCSP
0	1	H4
1	0	H4DS
1	1	H5



Schematic Design Guide- Power

1. R-C filtering is required on VDD_CORE to prevent high frequency clock edges from contaminating the 1.5V supply rail. This is essential to prevent 4MHz, 16MHz and 32MHz spurs from being generated on the VCO due to microprocessor.
2. The DC feed to the balun (hence to TX_A and TX_B) is via a 22nH inductor and 1pF RF decoupling capacitor. This helps to prevent RF energy from contaminating the 1.5V rail.
3. In MTK platform, BC6888 is supplied with 2.8V. When supplying 2.8V directly to VREGIN_EN, ensure that a 2.2 μ F capacitor to ground is connected.



Schematic Design Guide- Clock

BC6888 only support external clock.

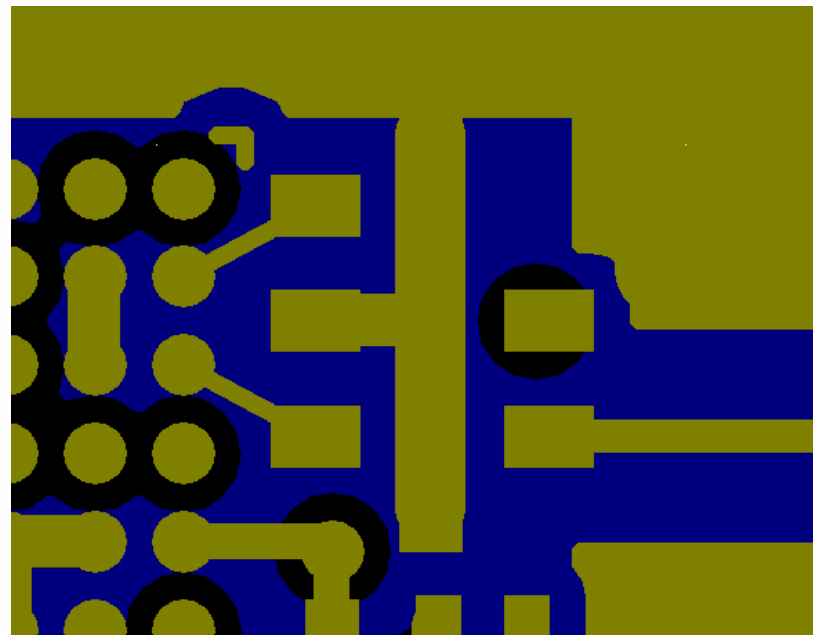
Clock Source	Min	Typ	Max	Unit
External Clock				
Input frequency ^(a)	12	26	52	MHz
Clock input level ^(b)	0.4	-	VDD_RADIO	V pk-pk
Edge jitter (allowable jitter), at zero crossing	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF



Layout Design Guide

Keep RF traces short in length

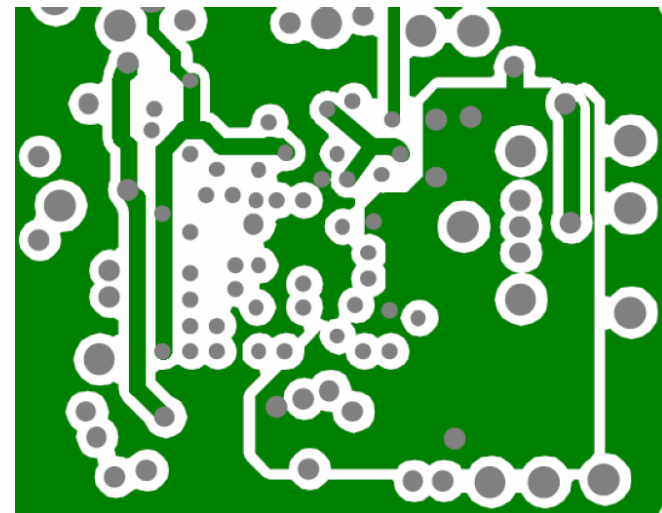
Use $50\ \Omega$ tracks for RF traces. Differential signal lines TX_A and TX_B should be of identical length. CSR qualified balance band-pass filter has been integrated with RX matching network so customers don't make any effort to do matching. A solid ground plane is required, particularly underneath the RF front-end section.



Layout Design Guide

Keep power traces as width as possible to reduce impedance

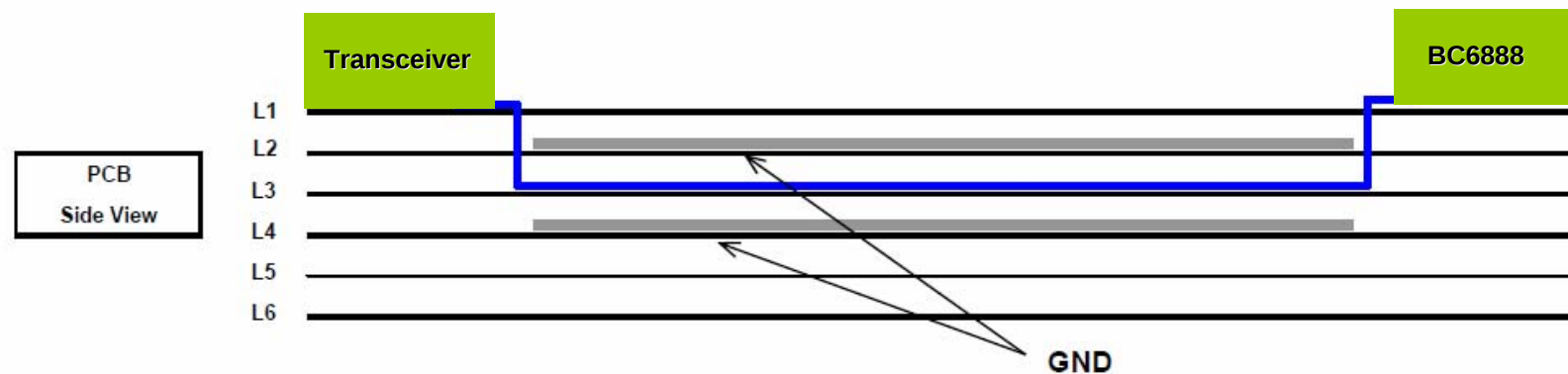
Place specific supply decoupling capacitors close to the corresponding BGA pin, with power trace running directly from BGA pin to decoupling capacitor to power net. The Radio supply, and balun supply are susceptible to RF pickup, hence, tracks for these supplies should be kept short and away from RF traces and components. Ground fill can assist in increasing isolation between these sections. The decoupling capacitor for VDD_Radio should be placed close to the chip. Routing the power line around the chip in internal layer, as routing under the chip is forbidden.



Layout Design Guide

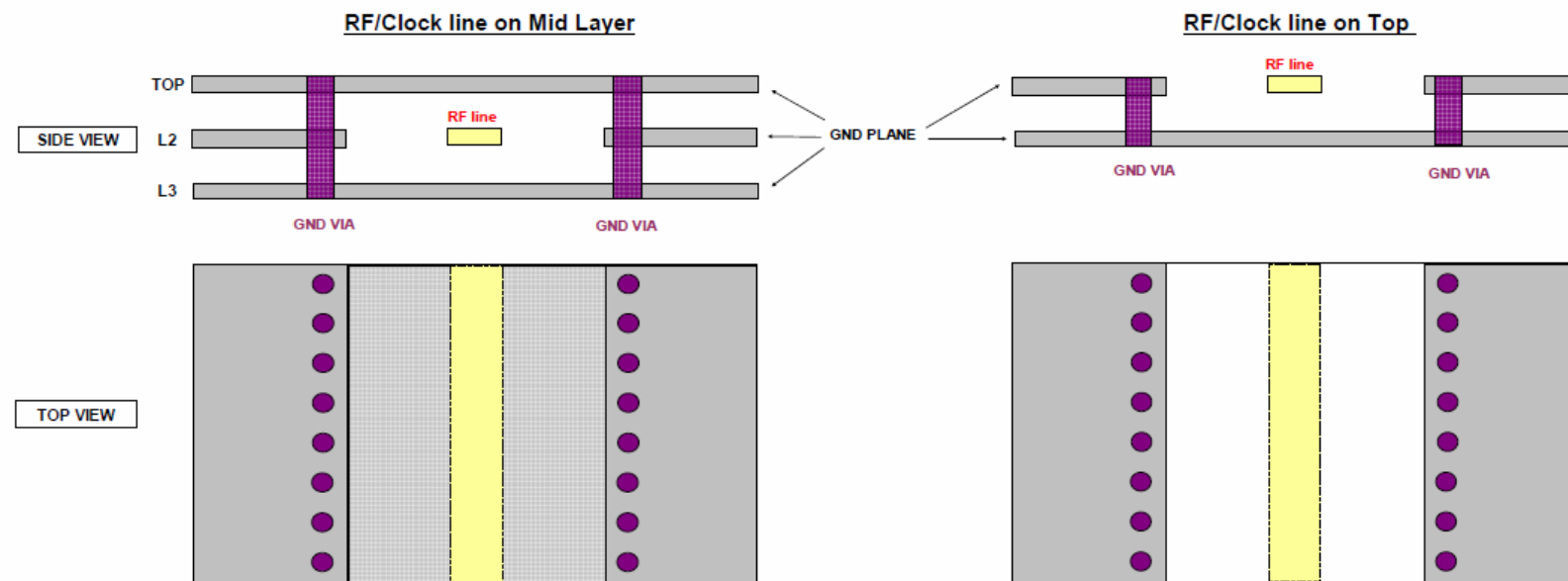
Protect clock lines well

Keep clock lines well protected from other signal noise. Do not run I/O traces parallel to clock traces (unless separated by a ground layer). Place a solid ground plane directly below (or above) clock lines that extends the full length of the clock tracks.



Layout Design Guide

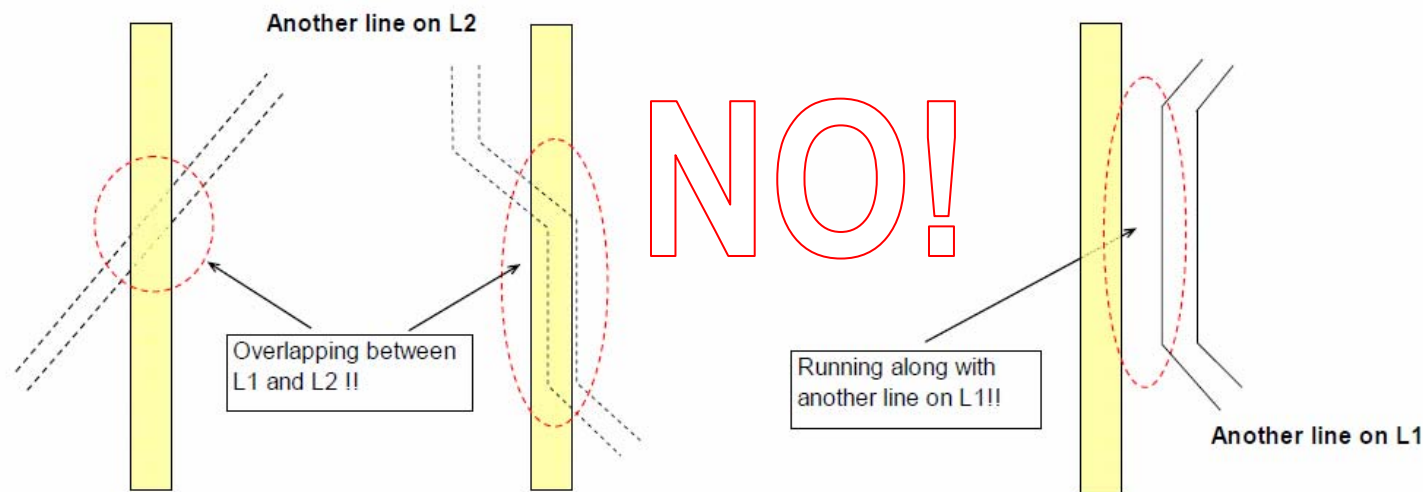
Protect clock lines well



Layout Design Guide

Protect clock lines well

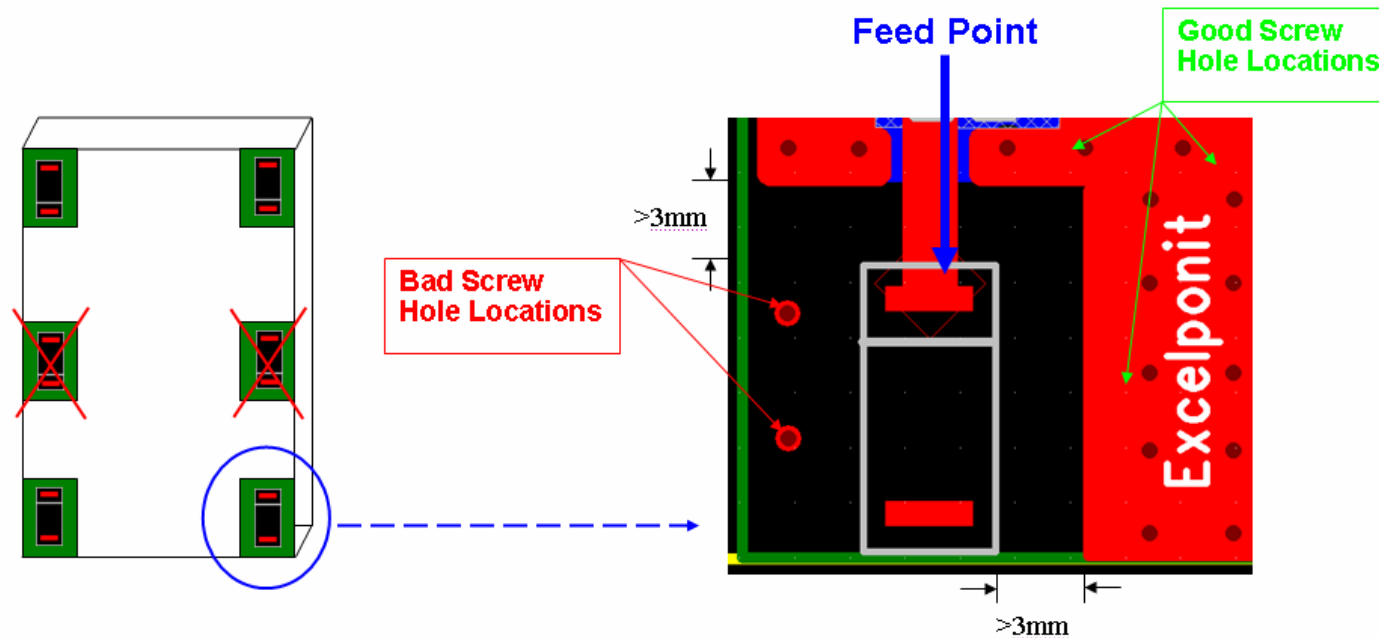
- No other lines run right underneath RF/Clock lines
- No other lines closely run along with RF/Clock lines on the same layer



Layout Design Guide

Antenna Placement

- Place the BT antenna in the corner of the PCB.
- Reserve enough distance between the antenna, ground and the shielding case.



CSR Bluetooth Performance



Power Consumption

HCI Power Consumption

Operation Mode	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.4	mA
Inquiry and page scan, time interval 1.28s	-	0.8	mA
ACL no traffic	Master	4	mA
ACL with file transfer	Master	9	mA
ACL 40ms sniff	Master	2	mA
ACL 1.28s sniff	Master	0.2	mA
eSCO EV5	Master	12	mA
eSCO EV3	Master	18	mA
eSCO EV3 - hands-free - setting S1	Master	18.5	mA
SCO HV1	Master	37	mA



Power Consumption

HCI Power Consumption

SCO HV3	Master	17	mA
SCO HV3 30ms sniff	Master	17	mA
ACL no traffic	Slave	14	mA
ACL with file transfer	Slave	17	mA
ACL 40ms sniff	Slave	1.6	mA
ACL 1.28s sniff	Slave	0.2	mA
eSCO EV5	Slave	19	mA
eSCO EV3	Slave	23	mA
eSCO EV3 - hands-free - setting S1	Slave	23	mA
SCO HV1	Slave	37	mA
SCO HV3	Slave	23	mA



Power Consumption

HCI Power Consumption

SCO HV3 30ms sniff	Slave	16	mA
Standby host connection (Deep-Sleep)	-	40	μ A
Reset (active low)	-	39	μ A

Note:

Conditions: 20°C, VREGIN 1.8V

VDD_PADS: 3.15V

UART BAUD rate: 115.2kbps



Migrate from BC3A18 to BC6888

Easily migration from BC3ROM design to BC6888

Hardware

- Reference schematic
- PCB layout guidance
- HW review

Software

- Protocol (Update lib and Add patch)
- Configuration





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Thank You!



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课程网址: <http://www.edatop.com/peixun/antenna/134.html>

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